Solutions Manual Errata for
Electronics, 2nd ed. by Allan R. Hambley

Problem 1.17

In line two, change 3.135 W to 3.125 W.

Problem 1.29

In line one, inside the first integral, delete the exponent 2 on i_1.

In line four, change $\frac{20/\sqrt{2}}{8}$ to $\frac{\left(20/\sqrt{2}\right)^2}{8}$.

In line five, change I_{iavg} to I_{1avg}.

Problem 1.49

Toward the end of the solution, change "when R_S changes from 1 MΩ to 10 kΩ" to "when R_L changes from 1 MΩ to 10 kΩ".

Problem 1.50

Change "when R_S changes from 0 to 100 Ω" to "when R_L changes from 0 to 100 Ω".

Problem 1.62

In line two of Part (b), change $\frac{1}{2}(G_{m1} + G_{m2})R_L$ to $(G_{m1} - G_{m2})R_L$. Make the same change in line two of Part (c).

Problem 2.12

In Part (d), change $\frac{1}{j\omega(99C)}$ to $\frac{1}{j\omega(101C)}$.

In the last paragraph, change 99-pF to 101-pF.

Problem 2.14

After the figure, change $v_o = 8v_{in}$ to $v_o = -8v_{in}$ and change the gain from 8 to –8.

Problem 2.16

At the end of the solution, after "For $A_{OL} = 10^5$", change $A_v = -9.998$ to $A_v = -9.9989$ and change $-R_2/R_1 = 10$ to $-R_2/R_1 = -10$.

Problem 2.33

The problem statement should have specified W_{space} = 10 μm instead of 5 μm.

Problem 2.38

In the figure, change the upper 10-kΩ resistor (connecting the inverting input to the output of the first op amp) to 15 kΩ.

Problem 2.43

In Part (b), Equation (4), change R_1 to R_2. In Part (c), in the first equation after the figure, change v_i to $-v_i$.

Problem 2.53

In the first line, change f_{0CL} to f_{BCL}.

Problem 2.73

Before the figure, add the sentence: "The PSpice simulation is stored in the file named P2_73."

Problem 2.75

Delete the sentence stating that the plot of $v_o(t)$ is on the next page.

Problem 3.10

In line three (an equation), change i_D/R to v_D/R.

Problem 3.53

In the sentence beginning with "The dynamic resistance", change nV_T/I_{CQ} to nV_T/I_{DQ}.

Problem 3.56

In Part (a), change nV_T/I_{CQ} to nV_T/I_{DQ}.

Problem 3.57

The solution uses r_d for the diode resistance rather than r_z as specified in the problem statement.

Problem 3.58

In Part (c), line two (an equation), change the minus sign inside the parentheses to a plus sign.

Problem 3.70

In line one, change "electon" to "atom".

Problem 3.90

In Part (c), line one, change the denominator of the fraction in parentheses from I_R to $-I_R$.

Problem 3.92

At the end of the solution, add: "Larger capacitance produces less output voltage ripple and higher peak diode current".

Problem 4.10

In line five of the solution (an equation), change "10 – 0.6585" to "0.6585 – 10".

Problem 4.25

In the equation for I_S (line seven of the solution), each of the two denominators should end with) – 1 instead of – 1).

Problem 4.34

In the line for part (d) with $\beta = 100$, we should have $I = 9.53$ mA (instead of 10 mA) and $V = 9.53$ V (rather than 10 V).

Problem 4.45

Change $A_{VO} = -\beta R_L/r_\pi$ to $A_{VO} = -\beta R_C/r_\pi$.

Problem 4.50

At the end of step one, add: "Set all other independent signal sources to zero."

Problem 4.54

Next to the figure, change V_{EQ} to V_{BEQ} .

Problem 4.60

In the first line after the figure, second equation, change I_{BEQ} to I_{BQ}.

Problem 4.65

In the first line after the figure, insert an equals sign after I_B.

Problem 5.3

Calculation of the drain currents was omitted. The drain currents are:

(a) $i_D = K(v_{GS} - V_{to})^2 = (W/L)(KP/2)(v_{GS} - V_{to})^2 = 2.25$ mA

(b) $i_D = K[2(v_{GS} - V_{to})v_{DS} - (v_{DS})^2]$

$= (W/L)(KP/2)[2(v_{GS} - V_{to})v_{DS} - (v_{DS})^2]$

$= 2$ mA

(c) $i_D = 0$

Problem 5.7

In the last sentence, change $K = 25$ to $K = 25\ \mu A/V^2$.

Problems 5.23

The last line of part (a) should read: $V_{DSQ} = 20 - 2I_{DQ} = 12$ V.

Problem 5.25

Change the second equation from $R_S I_{DSQ} = 6$ V to $R_S I_{DQ} \cong 6$ V.

Problem 5.46

Change "greater than zero" to "greater than unity".

Problem 5.65

In the third-to-last sentence, change $K(v_{GS5} - V_{to})$ to $K(v_{GS5} - V_{to})^2$.

Problem 5.74

In the sentence after the opening equation, change "saturation" to "triode region". In part (c) before the table, insert "Using the value of C given in part (d) of the problem, we have:"

Problem 6.16

At the beginning of the solution, insert "The following solution is for an inverter operating at 400 MHz." At the end of the solution, add "For an inverter operating at 400 Hz, $P_{dynamic} = 3.6 \times 10^{-10}$ W."

Problem 6.23

In the third line, change "$I_{OL} = -1$ mA" to "$I_{OL} = 1$ mA".

Problems 6.24

In the first line, change "$P_{dynamic} = If$ " to "$P_{dynamic} = Kf$".

Problem 6.25

In the equation for Energy, change $(4^2 - 1^2)$ to $(5^2 - 0^2)$ and change 150 pJ to 250 pJ. In the equation for $P_{dynamic}$, change 150 to 250 and change 3.75 mW to 6.25 mW.

Problem 6.32

In the circuit diagram, the device should be an enhancement MOSFET rather than a depletion MOSFET.

Problem 6.36

Change the middle of the fourth line to read "$V_{IH} = 2.04$ V, $V_{IL} = 1.08$ V".

Problem 6.51

At the end of the first paragraph, just before the figure, insert the following: [Note: The solution assumes $(W/L)_p = 1$. On the other hand for $(W/L)_p = 2$, we would need $(W/L)_n = 16$.]

Problem 7.1

Delete the comma after the phrase "high precision".

Problem 7.11

In the first sentence, change "below" to "on the next page".

Problem 7.18

Toward the end of the main paragraph, in the equation for R_2, insert a left-hand parenthesis the before 26mV.

Problem 7.20

Actually the current decreases when β decreases. Thus, the percentage increase should be stated as -0.99%.

Problem 7.22

At the beginning of part (a), add the following: (Note: The problem should have asked for proof that I_O, rather than I_{C2}, is independent of V_{BE}.)

Problem 7.25

In the first line, change V_{CC} in the fraction numerator to 10.

Problem 7.28

In the first sentence after the diagram, change P7_27 to P7_28.

Problem 7.37

In the third line, change $(15 + V_{GS1} - V_{GS3})$ to $(15 - V_{GS1} - V_{GS3})$.

Problem 7.38

At the beginning of the solution, add the following: "The problem statement should refer to Figure P7.38, not P7.36."

Problems 7.60 and 7.61

In the next-to-last sentence of each solution, change A_{cm} to $A_{v\text{cm}}$.

Problem 7.65

In the first paragraph, change the value found for A_{v1} from 64.6 to 36.23. At the end of the solution, change the value found for the overall gain A_v from 20.4×10^3 to 11.5×10^3.

Problem 7.66

At the end of the solution, add the following sentence: "The *pnp* stage drops the dc level down so it comes out zero after the last (Q_6) stage."

Problem 7.67

Throughout the solution, change all occurrences of $2000\pi t$ to $200\pi t$.

Problem 7.71

After the diagram, add the following: (Note: For the transistors to operate in the active region, the emitters of the current sinks must be connected to $-V_{EE}$ rather than to ground.)

In the third line of the main paragaph, change "Q_3 is a simple mirror" to "Q_8 is a simple mirror".

Problem 7.74

In the the top line of page 327, change (10 μA)/β to (100 μA)/β.

Problem 7.75

At the very end, change the value found for A_1/A_2 from 0.953 to 0.926.

Problem 8.8

In part (a) of the solution, the components of the phase plot are incorrectly added. The correct phase plot should show a phase of +90° for low f, 0° for high f, and should decrease in a straight line between 3.18 MHz and 318 MHz.

Problem 8.14

In the first line of part (b), change "drain" to "source". Notice that the expression abbreviated as B simplifies to $C_{gs}(R_{sig}+R_L') + C_{gd}R_{sig}(g_m R_L' + 1)$, and the expression abbreviated as A simplifies to $C_{gs}C_{gd}R_{sig}R_L'$.

Problem 8.18

In part (e), change "$r_d = \infty$ (because $\lambda = 0$)" to "$r_d \cong 1/\lambda I_{DQ} = 40$ kΩ". Change the sentence about the break frequency to read simply: "The break frequency is 251 kHz."

Problem 8.24

Change the table to appear thus:

R_L	1 kΩ	10 kΩ
R_L'	995 Ω	9.52 kΩ
A_V	-4.99	-9.05
$R_{in,Miller}$	33.4 kΩ	19.9 kΩ
R_x	25.0 kΩ	16.6 kΩ

Problem 8.25

Change the second line after the first figure to read:

$R_{in} = R_i || R_{in,Miller} \cong 0.1\ \Omega$.

Problem 8.30

Change "Equations 8.41 and 8.42" to "Equations 8.42 and 8.43".

Problem 8.33

In the second line change "Problem 8.33" to "Problem 8.32". In the equation for i_C, change 50sin(2000πt) to 500sin(2000πt). Change the value found for $I_{C,rms}$ to 354 μA.

Problem 8.36

Note that in the equation for h_{oe}, the current term $\frac{1}{r_\pi + r_\mu}$ is small, and has been ignored.

Problem 8.40

In the first line of part (a), in the equation for I_{BQ}, change "100" to "(1mA)/100".

Problem 8.42

In the table, change the units of the right-column value of R_E from mΩ to MΩ.

Problem 8.43

In the middle of part (a), "Solving Equation (2) for v_o" should read "Solving Equation (2) for v_π". In part (b), R_{EF} should be R_{E1}.

Problem 8.56

In the second circuit diagram, change $R'_{sig} = R_{sig}||R_D$ to $R'_{sig} = R_{sig}||R_G$.

Problem 8.66

The derivation of C_1 should read as follows:

Thus, the input resistance of the amplifier is

$R_{in} = R_B||[r_{\pi 1} + (\beta + 1)(R_{E1}||R_{E2}||r_{e2})] = 1046\ \Omega$

The resistance in series with C_1 is $R_{in} + R_s = 1096\ \Omega$.

$C_1 = 1/(2\pi f_1 1096) = 1/(2\pi 10 \times 1096) = 14.5\ \mu F$

Also, in the equation for C_2, change "$1/(2\pi f_2 1168)$" to "$1/(2\pi f_2 1020)$".

Problem 9.7

In part (a) of the solution, the final equation should read

$$A_f = \frac{X_o}{X_s} = \frac{A_1 A_{2f}}{1 + \beta_2 A_1 A_{2f}} = \frac{A_1 A_2}{1 + \beta_1 A_2 + \beta_2 A_1 A_2}$$

Also, in line four of part (b) change A_2 to A_3 and change "a a gain" to "a gain".

Problem 9.10

Change > to >>.

Problem 9.14

Part (a) uses $|V_{BE}| = 0.7$ V in saturation, not 0.6 V as specified in the problem.

Problem 9.35

In the first line, delete the second occurrence of i_i.

Problem 9.44

In the last line, change "parallel" to "voltage".

Problem 9.45

The last sentence, should read: "Since we want $A\beta$ to be very large in magnitude, we choose small resistances for a current feedback network."

Problem 9.47

At the very end of the solution, change the units of the value found for R_{of} from Ω to $k\Omega$.

Problem 9.49

The problem should have called for $R_{mf} = -5000\ \Omega$. In the solution, change the units of the value found for R_{if} from $M\Omega$ to Ω.

Problem 9.51

In the third line of part (a), delete the second occurrence of v_i.

Problem 9.52

In part (a) change the equation that begins line four to

$$v_o/i_i = -A_v R_i \times \frac{R_L}{R_o + R_L} = -417\ \text{M}\Omega$$

In the last line of part (a), add a negative sign in front of the value found for β. In the fourth line of part (b), change $\beta = 1/R_f$ to $\beta = -1/R_f$.

Problem 9.53

In the third line of part (a), add a negative sign in front of $A_{vo}R_i$. At the end of part (a), change the value found for β to -2.16×10^{-5}. In part (b), in the first line after the diagram, add a negative sign after the = and before the fraction.

Problem 9.59

In part (d), change both instances of "1000*t*" to "100*t*".

Problem 9.64

In the last line, change 3500 Hz to 350 Hz.

Problem 9.66

In the next-to-last line, change "imaginary" to "complex".

Problem 9.72

In the next-to-last line, change 180° to –180°.

Problem 9.86

In part (c), the last two sentences should read: "Finally setting $A\beta = 1$ yields $A = -29$ and $\omega = \sqrt{6}/(RC)$. Thus an inverting amplifier is needed."

In part (d), change the sign on the last term from – to + in the denominator of the second equation.

Problem 10.11

Delete the closing parenthesis after 0.0025 in the middle of the first equation. Change the value found for θ_{JA} to 150 °C/W.

Problem 10.23

The trigonometric identity should read $2\sin^2(x) = 1 - \cos(2x)$. In the integral equation that follows, change $10\sin(4000\pi t)$ to $10\cos(4000\pi t)$.

Problem 10.27

In the fifth line, change the integrand to $[1 - \cos(2\omega t)]$.

Problem 10.35

In part (a), change $(V_{CC}/\sqrt{2})R_L$ to $(V_{CC}/\sqrt{2})^2/R_L$.

Problem 10.37

In part (d), the final equation should read

$$P_{Q1max} = (V_{CC}/2) \times V_{CC}/(2R_L) = V_{CC}^2/(4R_L) = 7.03 \text{ W}.$$

Problem 10.45

In Equation 10.49 in the text, $\frac{R_2}{R_1 + R_2}$ should be replaced by $\frac{R_1 + R_2}{R_2}$.

Problem 10.50

In the second line of the solution, change "op amp" to "transistor".

Problem 10.63

In the second line, change "on the next page" to "below".

Problem 11.16

In the equation for C, insert a closing square bracket after the L.

Problem 11.21

In the third line of the solution, change $\omega_R = 3\omega_0$ to $f_R = 3f_0$.

Problem 11.37

In the first line after the last set of diagrams, change $Q_2^2 = R_L / R_s$ to $Q_2 = \sqrt{R_L / R_s}$.

Also note that in the first diagram of the solution, R_S represents the internal source resistance, while in the rest of the solution, R_S represents the series equivalent of R_L.

Problem 11.38

Note that R_s represents the series equivalent of R_L. In the second line, note that Q_C = 10 and change the value found for R_S to 5 Ω. In the third line, change 4.47 to 3.16, change 1423.5 to 1006.6, and change 409.77 to 465.2. Then the simulation results closely match predictions.

Problem 11.39

Note that R_s represents the series equivalent of R_L. In the second line, change the value found for R_s to 50 mΩ. (Note that Q_C = 100.)

Problem 11.45

In part (c), change 256.51 pF to 316.43 pF and change 20.21 nF to 1269 pF.

Problem 11.50

Note that in the solution r_d has been taken to be very large.

Problem 11.54

At the end of the solution sentence, change the period to a comma and add "or approximately 20 MHz. The third overtone frequency is about 30 MHz."

Problem 11.57

Note that "antiresonant frequency" means the same thing as "parallel-resonant frequency."

Problem 12.11

Note that in the solution, "node 2" refers to the noninverting input.

Problem 12.12

After the first paragraph, change $v_O = V_B + 4.7$ to $v_O = V_B - 4.7$. After the second paragraph, change $v_O = V_B - 4.7$ to $v_O = V_B + 4.7$ and change $v_{in} > V_B$ to $v_{in} < V_B$. In the plot at the end of the solution, change –1.3 on the y-axis to –1.7.

Problem 12.17

Note that in the problem statement, the v_2 referenced in the ninth line should be v_1 .

Problem 12.40

At the end of the solution, change $i_O R/2$ to $-i_O R/2$ and change 9.96 V to –9.96 V.

Chapter 1

Exercise 1.1

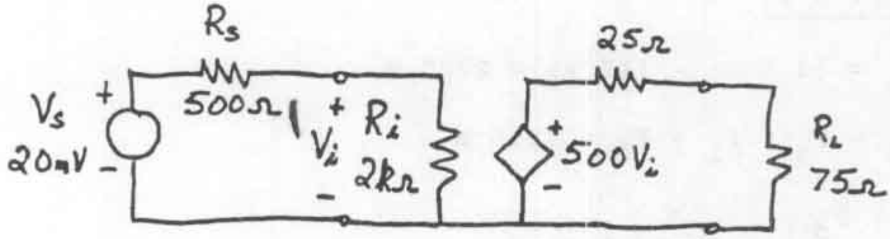
(a) For a noninverting amplifier $A_v = +50$ and we have:

$$v_o(t) = A_v v_i(t) = 50 \times 0.1\sin(2000\pi t) = 5\sin(2000\pi t)$$

(b) For an inverting amplifier $A_v = -50$ and we have:

$$v_o(t) = A_v v_i(t) = -50 \times 0.1\sin(2000\pi t) = -5\sin(2000\pi t)$$

Exercise 1.2



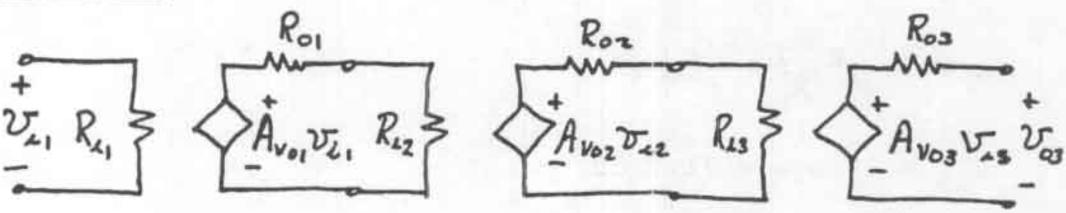
$$A_{vs} = \frac{R_i}{R_s + R_i} \times A_{vo} \times \frac{R_L}{R_L + R_o} = 300 \qquad A_i = A_v \frac{R_i}{R_L} = 10^4$$

$$A_v = \frac{V_o}{V_i} = A_{vo} \times \frac{R_L}{R_L + R_o} = 375 \qquad G = A_v A_i = 3.75 \times 10^6$$

Exercise 1.3

For maximum power transfer to the load, we must have $R_L = R_o = 25\ \Omega$. Then as in Exercise 1.2 we find $A_v = 250$, $A_i = 2 \times 10^4$, and $G = 5 \times 10^6$.

Exercise 1.4



$$A_{vo} = A_{vo1} \frac{R_{i2}}{R_{o1} + R_{i2}} A_{vo2} \frac{R_{i3}}{R_{o2} + R_{i3}} A_{vo3} = 5357$$

$R_i = R_{i1} = 1000\ \Omega$ $\qquad$ $R_o = R_{o3} = 300\ \Omega$

Exercise 1.5

$$A_{vo} = A_{vo3} \frac{R_{i2}}{R_{o3} + R_{i2}} A_{vo2} \frac{R_{i1}}{R_{o2} + R_{i1}} A_{vo1} = 4348$$

$R_i = R_{i3} = 3000\ \Omega$

$R_o = R_{o1} = 100\ \Omega$

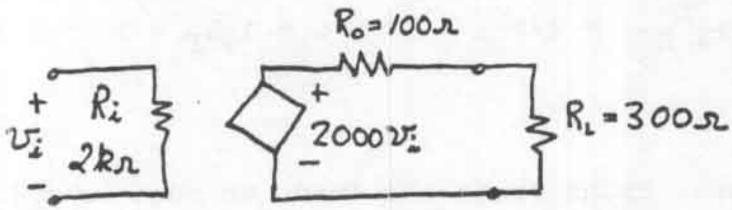
Exercise 1.6

$P_s = (1.5\text{ A}) \times (15\text{ V}) = 22.5\text{ W}$

$P_d = P_s + P_i - P_o = 20.5\text{ W}$

$$\eta = \frac{P_o}{P_s} \times 100\% = 11.1\%$$

Exercise 1.7



$$A_v = v_o/v_i = 2000 \frac{R_L}{R_L + R_s} = 1500$$

$A_{vdB} = 20\log|A_v| = 63.5\text{ dB}$

$$G = (A_v)^2 \frac{R_i}{R_L} = 1.5 \times 10^7$$

$G_{dB} = 10\log G = 71.8\text{ dB}$

Exercise 1.8

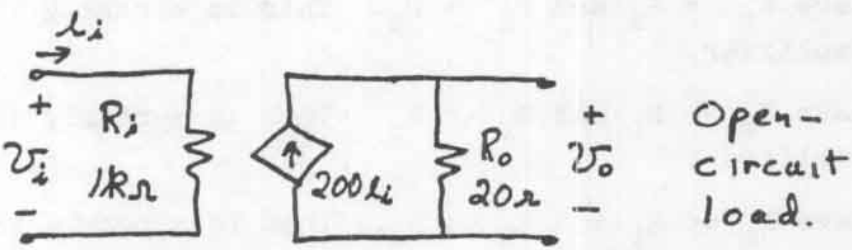
$$P_{dBW} = 10\log\left(\frac{P}{1\ W}\right) = 10\log\left(\frac{5\times10^{-3}}{1}\right) = -23.0\ dBW$$

$$P_{dBm} = 10\log\left(\frac{P}{1\ mW}\right) = 10\log\left(\frac{5\times10^{-3}}{10^{-3}}\right) = 10\log(5) = 6.99\ dBm$$

Exercise 1.9

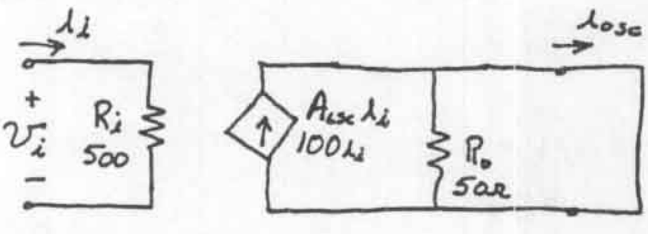
$$20\log\left(\frac{V_x}{1\ V}\right) = 23 \quad \Rightarrow \quad V_x = 10^{23/20} = 14.13\ V$$

Exercise 1.10



$$A_{vo} = \frac{v_o}{v_i} = \frac{200 i_i R_o}{i_i R_i} = 4 \qquad R_i = 1000\ \Omega \qquad R_o = 20\ \Omega$$

Exercise 1.11

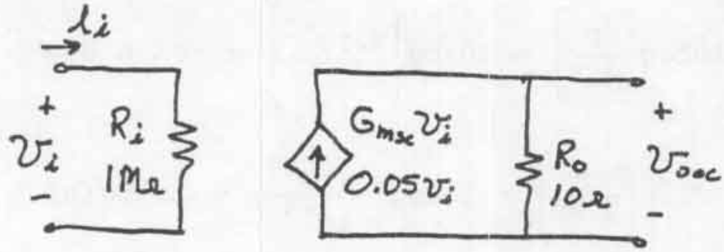


$$G_{msc} = \frac{i_{osc}}{v_i} = \frac{100 i_i}{500 i_i} = 0.2\ S$$

$R_i = 500\ \Omega$

$R_o = 50\ \Omega$

Exercise 1.12



$$R_{moc} = \frac{v_{ooc}}{i_i} = \frac{G_{msc}v_iR_o}{v_i/R_i} = G_{msc}R_oR_i = 500\ k\Omega$$

Exercise 1.13

(a) We have $R_s << R_i$ and $R_L >> R_o$. This is a nearly ideal voltage amplifier.

(b) We have $R_s >> R_i$ and $R_L << R_o$. This is a nearly ideal current amplifier.

(c) We have $R_s << R_i$ and $R_L << R_o$. This is a nearly ideal transconductance amplifier.

(d) We have $R_s >> R_i$ and $R_L >> R_o$. This is a nearly ideal transresistance amplifier.

(e) We have $R_s = R_i$ and $R_L << R_o$. This is not close to any ideal amplifier.

Exercise 1.14

$A_{cm} = v_{ocm}/v_{icm} = 0.1/1 = 0.1$

$A_{cmdB} = 20\log|A_{cm}| = -20$ dB

$$CMRR_{dB} = 20\log\frac{|A_d|}{|A_{cm}|} = 20\log\frac{50 \times 10^3}{0.1} = 114\ dB$$

Exercise 1.15

(a) $v_{id} = v_{i1} - v_{i2} = 1\text{ V}$

$v_{icm} = \frac{1}{2}(v_{i1} + v_{i2}) = 0\text{ V}$

$$v_o = A_1 v_{i1} - A_2 v_{i2} = \frac{A_1 + A_2}{2}$$

$$A_d = v_o/v_{id} = \frac{A_1/2 + A_2/2}{1} = \frac{1}{2}(A_1 + A_2)$$

(b) $v_{id} = v_{i1} - v_{i2} = 0\text{ V}$

$v_{icm} = \frac{1}{2}(v_{i1} + v_{i2}) = 1\text{ V}$

$v_o = A_1 v_{i1} - A_2 v_{i2} = A_1 - A_2$

$A_{cm} = v_o/v_{icm} = A_1 - A_2$

(c)

$$\text{CMRR} = 20\log\frac{|A_d|}{|A_{cm}|} = 20\log\left|\frac{A_1 + A_2}{2(A_1 - A_2)}\right| = 20\log\left|\frac{201}{2(100-101)}\right| = 40\text{ dB}$$

Problem 1.1

Some examples of electronic systems are electronic brakes, printers, cash registers, microwave ovens, CD players, airport landing systems, electronic door locks, and so forth.

Problem 1.2

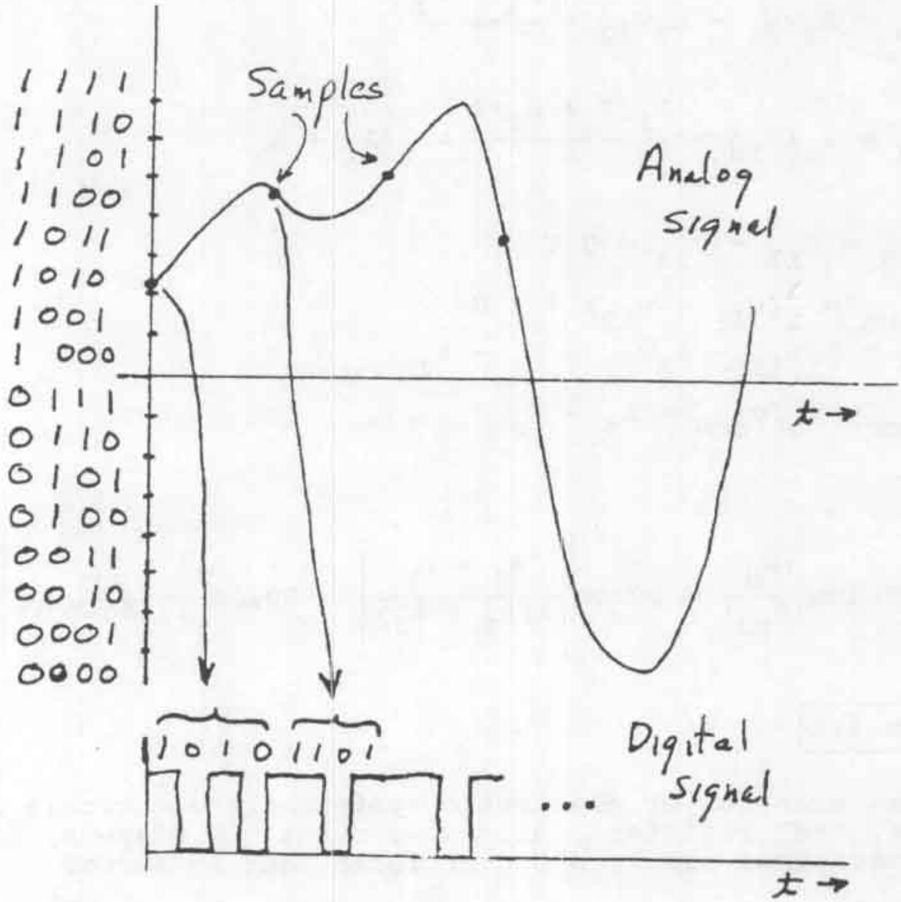
Electronic system blocks include amplifiers, filters, signal sources, wave-shaping circuits, digital logic functions, digital memories, power supplies, and converters.

Problem 1.3

Some electronic systems process information in electronic form and some power (hopefully as little as possible) is consumed. In power electronics, the power delivered to a load is the main concern.

Problem 1.4

Conversion of analog signals to digital form is a two-step process. First, the signal is sampled at periodic points in time. Second, each sample is approximately represented by a codeword.



Problem 1.5

Provided that it is not too large in amplitude, noise can be completely removed from a digital signal. Noise tends to accumulate in analog signals. Digital circuits tend to be easier than analog circuits to implement with integrated techniques. Thus extremely complex digital systems are feasible while equally complex analog systems are not. Digital systems are more adaptable than analog systems to a variety of uses.

Problem 1.6

Number of bits per second = $16 \times 44.1 \times 10^3$ = 705.6 kbit/s (for monaural) (1.411 Mbits/s are used for stereo.)

Number of amplitude zones = 2^{16} = 65,536

$$\Delta = \frac{5 - (-5)}{65536} = 152.6\ \mu V$$

Problem 1.7

Minimum sampling rate = $2f_H$ = 200 sample/s

$N = \frac{10\text{ mV}}{0.01\text{ mV}} = 1000$ which requires k = 10 at least ($2^{10} = 1024$)

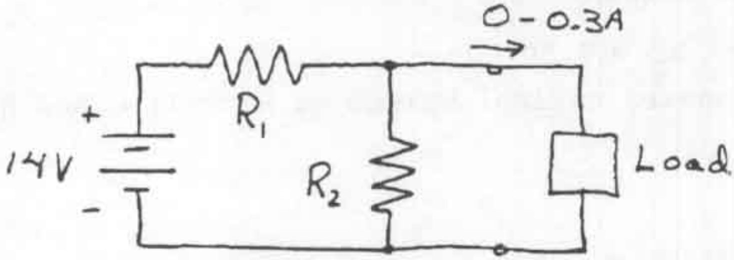
Number of bits per second = 200 × 10 = 2 kbit/s

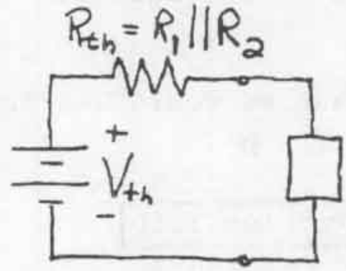
Problem 1.8

See Figure 1.6 in the book.

Problem 1.9

Because we are limited to resistors, the only option is a resistive voltage divider as shown below.





We denote the nominal values of the resistors as R_1 and R_2. The highest load voltage (at most 6 V) occurs when $I_L = 0$, when the resistor in parallel with the load has its highest value (which is $1.05R_2$), and when the resistor in series with the source has its lowest value (which is $0.95R_1$). To achieve the desired no-load voltage we need

$$14 \frac{1.05R_2}{0.95R_1 + 1.05R_2} = 6$$

Solving for R_2, we have

$$R_2 = 0.6786\ R_1 \qquad (1)$$

The smallest load voltage (at least 4 V) occurs with I_L = 0.3 and resistance values of $0.95R_2$ and $1.05R_1$. For these values, the Thévenin voltage is

$$V_{th} = 14 \frac{0.95\ R_2}{1.05R_1 + 0.95R_2}$$

and the load voltage is

$$V_L = 4 = V_{th} - R_{th}I_L$$

$$4 = 14 \frac{0.95\ R_2}{1.05R_1 + 0.95R_2} - 0.3 \frac{0.95(1.05)\ R_1R_2}{1.05R_1 + 0.95R_2} \qquad (2)$$

Using Equation (1) to substitute for R_2 in Equation (2) and solving we obtain:

$$R_1 = 11.06\ \Omega$$

Then from Equation (1) we obtain:

$$R_2 = 7.507\ \Omega$$

Thus we could use the standard nominal values of $R_1 = 11\ \Omega$ and $R_2 = 7.5\ \Omega$.

Problem 1.10

System engineers design the block diagrams of systems including specifications for each block. Circuit designers design the circuits for each block. Process engineers design the fabrication processes. Semiconductor physicists research fundamental processes used in electronic devices.

Problem 1.11

The components of integrated circuits and their interconnections are manufactured concurrently on a semiconductor wafer by a sequence of photolithographic processing steps. The components of a discrete circuit are manufactured separately and then interconnected, usually on a circuit board. Often overall cost can be reduced by integrating the system onto as few chips as possible because chip cost is nearly independent of complexity (within certain bounds).

Problem 1.12

The area consumed by each transistor is $(10\ \mu m) \times (10\ \mu m) = 10^{-10}\ m^2$. The chip area is $(2\ cm) \times (2\ cm) = 4 \times 10^{-4}\ m^2$. Thus the number of transistors that can be placed on the chip is

$$(4 \times 10^{-4})/(10^{-10}) = 4 \times 10^{6} \text{ transistors/chip}$$

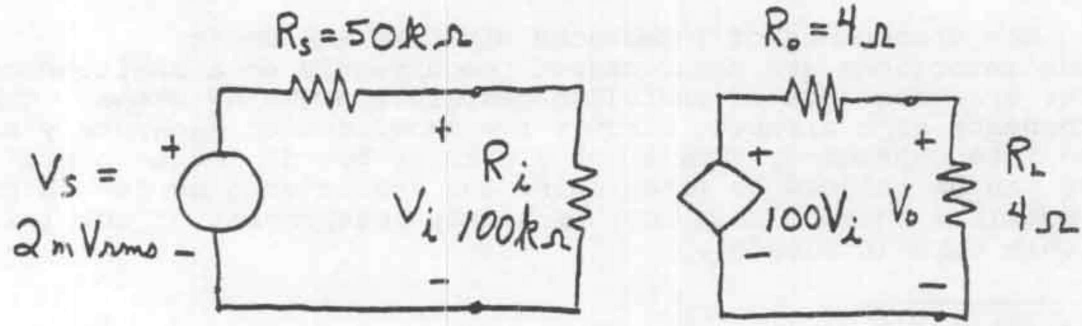
Problem 1.13

Gain is a negative number for an inverting amplifier, and the output signal is an inverted version of the input signal. Gain is a positive number for a noninverting amplifier, and the output signal has the same polarity as the input signal at each instant of time.

Problem 1.14

"Loading effects" refer to the fact that the input voltage of an amplifier is less than the internal source voltage because of the voltage drop across the internal source impedance. Also the amplifier output voltage is less than the open-circuit voltage gain times the input voltage because of the voltage drop across the output impedance of the amplifier.

Problem 1.15



$$A_v = \frac{V_o}{V_i} = A_{vo}\frac{R_L}{R_L + R_o} = 50$$

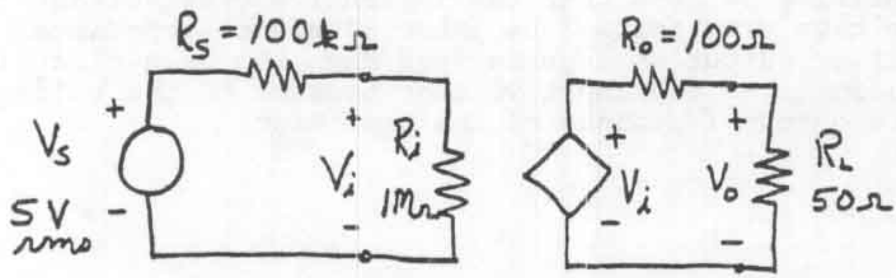
$$A_{vs} = \frac{V_o}{V_s} = A_{vo}\frac{R_L}{R_L + R_o}\frac{R_i}{R_i + R_s} = 33.3$$

$$A_i = A_v\frac{R_i}{R_L} = 1.25 \times 10^6$$

$$G = A_v A_i = 6.25 \times 10^7$$

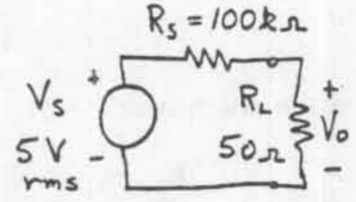
Problem 1.16

Using the unity-gain amplifier we have:



$$V_o = V_s\frac{R_i}{R_i + R_s}\frac{R_L}{R_L + R_o} = 1.52 \text{ V rms} \quad \text{and} \quad P_o = V_o^2/R_L = 45.9 \text{ mW}$$

With the source connected directly to the load, we have:



$$V_o = V_s \frac{R_L}{R_L + R_s} = 2.5 \text{ mV rms}$$

$$P_o = V_o^2/R_L = 125 \text{ nW}$$

Thus the output power is much larger if the unity-gain amplifier is used.

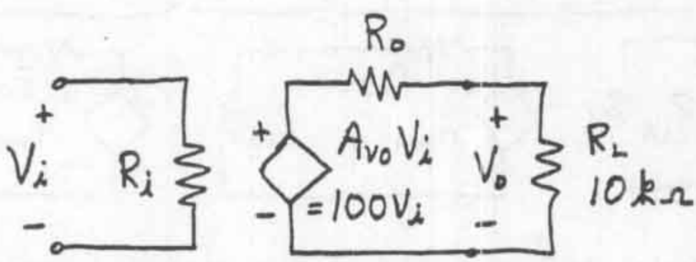
Problem 1.17

$$P_{in} = V_{in}^2/R_{in} = 0.333 \text{ pW}$$

$$P_o = V_o^2/R_L = 3.135 \text{ W}$$

$$G = P_o/P_{in} = 9.376 \times 10^{12}$$

Problem 1.18



$$A_v = 90 = A_{vo} \frac{R_L}{R_o + R_L} = 100 \frac{10^4}{R_o + 10^4}$$

Solving we find that $R_o = 1.11\ k\Omega$

Problem 1.19

With the switch open we have:

$$V_o = 50 \text{ mV} = V_s \frac{R_i}{R_i + 10^6} A_{vo} \frac{R_L}{R_L + R_o} \quad (1)$$

With the switch closed we have:

$$V_o = 100 \text{ mV} = V_s A_{vo} \frac{R_L}{R_L + R_o} \quad (2)$$

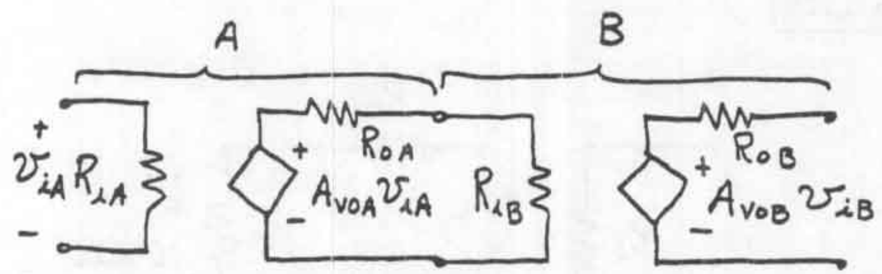
Dividing the respective sides of Equation (1) by those of Equation (2), we have:

$$\frac{50 \text{ mV}}{100 \text{ mV}} = \frac{R_i}{R_i + 10^6}$$

Solving we obtain $R_i = 1 \text{ M}\Omega$.

Problem 1.20

If we cascade two amplifiers A and B the equivalent circuit is:



The open-circuit voltage gain of the cascaded amplifier is:

$$A_{vo} = A_{voA} A_{voB} \frac{R_{iB}}{R_{oA} + R_{iB}}$$

Problem 1.21

See the figure shown in the solution for Problem 1.20. When the amplifiers are cascaded in the order A-B, we have:

$$R_i = R_{iA} = 3\ \text{k}\Omega$$

$$R_o = R_{oB} = 20\ \Omega$$

$$A_{vo} = A_{voA}A_{voB}\frac{R_{iB}}{R_{oA} + R_{iB}} = 4.998 \times 10^4$$

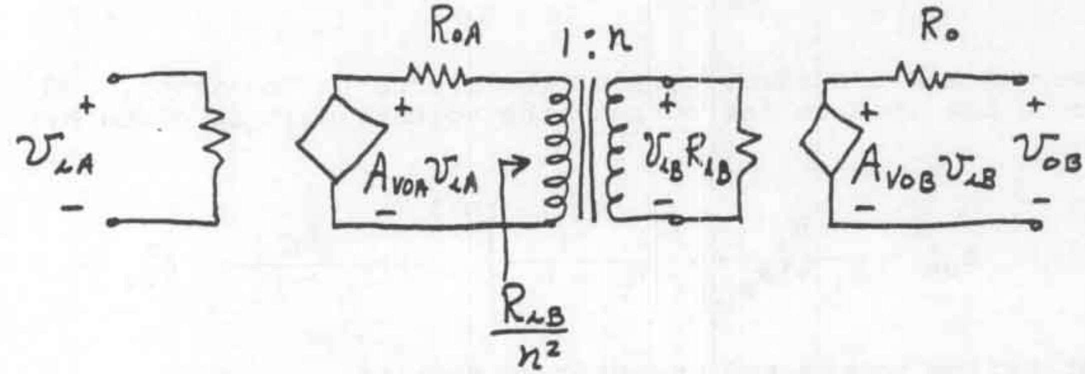
On the other hand for the B-A cascade we have:

$$R_i = R_{iB} = 1\ \text{M}\Omega$$

$$R_o = R_{oA} = 400\ \Omega$$

$$A_{vo} = A_{voA}A_{voB}\frac{R_{iA}}{R_{oB} + R_{iA}} = 4.967 \times 10^4$$

Problem 1.22



$$\left|A_{vo}\right| = \frac{v_{oB}}{v_{iA}} = \left|A_{voA}\right| \times \frac{R_{iB}/n^2}{R_{oA} + R_{iB}/n^2} \times n \times \left|A_{voB}\right|$$

$$\left|A_{vo}\right| = \left|A_{voA}\right| \times \left|A_{voB}\right| \times \frac{R_{iB}n}{n^2R_{oA} + R_{iB}}$$

$$\frac{d|A_{vo}|}{dn} = 0 = \left|A_{voA}\right| \times \left|A_{voB}\right| \times \frac{R_{iB}^2 - n^2 R_{oA} R_{iB}}{(n^2 R_{oA} + R_{iB})^2}$$

Solving for n we have:

$$n = \sqrt{\frac{R_{iB}}{R_{oA}}}$$

Problem 1.23

The internal source impedance is:

$$R_s = \frac{\text{open-circuit voltage}}{\text{short-circuit current}} = \frac{20 \times 10^{-3}}{10^{-6}} = 20 \text{ k}\Omega$$

The desired voltage gain is required to be at least:

$$A_{vs} = \frac{V_o}{V_s} = \frac{10}{20 \times 10^{-3}} = 500$$

If we cascade n stages, connect the source to the input, and connect the load to the output, the voltage gain is given by:

$$A_{vs} = \frac{R_i}{R_i + R_s} \times \left(\frac{R_i}{R_i + R_o}\right)^{n-1} \times \frac{R_L}{R_L + R_o} \times A_{vo}^n$$

Substituting values and reducing we obtain:

$$A_{vs} = 0.02381 \times (0.9091)^{n-1} \times (10)^n$$

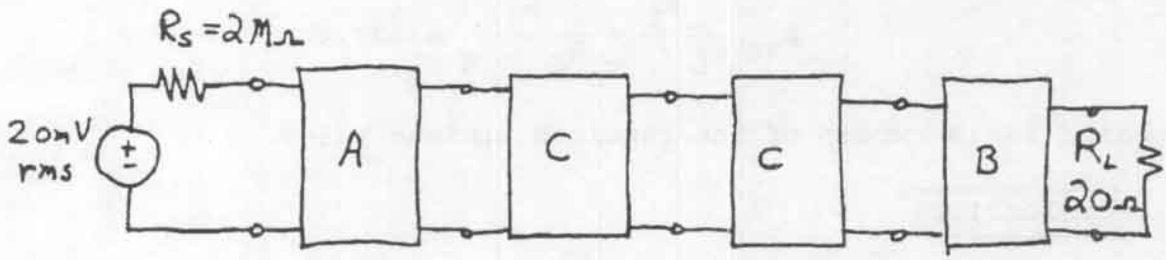
By trial and err we determine that we must have n = 5 to achieve A_{vs} in excess of 500.

Problem 1.24

To avoid excessive loading effects at the input, we should choose the first stage such that its input resistance is larger than the source resistance. Therefore we choose type A as the input stage. To avoid excessive loading effects at the output, we should choose the last stage such that its output impedance is much less than the load impedance. Therefore we choose type B as the output stage.

To achieve output power of 1 W we need $P_o = 1 = V_o^2/R_L$. Solving we determine that $V_o = 4.472$ V rms. Thus we require an overall gain of $A_{vs} = V_o/V_s = 4.472/(20 \times 10^{-3}) = 223.6$ as a minimum value.

To attain the required gain with the least number of stages we use intermediate stages of type C. Thus the amplifier diagram is:



The cascade has $R_i = 10$ MΩ, $R_o = 1$ Ω, and $A_{vo} = 376.9$. The resulting loaded gain is

$$A_{vo} \frac{R_L}{R_L + R_o} \frac{R_i}{R_i + R_s} = 299.1$$

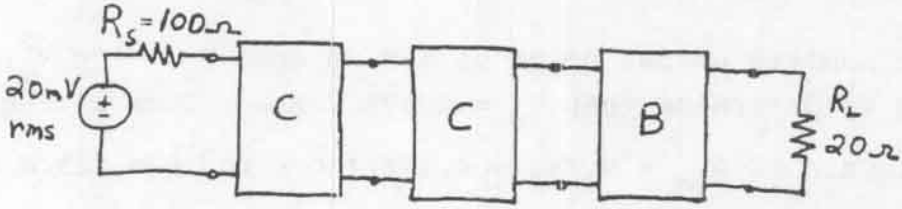
which is in excess of the required minimum value.

Problem 1.25

The source impedance is lower than the input impedances of any of the stage types. Therefore we choose type C as the input stage to achieve the highest gain. To avoid excessive loading effects at the output, we should choose the last stage such that its output impedance in much less than the load impedance. Therefore we choose type B as the output stage.

To achieve output power of 1 W we need $P_o = 1 = V_o^2/R_L$. Solving we determine that $V_o = 4.472$ V rms. Thus we require an overall gain of $A_{vs} = V_o/V_s = 4.472/(20 \times 10^{-3}) = 223.6$ as a minimum value.

To attain the required gain with the least number of stages we use intermediate stages of type C. Thus the amplifier diagram is:



The cascade has $R_i = 20\ \text{k}\Omega$, $R_o = 1\ \Omega$, and $A_{vo} = 452.2$. The resulting loaded gain is

$$A_{vo} \frac{R_L}{R_L + R_o} \frac{R_i}{R_i + R_s} = 428.6$$

which is in excess of the required minimum value.

Problem 1.26

The efficiency η of an amplifier is the output power divided by the supply power times 100%.

$$\eta = \frac{P_{out}}{P_{supply}} \times 100\%$$

Dissipated power is the power converted to heat.

Problem 1.27

$$P_{in} = V_{in}^2/R_{in} = (0.1)^2/10^5 = 0.1\ \mu\text{W}$$

$$P_{out} = V_o^2/R_L = (10)^2/8 = 12.5\ \text{W}$$

$$P_{supply} = V_{CC}I_{CC} = 15 \times 2 = 30\ \text{W}$$

$$P_{dissipated} = P_{supply} + P_{in} - P_o = 17.5\ \text{W}$$

$$\eta = \frac{P_{out}}{P_{supply}} \times 100\% = \frac{12.5}{30} \times 100\% = 41.67\%$$

Problem 1.28

Power is delivered to the amplifier by both of the 15-V sources. Part of this power is returned to the 5-V source. The net power supplied is

$$P_{supply} = 15 \times 1 + 15 \times 2 - 5 \times 1 = 40 \text{ W}$$

Problem 1.29

$$I_{1avg} = \frac{1}{T}\int_0^T i_1^2(t)\,dt = \frac{1}{0.01}\int_0^{0.005} 2.5\sin(200\pi t)\,dt =$$

$$\frac{250}{200\pi}\left[-\cos(200\pi t)\right]_0^{0.005} = \frac{500}{200\pi} = 0.7958 \text{ A}$$

Similarly $I_{2avg} = 0.7958$ A.

$$P_{out} = \frac{V_{o,rms}^2}{R_L} = \frac{20/\sqrt{2}}{8} = 25 \text{ W}$$

$$P_{supply} = (25 \text{ V}) \times I_{iavg} + (25 \text{ V}) \times I_{2avg} = 39.79 \text{ W}$$

$$\eta = \frac{P_{out}}{P_{supply}} \times 100\% = 62.83\%$$

Problem 1.30

$$G_{dB} = 10\log(G)$$

$$A_{vdB} = 20\log|A_v|$$

Problem 1.31

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{10 \text{ mV}}{1\ \mu\text{A}} = 10 \text{ k}\Omega$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{5 \text{ V}}{10 \text{ mV}} = 500 \qquad A_{vdB} = 20\log(A_v) = 53.98 \text{ dB}$$

$$A_i = A_v \frac{R_{in}}{R_L} = 500 \frac{10\ k\Omega}{10\ \Omega} = 5 \times 10^5 \qquad A_{idB} = 20\log(A_i) = 113.98\ dB$$

$$G = A_v A_i = 250 \times 10^6 \qquad G_{db} = 10\log(G) = 83.98\ dB$$

Problem 1.32

$$A_i = A_v \frac{R_{in}}{R_L} = 1 \times \frac{10^5}{8} = 12.5 \times 10^3 \qquad A_{idB} = 20\log(A_i) = 81.94\ dB$$

$$G = A_v A_i = 12.5 \times 10^3 \qquad G_{db} = 10\log(G) = 40.97\ dB$$

Problem 1.33

$$G_{db} = 10\log(A_v A_i) = 10\log A_v + 10\log A_i = \frac{A_{vdB} + A_{idB}}{2} = 50\ dB$$

$$A_v = 10^{30/20} = 31.62 \qquad A_i = 10^{70/20} = 3162$$

$$A_i = 3162 = A_v \frac{R_i}{R_L} = 31.62 \frac{100\ k\Omega}{R_L} \quad \Rightarrow \quad R_L = 1\ k\Omega$$

Problem 1.34

(a) $10\ dbV = 20\log\frac{V_a}{1\ V} \quad \Rightarrow \quad V_a = 10^{0.5} = 3.162\ V$

(b) $-30\ dbV = 20\log\frac{V_b}{1\ V} \quad \Rightarrow \quad V_b = 10^{-1.5} = 31.62\ mV$

(c) $10\ dbmV = 20\log\frac{V_c}{1\ mV} \quad \Rightarrow \quad V_c = (1\ mV) \times 10^{0.5} = 3.162\ mV$

(d) $20\ dBW = 10\log\frac{P}{1\ W} \quad \Rightarrow \quad P = 10^2 = \frac{V_d^2}{50} \quad \Rightarrow \quad V_d = 70.71\ V$

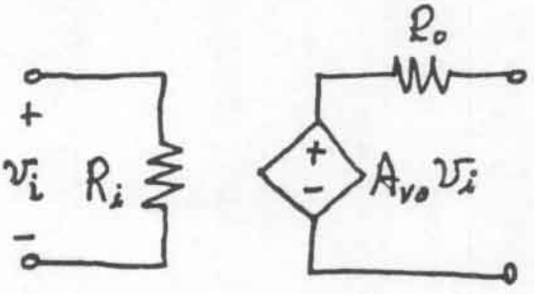
Problem 1.35

(a) $20\text{ dBm} = 10\log\frac{P_a}{1\text{ mW}} \quad \Rightarrow \quad P_a = (1\text{ mW}) \times 10^2 = 100\text{ mW}$

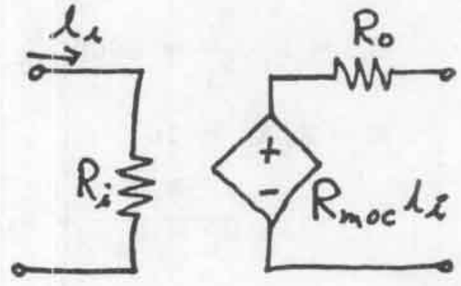
(b) $-60\text{ dBW} = 10\log\frac{P_b}{1\text{ W}} \quad \Rightarrow \quad P_b = (1\text{ W}) \times 10^{-6} = 1\ \mu\text{W}$

(c) $10\text{ dBW} = 10\log\frac{P_c}{1\text{ W}} \quad \Rightarrow \quad P_c = (1\text{ W}) \times 10^{1} = 10\text{ W}$

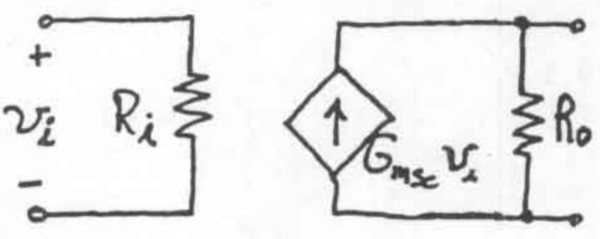
Problem 1.36



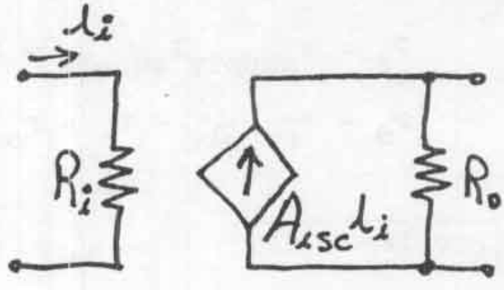
Voltage amplifier



Transresistance amplifier



Transconductance amplifier

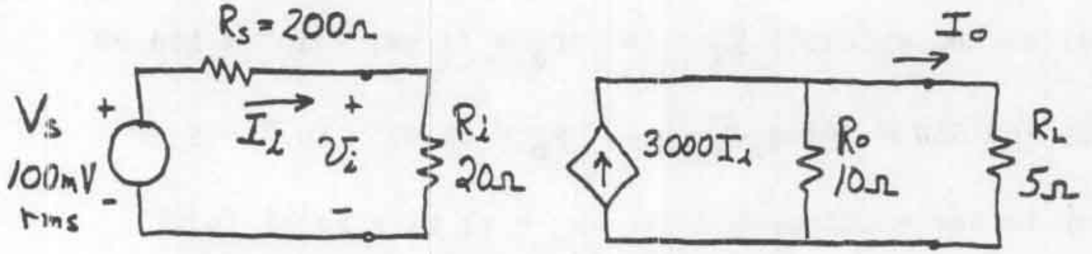


Current amplifier

A_{vo} and R_{moc} are measured with the output open circuited.

G_{msc} and A_{isc} are measured with the output short circuited.

Problem 1.37



$$A_i = \frac{I_o}{I_i} = A_{isc} \frac{R_o}{R_o + R_L} = 3000 \frac{10}{10 + 5} = 2000$$

$$A_v = A_i \frac{R_L}{R_i} = 2000 \frac{5}{20} = 500$$

$$G = A_v A_i = 10^6$$

$$V_i = V_s \frac{R_i}{R_s + R_i} = 9.091 \text{ mV}$$

$$P_i = \frac{V_i^2}{R_i} = 4.13 \ \mu\text{W}$$

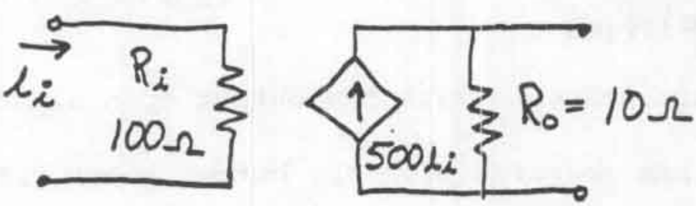
$$P_o = GP_i = 4.13 \text{ W}$$

$$P_s = V_{supply} I_{supply} = 24 \text{ W}$$

$$P_d = P_{supply} + P_i - P_o = 19.9 \text{ W}$$

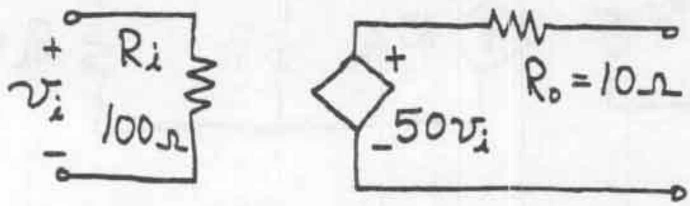
Problem 1.38

The current amplifier model is:



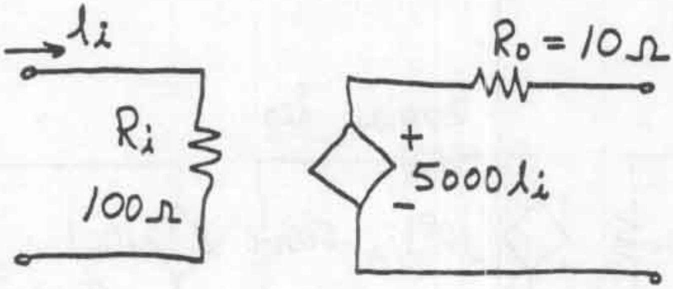
(a) Voltage amplifier model:

$$A_{vo} = \frac{v_{ooc}}{v_i} = \frac{500 i_i R_o}{R_i i_i} = 50$$



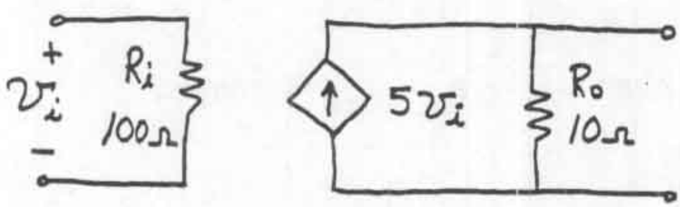
(b) Transresistance amplifier model:

$$R_{moc} = \frac{v_{ooc}}{i_i} = \frac{500 i_i R_o}{i_i} = 5\ \text{k}\Omega$$

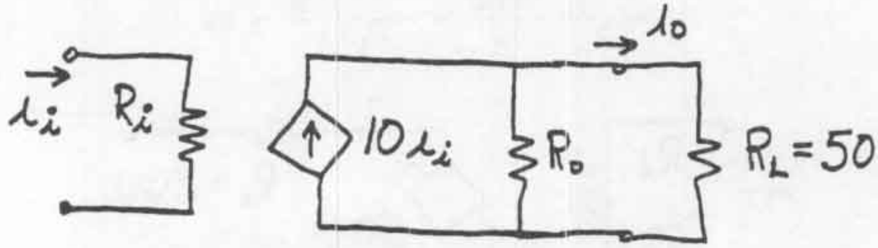


(c) Transconductance amplifier model:

$$G_{msc} = \frac{i_{osc}}{v_i} = \frac{500 i_i}{R_i i_i} = 5\ \text{S}$$



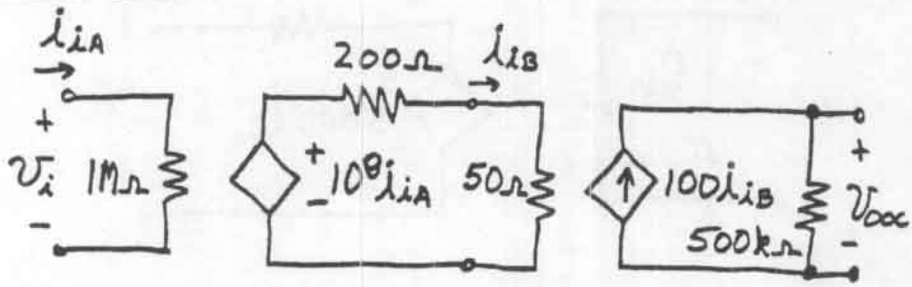
Problem 1.39



$$A_i = A_{isc} \frac{R_o}{R_o + R_L}$$

$$8 = 10 \frac{R_o}{R_o + 50} \quad \Rightarrow \quad R_o = 200\ \Omega$$

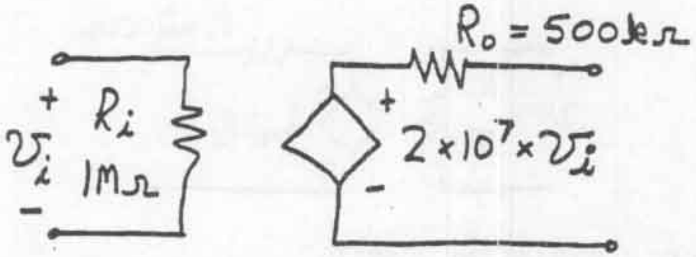
Problem 1.40



Voltage amplifier model:

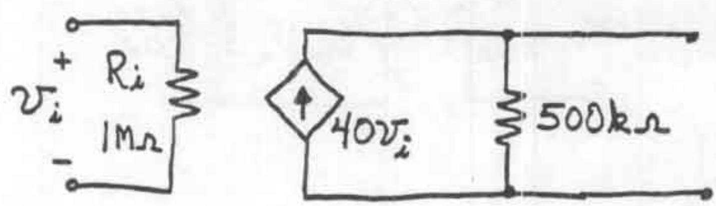
$$A_{vo} = \frac{v_{ooc}}{v_i} = \frac{500 \times 10^3 \times 100 \times \dfrac{10^8 i_{iA}}{200 + 50}}{10^6 i_{iA}} = 2 \times 10^7$$

$$R_i = R_{iA} = 1\ \text{M}\Omega \qquad R_o = R_{oB} = 500\ \text{k}\Omega$$

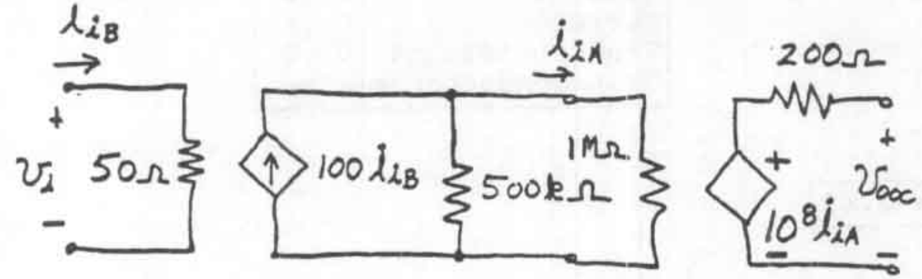


Transconductance amplifier model:

$$G_{msc} = \frac{i_{osc}}{v_i} = \frac{A_{vo}v_i/R_o}{v_i} = \frac{A_{vo}}{R_o} = 40\ S$$



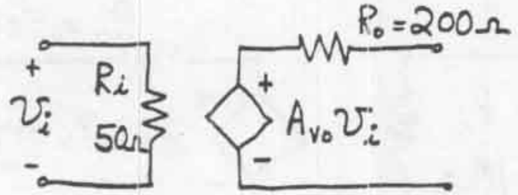
Problem 1.41



Voltage amplifier model:

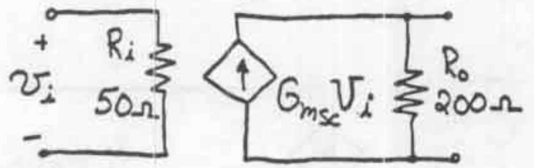
$$A_{vo} = \frac{v_{ooc}}{v_i} = \frac{10^8\ \dfrac{500\ k\Omega}{1\ M\Omega + 500\ k\Omega}\ 100\ i_{iB}}{50 i_{iB}} = 6.667 \times 10^7$$

$R_i = R_{iB} = 50\ \Omega$ $\qquad$ $R_o = R_{oA} = 200\ \Omega$



Transconductance amplifier model:

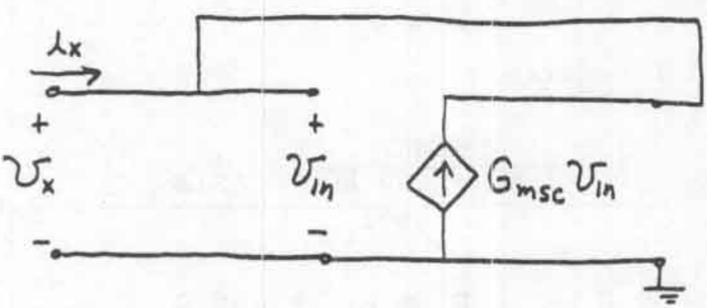
$$G_{msc} = \frac{i_{osc}}{v_i} = \frac{A_{vo}v_i/R_o}{v_i} = \frac{A_{vo}}{R_o} = 333.3 \times 10^3 \text{ S}$$



Problem 1.42

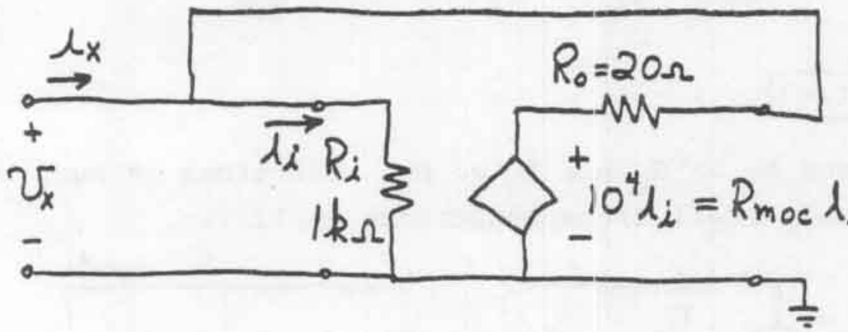
Amplifier type	R_i	R_o
Voltage	∞	0
Current	0	∞
Transresistance	0	0
Transconductance	∞	∞

Problem 1.43



$$R_x = \frac{v_x}{i_x} = \frac{v_{in}}{-G_{msc}v_{in}} = -\frac{1}{G_{msc}} = -10\ \Omega$$

Problem 1.44



From the circuit we can write:

$$i_i = \frac{v_x}{R_i} \qquad (1)$$

$$i_x = i_i + \frac{v_x - R_{moc} i_i}{R_o} \qquad (2)$$

Then using Equation (1) to substitute for i_i in Equation (2) and solving, we obtain:

$$R_x = \frac{v_x}{i_x} = \frac{1}{\frac{1}{R_i} + \frac{1}{R_o} - \frac{R_{moc}}{R_i R_o}} = -2.23\ \Omega$$

Problem 1.45

We have $R_i << R_s$ and $R_o << R_L$. Therefore we have a nearly ideal transresistance amplifier. Then as in Example 1.7, we have

$$R_{moc} = \frac{v_o}{i_i} = \frac{v_o}{v_i/R_i} = A_{vo}R_i = 10 \times (1\ \Omega) = 10\ \Omega$$

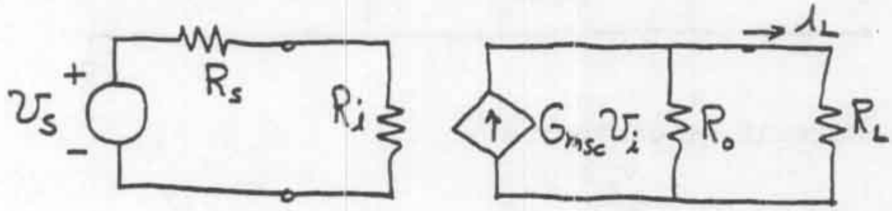
Problem 1.46

We have $R_i >> R_s$ and $R_o >> R_L$. Therefore we have a nearly ideal transconductance amplifier. Then as in Example 1.6, we have:

$$G_{msc} = \frac{i_o}{v_i} = \frac{v_o/R_o}{v_i} = \frac{A_{vo}}{R_o} = \frac{100}{10^6} = 10^{-4}\ \text{S}$$

Problem 1.47

We need $R_i >> R_s$ and $R_o >> R_L$. Therefore we must have an approximately ideal transconductance amplifier.



$$i_L = \frac{R_i}{R_i + R_s}\frac{R_o}{R_o + R_L}G_{msc}v_s$$

For a 1% change in i_L when R_s increases from 1 kΩ to 2 kΩ, we must have

$$0.99 \times \frac{R_i}{R_i + 1000} = \frac{R_i}{R_i + 2000}$$

Solving we find that R_i = 98 kΩ.

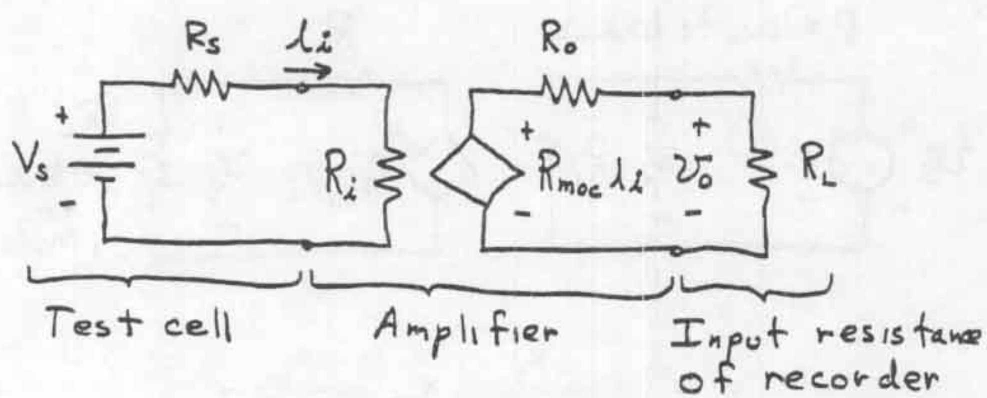
For a 1% change in i_L when R_L increases from 100 Ω to 300 Ω, we must have

$$0.99 \times \frac{R_o}{R_o + 100} = \frac{R_o}{R_o + 300}$$

Solving we find that R_o = 19.7 kΩ.

Problem 1.48

We need R_i < 10 Ω, R_o << 10 kΩ and a transresistance gain of R_{moc} = (1 V)/(1 mA) = 1000 Ω. Therefore we must have an approximately ideal transresistance amplifier.



To achieve approximately ±3% accuracy we will allow ±1% each for load resistance variations, amplifier gain variations, and strip chart recorder gain variations.

Allowing for a 1% increase in v_o as R_L increases from 10 kΩ to an open circuit, we require

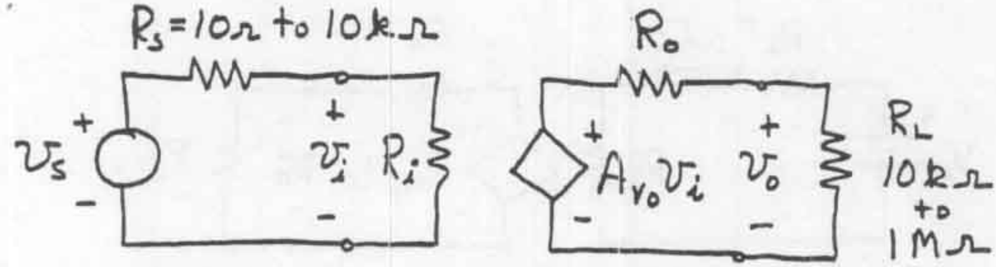
$$\frac{10\ k\Omega}{R_o + 10\ k\Omega} = 0.99$$

Solving we find that R_o = 101 Ω, therefore we specify an amplifier with

$$R_{moc} = 1000\ \Omega \pm 1\%$$
$$R_i < 10\ \Omega$$
$$R_o \leq 101\ \Omega$$

Problem 1.49

We need an amplifier with high input resistance, low output resistance, and a voltage gain of 10. Thus a nearly ideal voltage amplifier is needed. Let us allow for ±1% variations in the output voltage due to changes in source resistance, in amplifier gain, and in load resistance. The equivalent circuit for the system is:



$$v_o = v_s \frac{R_i}{R_i + R_s} A_{vo} \frac{R_L}{R_o + R_L}$$

Allowing a 1% change in v_o when R_s changes from 10 Ω to 10 kΩ, we require:

$$0.99 \frac{R_i}{R_i + 10} = \frac{R_i}{R_i + 10^4} \quad \Rightarrow \quad R_i = 9.89 \times 10^5$$

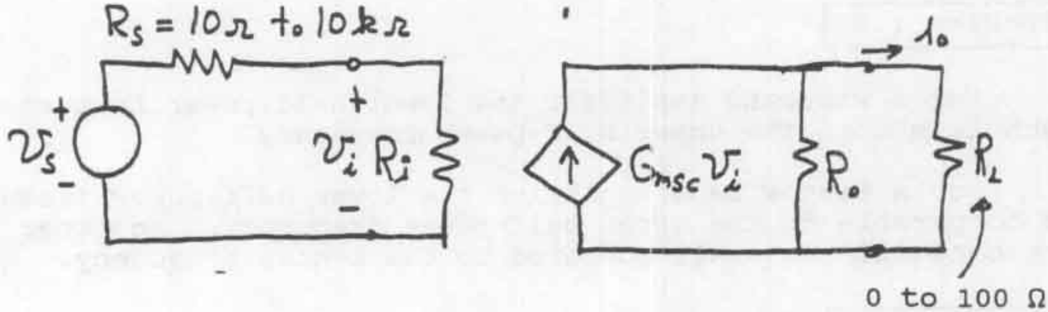
Allowing a 1% change in v_o when R_s changes from 1 MΩ to 10 kΩ, we require:

$$0.99 \frac{10^6}{R_o + 10^6} = \frac{10^4}{R_o + 10^4} \quad \Rightarrow \quad R_o = 102\ \Omega$$

Thus we specify an amplifier having A_{vo} = 10 ± 1%, R_i > 989 kΩ, and R_o < 102 Ω.

Problem 1.50

We need an amplifier with high input resistance, high output resistance, and a gain of G_m = (1 mA)/(0.1 V) = 10^{-2} S. The sensitivity of the recorder varies by ±1%. Therefore to achieve an overall accuracy of ±3%, let us allow ±0.667% each for variations in R_s, R_L, and amplifier gain. A nearly ideal transconductance amplifier is needed. The system diagram is:



$$i_o = v_s \frac{R_i}{R_i + R_s} G_{msc} \frac{R_o}{R_o + R_L}$$

Allowing for a 0.667% change in i_o when R_s changes from 10 Ω to 10 kΩ, we require:

$$0.9933 \frac{R_i}{R_i + 10} = \frac{R_i}{R_i + 10^4} \quad \Rightarrow \quad R_i = 1.49 \text{ M}\Omega$$

Allowing for a 0.667% change in i_o when R_s changes from 0 to 100 Ω, we require:

$$0.9933 \frac{R_o}{R_o + 0} = \frac{R_o}{R_o + 100} \quad \Rightarrow \quad R_o = 14.9 \text{ k}\Omega$$

Thus we need an amplifier with $G_{msc} = 10^{-2}$ S ± 0.667%, $R_i >$ 1.49 MΩ, and $R_o >$ 14.9 kΩ.

Problem 1.51

Any signal is the summation of sine waves of various frequencies, amplitudes, and phases. The spectrum of a signal is a plot of the amplitudes of these components versus frequency. By knowing the range of frequencies with significant amplitudes, we can specify the required frequency response for an amplifier that can amplify the signal without significant distortion.

Problem 1.52

See Figure 1.36 in the book.

Problem 1.53

For a wideband amplifier the lower half-power frequency is much less than the upper half-power frequency.

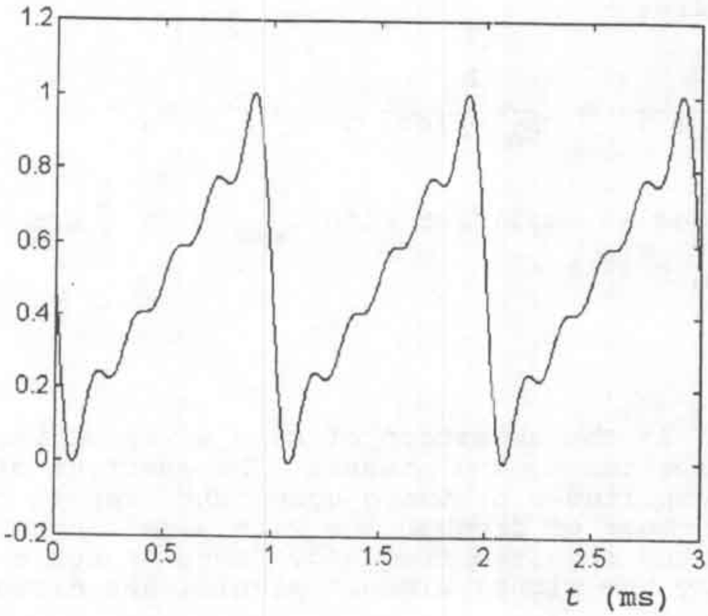
For a narrow band amplifier the lower half-power frequency is comparable to the upper half-power frequency. In other words the bandwidth is small compared to the center frequency.

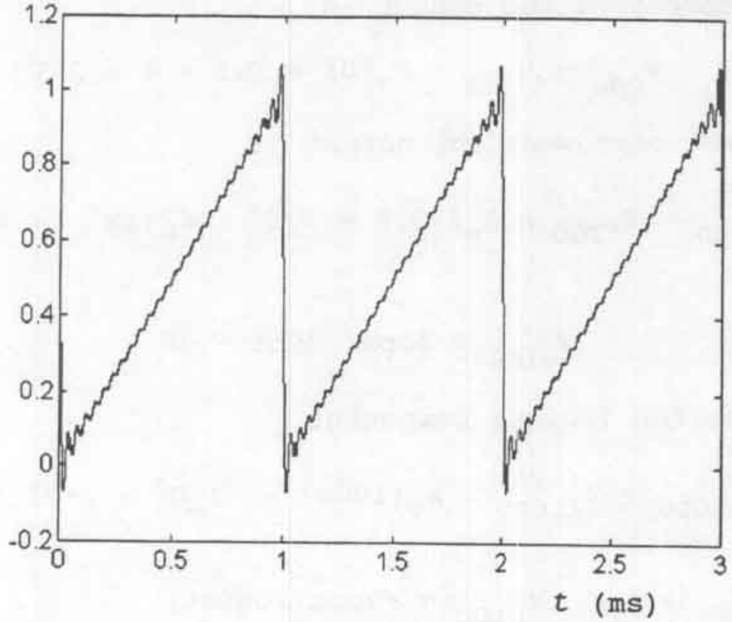
Problem 1.54

Various programs can be used. A MATLAB file that will produce the plot for 25 terms (including the constant) is:

```
t = 0:3e-7:3e-3;
vt = 0.5;
for n = 1:24       %change to n = 1:4 for five terms
vt = vt - sin(2000*n*pi*t)/(n*pi);
end
plot(t,vt)
```

The resulting plots are:





Problem 1.55

The phasor for the input signal is $\mathbf{V}_i = 0.1\angle 30^\circ$. The output can be written as a cosine function:

$$v_o(t) = 10\sin(2000\pi t + 15^\circ) = 10\cos(2000\pi t - 75^\circ)$$

Thus the phasor for the output is $\mathbf{V}_o = 10\angle -75^\circ$. The complex voltage gain is the output phasor divided by the input phasor.

$$A_v = \frac{\mathbf{V}_o}{\mathbf{V}_i} = \frac{10\angle -75^\circ}{0.10\angle 30^\circ} = 100\angle -105^\circ$$

$$A_{vdB} = 20\log|A_v| = 20\log(100) = 40 \text{ dB}$$

Problem 1.56

The input signal has three components: one with a frequency of 0 (dc), one with a frequency of 100 Hz, and one with a frequency of 1000 Hz. From Figure P1.56 we have $A_v(0) = 4$, $A_v(100) = 4\angle -18^\circ$, and $A_v(1000) = 2\angle 180^\circ = -2$.

For the dc component the output is:

$$v_{odc} = v_{idc} \times A_v(0) = 0.5 \times 4 = 2\ V$$

For the 100-Hz component the output is

$$\mathbf{V}_{o100} = \mathbf{V}_{i100} \times A_v(100) = 1\angle 0^\circ \times 4\angle -18^\circ = 4\angle -18^\circ$$

Thus

$$v_{o100} = 4\cos(200\pi t - 18^\circ)$$

Similarly for the 1000-Hz component

$$\mathbf{V}_{o1000} = \mathbf{V}_{i1000} \times A_v(1000) = 1\angle 0^\circ \times (-2) = -2$$

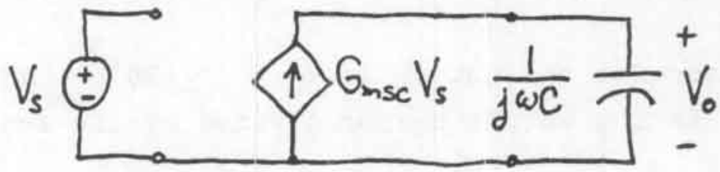
Thus

$$v_{o100} = -2\cos(2000\pi t)$$

The output voltage is the sum of its components:

$$v_o(t) = 2 + 4\cos(200\pi t - 18^\circ) - 2\cos(2000\pi t)$$

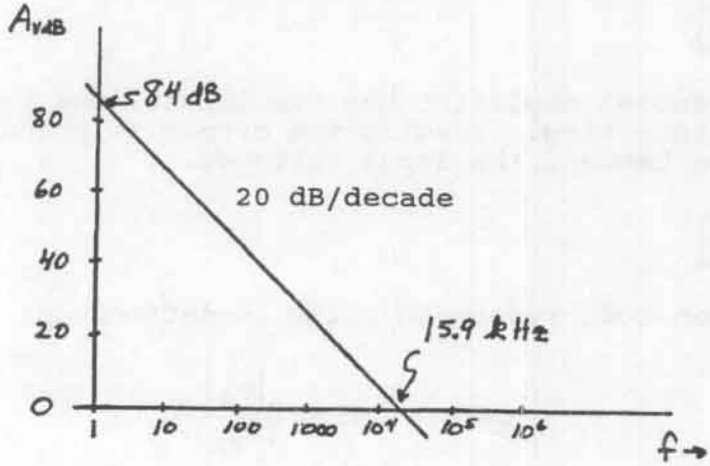
Problem 1.57



$$\mathbf{V}_o = G_{msc}\mathbf{V}_s \times \frac{-j}{\omega C}$$

$$A_v = \frac{\mathbf{V}_o}{\mathbf{V}_s} = -j\ \frac{G_{msc}}{\omega C} = -j\ \frac{10^{-3}}{2\pi f 10^{-8}} = -j\ \frac{15.9 \times 10^3}{f}$$

$$A_{vdB} = 20\log|A_v| = 20\log\left(\frac{15.9 \times 10^3}{f}\right) = 84.0 - 20\log(f)$$



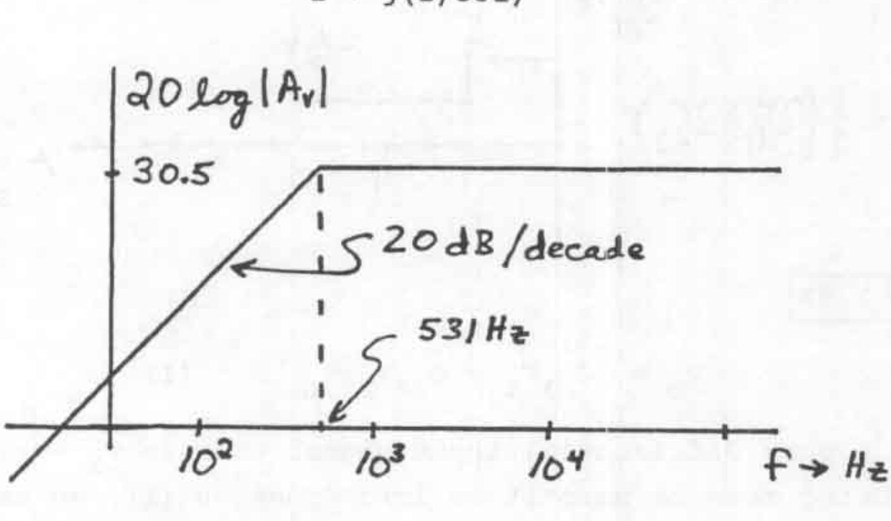
Problem 1.58

We ignore the dc source because the capacitor is an open circuit at dc.

$$A_v = \frac{R_i}{R_i + R_m - j/(\omega C)} \times 100 \times \frac{R_L}{R_o + R_L}$$

$$A_v = \frac{j\omega R_i C}{1 + j\omega(R_i + R_m)C} \times 100 \times \frac{R_L}{R_o + R_L}$$

$$A_v = 62.83 \times 10^{-3} \times \frac{jf}{1 + j(f/531)}$$



Problem 1.59

A differential amplifier has two inputs, one inverting and the other noninverting. Ideally the output is proportional to the difference between the input voltages.

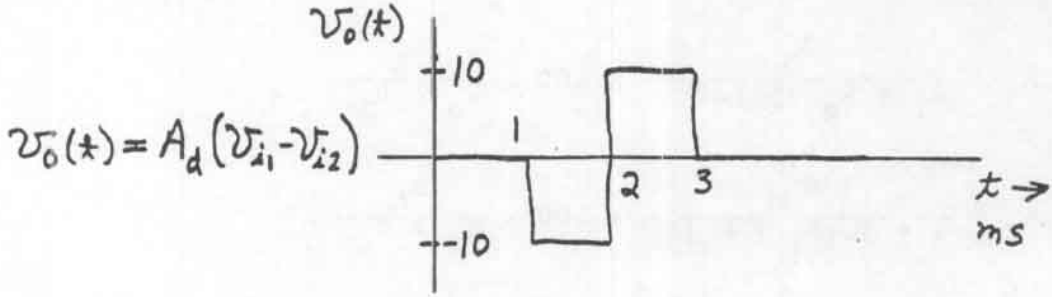
Problem 1.60

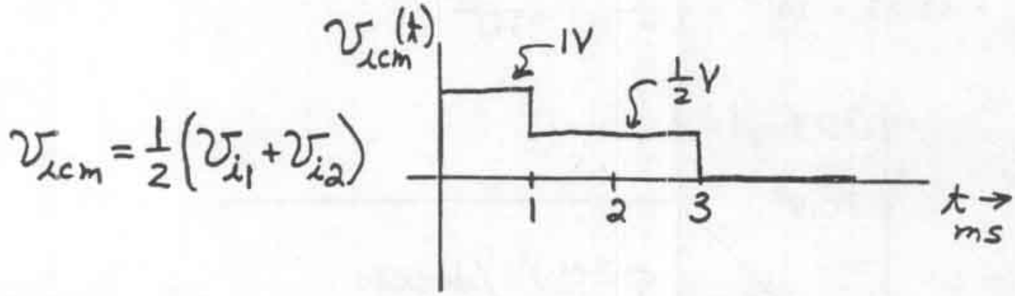
The common-mode rejection ratio is defined as:

$$\text{CMRR} = 20\log\frac{|A_d|}{|A_{cm}|}$$

in which A_d is the gain for the differential component and A_{cm} is the gain for the common-mode signal.

Problem 1.61





Problem 1.62

(a) $$v_o = (G_{m1}v_1 - G_{m2}v_2)R_L \qquad (1)$$

For a pure differential input signal we have $v_1 = -v_2 = v_{id}/2$. Using this to substitute into Equation (1), we have

$$v_{od} = (G_{m1}v_{id}/2 + G_{m2}v_{id}/2)R_L$$

and the differential gain is

$$A_d = \frac{v_{od}}{v_{id}} = \frac{1}{2}(G_{m1} + G_{m2})R_L$$

For a pure common mode input signal we have $v_1 = v_2 = v_{icm}$. Using this to substitute into Equation (1), we have

$$v_{ocm} = (G_{m1}v_{icm} - G_{m2}v_{icm})R_L$$

and the common-mode gain is

$$A_{cm} = \frac{v_{ocm}}{v_{icm}} = (G_{m1} - G_{m2})R_L$$

(b)

$$A_d = \frac{1}{2}(G_{m1} + G_{m2})R_L = 10$$

$$A_{cm} = \frac{1}{2}(G_{m1} + G_{m2})R_L = 0$$

$$\text{CMRR} = 20\log\frac{|A_d|}{|A_{cm}|} = \infty$$

(c)

$$A_d = \frac{1}{2}(G_{m1} + G_{m2})R_L = 9.95$$

$$A_{cm} = \frac{1}{2}(G_{m1} + G_{m2})R_L = 0.1$$

$$\text{CMRR} = 20\log\frac{|A_d|}{|A_{cm}|} = 40\text{ dB}$$

Problem 1.63

$$v_o = A_1v_1 - A_2v_2 \qquad (1)$$

For a pure differential input signal we have $v_1 = -v_2 = v_{id}/2$. Using this to substitute into Equation (1), we have

$$v_{od} = A_1v_{id}/2 + A_2v_{id}/2$$

and the differential gain is

$$A_d = \frac{v_{od}}{v_{id}} = \frac{1}{2}(A_1 + A_2)$$

For a pure common-mode input signal, we have $v_1 = v_2 = v_{icm}$. Using this to substitute into Equation (1), we have

$$v_{ocm} = A_1 v_{icm} - A_2 v_{icm}$$

and the common-mode gain is

$$A_{cm} = \frac{v_{ocm}}{v_{icm}} = A_1 - A_2$$

$$\text{CMRR} = 20\log\frac{|A_d|}{|A_{cm}|} = 20\log\frac{|A_1 + A_2|}{2|A_1 - A_2|}$$

$$\text{CMRR} = 20\log\frac{1000 + 999}{2(1000 - 999)} = 60 \text{ dB}$$

Problem 1.64

With the input terminals connected together we have a pure common-mode input signal. Thus the common-mode gain is

$$A_{cm} = \frac{v_{ocm}}{v_{icm}} = \frac{20 \text{ mV}}{10 \text{ mV}} = 2$$

$$\text{CMRR} = 20\log\frac{|A_d|}{|A_{cm}|} = 20\log\frac{500}{2} = 48 \text{ dB}$$

Problem 1.65

The differential output is

$$V_{od} = A_d V_{id} = A_d \times (20 \text{ mV}) \qquad (1)$$

The common-mode output is

$$V_{ocm} = A_{cm}V_{icm} = A_{cm} \times (5\ V) \qquad (2)$$

The common-mode output is required to be 60 dB less than the differential output:

$$60\ dB = 20\log\frac{V_{od}}{V_{ocm}} \qquad (3)$$

Using Equations (1) and (2) to substitute into Equation (3), we have

$$60 = 20\ \log\frac{A_d \times (20\ mV)}{A_{cm} \times (5\ V)}$$

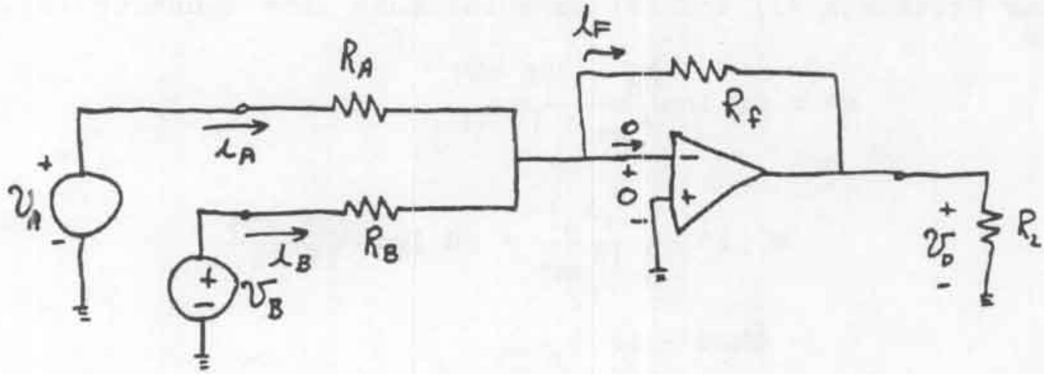
$$= 20\log\frac{|A_d|}{|A_{cm}|} + 20\ \log\frac{(20\ mV)}{(5\ V)}$$

$$= CMRR - 48$$

$$CMRR = 108\ dB$$

Chapter 2

Exercise 2.1



(a) $i_A = \frac{v_A}{R_A}$ $\quad i_B = \frac{v_B}{R_B}$ $\quad i_f = i_A + i_B = \frac{v_A}{R_A} + \frac{v_B}{R_B}$

$$v_o = -R_f i_f = -\left(\frac{R_f}{R_A} v_A + \frac{R_f}{R_B} v_B\right)$$

(b) For the v_A source:

$$R_{inA} = \frac{v_A}{i_A} = R_A$$

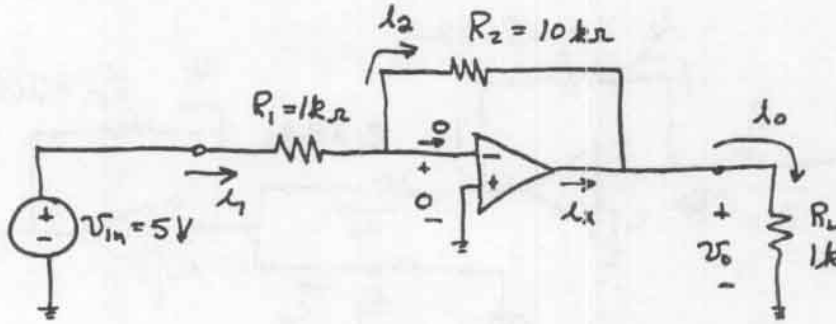
(c) for the v_B source:

$$R_{inB} = \frac{v_B}{i_B} = R_B$$

(d) Because v_o is independent of R_L, the output of the amplifier behaves as an ideal voltage source. Thus the output resistance is zero.

Exercise 2.2

(a)

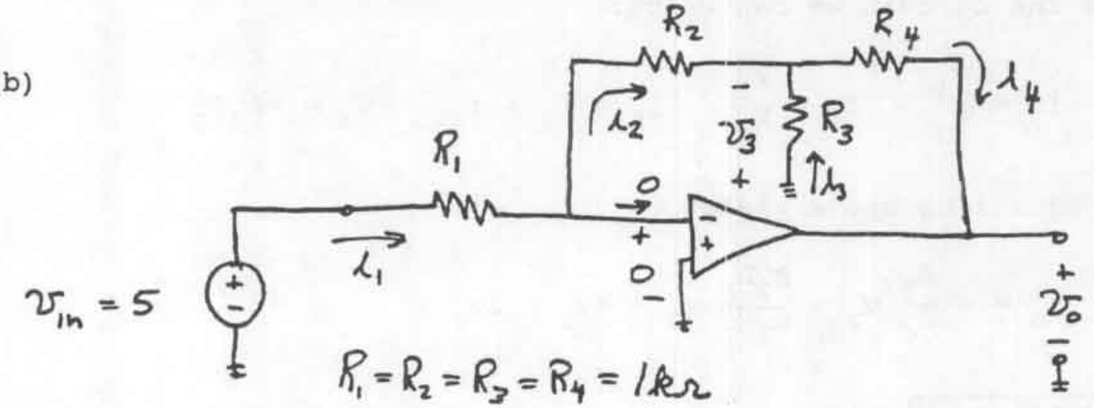


$$i_1 = \frac{v_{in}}{R_1} = 5 \text{ mA} \qquad i_2 = i_1 = 5 \text{ mA}$$

$$v_o = -R_2 i_2 = -50 \text{ V} \qquad i_o = \frac{v_o}{R_L} = -50 \text{ mA}$$

$$i_x = i_o - i_2 = -55 \text{ mA}$$

(b)

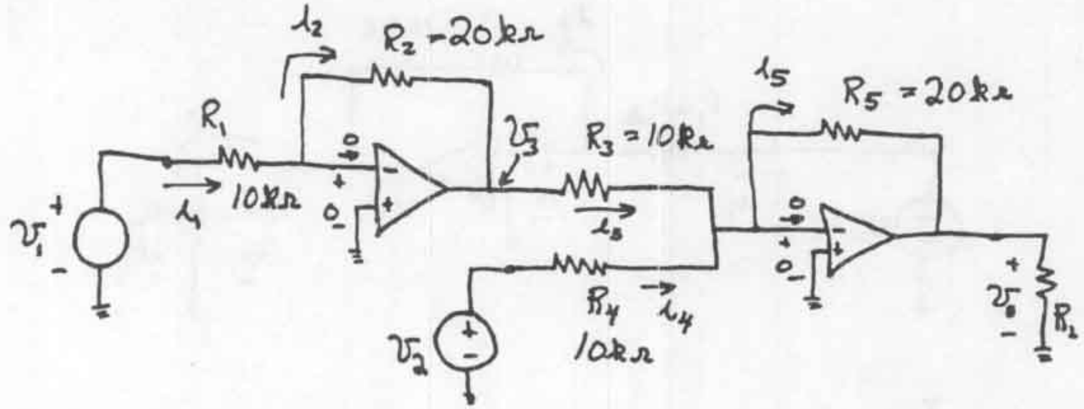


$$i_1 = \frac{v_{in}}{R_1} = 5 \text{ mA} \qquad i_2 = i_1 = 5 \text{ mA} \qquad v_3 = R_2 i_2 = 5 \text{ V}$$

$$i_3 = \frac{v_3}{R_3} = 5 \text{ mA} \qquad i_4 = i_2 + i_3 = 10 \text{ mA}$$

$$v_o = -R_4 i_4 - v_3 = -15 \text{ V}$$

Exercise 2.3



From the circuit we can write:

$$i_1 = \frac{v_1}{R_1} \qquad i_2 = i_1 \qquad v_3 = -R_2 i_2$$

The equations above yield: $v_3 = -\frac{R_2}{R_1} v_1 = -2v_1$

From the circuit we can write:

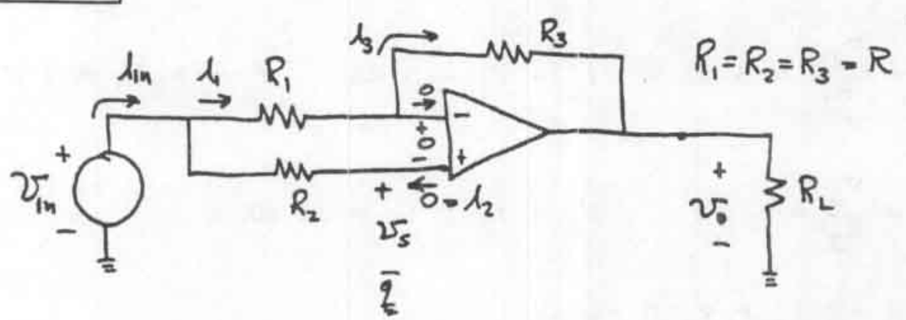
$$i_3 = \frac{v_3}{R_3} \qquad i_4 = \frac{v_2}{R_4} \qquad i_5 = i_3 + i_4 \qquad v_o = -R_5 i_5$$

The equations above yield:

$$v_o = -\frac{R_5}{R_4} v_2 + \frac{R_2 R_5}{R_1 R_3} v_1 = 4v_1 - 2v_2$$

Exercise 2.4

(a)



$$v_s = R_2 i_2 + v_{in} = v_{in} \text{ (because } i_2 = 0 \text{ by summing constraint)}$$

$$i_1 = \frac{v_{in} - v_s}{R_1} = 0$$

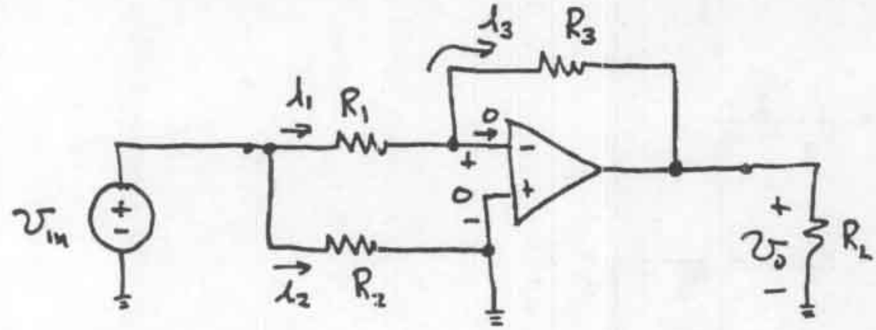
$$i_3 = i_1 = 0$$

$$v_o = -R_3 i_3 + v_s = 0 + v_{in}$$

Thus $v_o = v_{in}$ and $A_v = v_o/v_{in} = +1$

$$R_{in} = v_{in}/i_{in} = \infty$$

(b)



$$i_3 = i_1 = \frac{v_{in}}{R_1} \qquad v_o = -R_3 i_3$$

$$v_o = -\frac{R_3}{R_1} v_{in} \qquad A_v = -\frac{R_3}{R_1} = -1$$

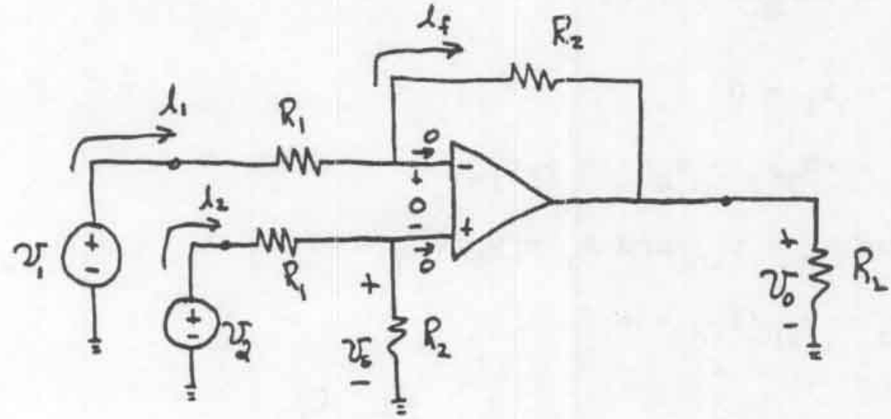
$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{v_{in}}{i_1 + i_2}$$

$$= \frac{v_{in}}{v_{in}/R_1 + v_{in}/R_2}$$

$$= \frac{1}{1/R_1 + 1/R_2}$$

$$= \frac{R}{2}$$

Exercise 2.5



$$i_2 = \frac{v_2}{R_1 + R_2}$$

$$v_s = R_2 i_2 = \frac{R_2}{R_1 + R_2} v_2$$

$$i_1 = \frac{v_1 - v_s}{R_1} = i_f$$

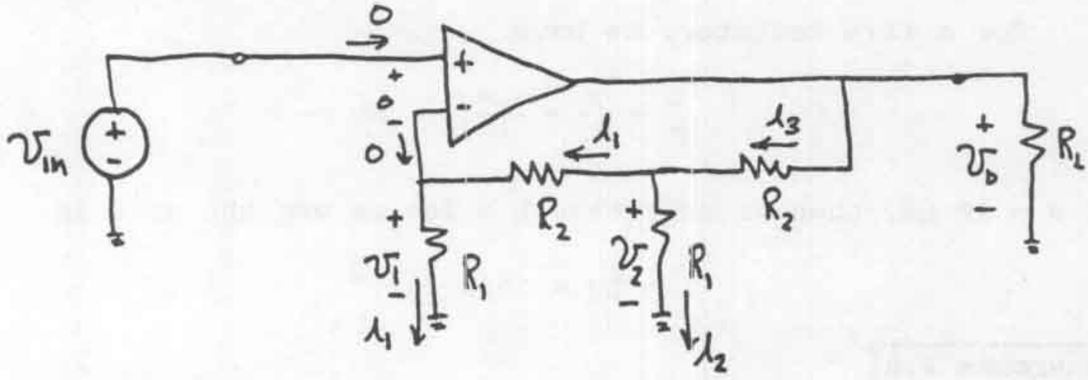
$$v_o = -R_2 i_f + v_s$$

$$= -R_2 \frac{v_1 - v_s}{R_1} + v_s = -\frac{R_2}{R_1} v_1 + \left(1 + \frac{R_2}{R_1}\right) v_s$$

$$= -\frac{R_2}{R_1} v_1 + \frac{R_1 + R_2}{R_1} \frac{R_2}{R_1 + R_2} v_2$$

$$v_o = \frac{R_2}{R_1} (v_2 - v_1)$$

Exercise 2.6



(a) $v_1 = v_{in} \quad i_1 = v_{in}/R_1 \quad v_2 = v_1 + R_2 i_1$

$$v_2 = v_{in} + \frac{R_2}{R_1} v_{in} = v_{in} \frac{R_1 + R_2}{R_1}$$

$$i_2 = \frac{v_2}{R_1} = v_{in} \frac{R_1 + R_2}{R_1^2}$$

$$i_3 = i_1 + i_2 = v_{in} \frac{1}{R_1} + v_{in} \frac{R_1 + R_2}{R_1^2}$$

$$i_3 = v_{in} \frac{2R_1 + R_2}{R_1^2}$$

$$v_o = R_2 i_3 + v_2 = v_{in} \frac{R_1^2 + R_2^2 + 3R_1R_2}{R_1^2}$$

$$A_v = \frac{v_o}{v_{in}} = 1 + 3\frac{R_2}{R_1} + \left(\frac{R_2}{R_1}\right)^2$$

(b) $A_v = 131$

(c) $R_{in} = v_{in}/i_{in} = v_{in}/0 = \infty$

(d) v_o is independent of R_L, therefore $R_o = 0$.

Exercise 2.7

For a film resistor, we have

$$\frac{L}{W} = \frac{R}{R_\square} = \frac{6000}{300} = 20$$

If W = 10 μm, then we must have L = 200 μm and the area is

$$A = LW = 2000\ (\mu m)^2$$

Exercise 2.8

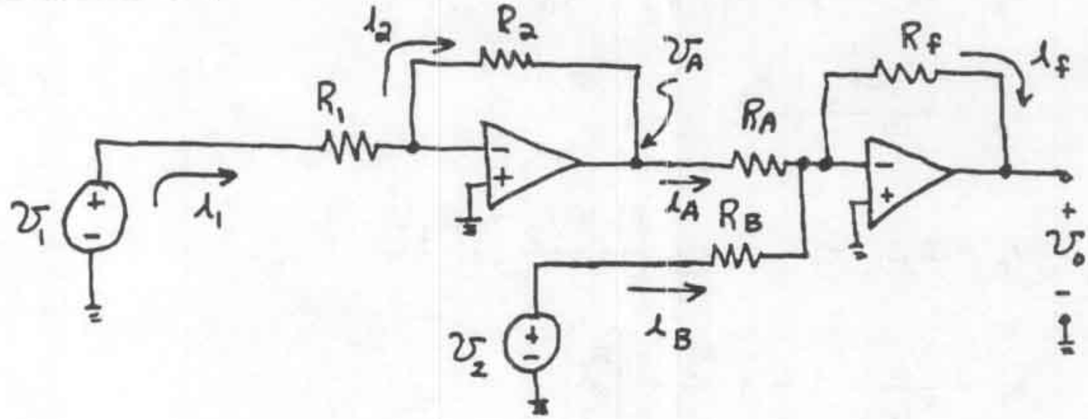
We have three rectangular sections with L/W = 5, 4, and 5 respectively. We count the corners as 0.56 square each and the end pads as 0.65 square each. Thus we have

number of squares = 2(0.65) + 2(0.56) + 5 + 4 + 5 = 16.42

Then the resistance is the number of squares times the sheet resistance.

$$R = 16.42 \times R_\square = 1642\ \Omega$$

Exercise 2.9



$$i_1 = i_2 = \frac{v_1}{R_1} \qquad v_A = -R_2 i_2 = -\frac{R_2}{R_1} v_1$$

$$i_A = \frac{v_A}{R_A} \qquad i_B = \frac{v_2}{R_B} \qquad i_f = i_A + i_B$$

$$v_o = -R_f i_f = -\frac{R_f}{R_A} v_A - \frac{R_f}{R_B} v_2$$

$$v_o = \frac{R_f R_2}{R_A R_1} v_1 - \frac{R_f}{R_B} v_2$$

Exercise 2.10

Use the circuit of Figure 2.11 with $R_2 = 3R_1$. Many resistance values would work. One example is $R_2 = 30\ \text{k}\Omega$ and $R_1 = 10\ \text{k}\Omega$. The gain of the noninverting amplifier is given by

$$A_v = 1 + \frac{R_2}{R_1}$$

The minimum value of A_v occurs if R_2 is 5% lower than its nominal value and R_1 is 5% higher. Then the gain is

$$A_v = 1 + \frac{0.95\ R_2}{1.05\ R_1} = 1 + \frac{0.95}{1.05} \times 3 = 3.714$$

which is lower than the nominal value by

$$\frac{4 - 3.714}{4} \times 100\% = 7.14\%$$

Similarly the maximum value of A_v occurs if R_2 is 5% higher than its nominal value and R_1 is 5% lower. Then the gain is

$$A_v = 1 + \frac{1.05\ R_2}{0.95\ R_1} = 1 + \frac{1.05}{0.95} \times 3 = 4.316$$

which is higher than the nominal value by

$$\frac{4.316 - 4}{4} \times 100\% = 7.89\%$$

Exercise 2.11

(a) From Equation (2.39) in the text we have:

$$f_{BOL} = \frac{A_{0CL} f_{BCL}}{A_{0OL}} = \frac{10 \times 200 \times 10^3}{10^6} = 2 \text{ Hz}$$

(b) $$f_{BCL} = \frac{A_{0OL} f_{BOL}}{A_{0CL}} = \frac{10^6 \times 2}{100} = 20 \text{ kHz}$$

Exercise 2.12

For $A_{0OL} = 10^6$ we have

$$A_{0CL} = \frac{A_{0OL}}{1 + \beta A_{0OL}} = \frac{10^6}{1 + 0.01 \times 10^6} = 99.9900$$

For $A_{0OL} = 0.9 \times 10^6$ we have

$$A_{0CL} = \frac{A_{0OL}}{1 + \beta A_{0OL}} = \frac{0.9 \times 10^6}{1 + 0.01 \times 0.9 \times 10^6} = 99.9889$$

The percentage change in gain is

$$\frac{99.9889 - 99.9900}{99.9900} = -1.1 \times 10^{-3}\%$$

Exercise 2.13

For $A_{0OL} = 10^6$ we have

$$A_{0CL} = \frac{A_{0OL}}{1 + \beta A_{0OL}} = \frac{10^6}{1 + 0.1 \times 10^6} = 9.99990$$

For $A_{0OL} = 0.9 \times 10^6$ we have

$$A_{0CL} = \frac{A_{00L}}{1 + \beta A_{00L}} = \frac{0.9 \times 10^6}{1 + 0.1 \times 0.9 \times 10^6} = 9.99989$$

The percentage change in gain is

$$\frac{9.99989 - 9.99990}{9.99990} = -0.111 \times 10^{-3}\%$$

Exercise 2.14

The circuit is shown in Figure 2.29 in the text. The op amp limits at output voltages of ±12 V and currents of ±20 mA. The gain of the circuit is 4. The output current of the op amp is

$$i_o = \frac{v_o}{R_1 + R_2} + \frac{v_o}{R_L} \qquad (1)$$

(a) For a load resistance R_L = 1 kΩ, clipping occurs for v_o = 12 V (or v_s = 3 V) because the current required for a 12-V output is 15 mA which is less than the current limit of the op amp.

(b) For a load resistance R_L = 200 Ω, clipping occurs for i_o = 20 mA. Using Equation (1), we find that this corresponds to an output voltage of v_o = 3.81 V or an input voltage of 0.952 V.

Exercise 2.15

(a) $f_{FP} = \frac{SR}{2\pi V_{omax}} = \frac{5 \times 10^6}{2\pi(4)} = 199$ kHz

(b) Clipping occurs when the output voltage limit occurs which is ±4 V.

(c) The output current is given by

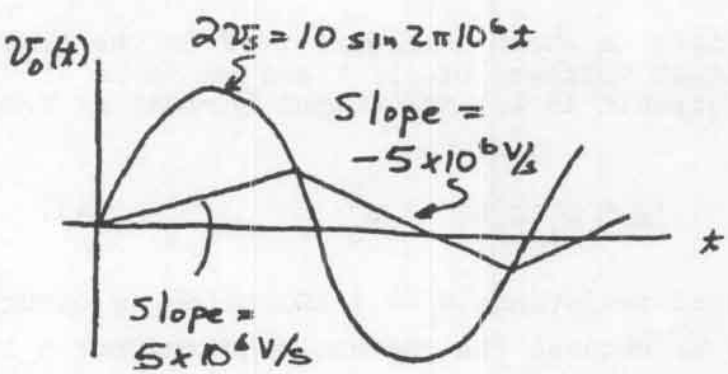
$$i_o = \frac{v_o}{R_1 + R_2} + \frac{v_o}{R_L}$$

Substituting i_o = 10 mA and the resistor values, we find v_{omax} = 0.9995 V.

(d) In this case the slew rate is the limitation.

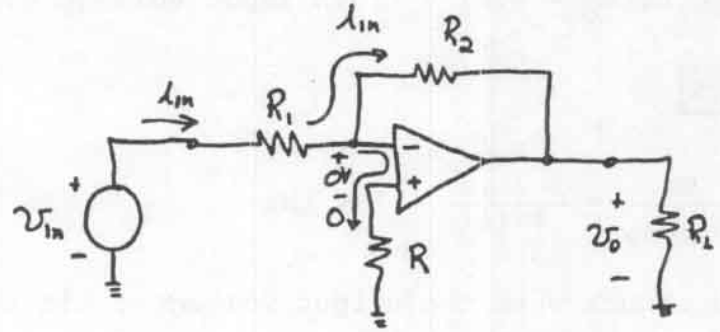
$$V_{omax} = \frac{SR}{2\pi f} = \frac{5 \times 10^6}{2\pi 10^6} = 0.796 \text{ V}$$

(e) The output is limited by the slew rate and is a triangular waveform. Its peak-to-peak amplitude is $V_{p-p} = SR \times T/2$ where $T = 1\ \mu s$ is the period of the waveform. Thus $V_{peak} = V_{p-p}/2 = 1.25$ V.



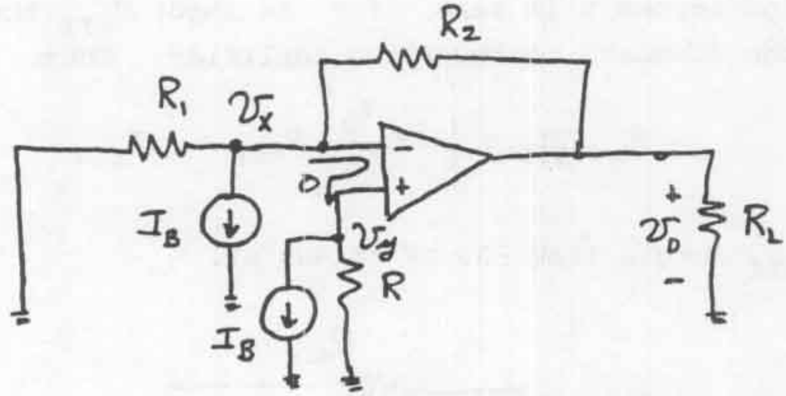
Exercise 2.16

(a)



$$i_{in} = \frac{v_{in}}{R_1} \qquad v_o = -R_2 i_{in} = -\frac{R_2}{R_1} v_{in} \qquad A_v = \frac{v_o}{v_{in}} = -\frac{R_2}{R_1}$$

(b)



The current equation at the inverting input is:

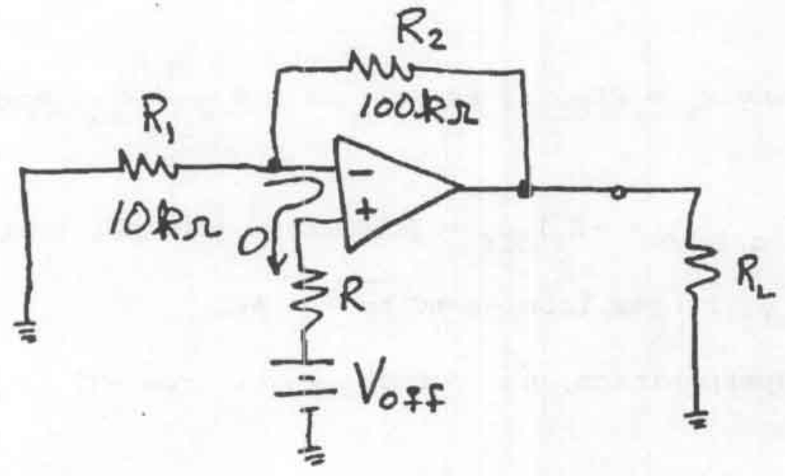
$$\frac{v_x}{R_1} + I_B + \frac{v_x - v_o}{R_2} = 0 \qquad (1)$$

Note that $v_y = -RI_B$. By the summing-point constraint we have $v_x = v_y = -RI_B$. Substituting for v_x in Equation (1) we have

$$\frac{-RI_B}{R_1} + I_B + \frac{-RI_B - v_o}{R_2} = 0$$

Then substituting $R = \frac{R_1 R_2}{R_1 + R_2}$ and solving for v_o, we find $v_o = 0$.

(c)

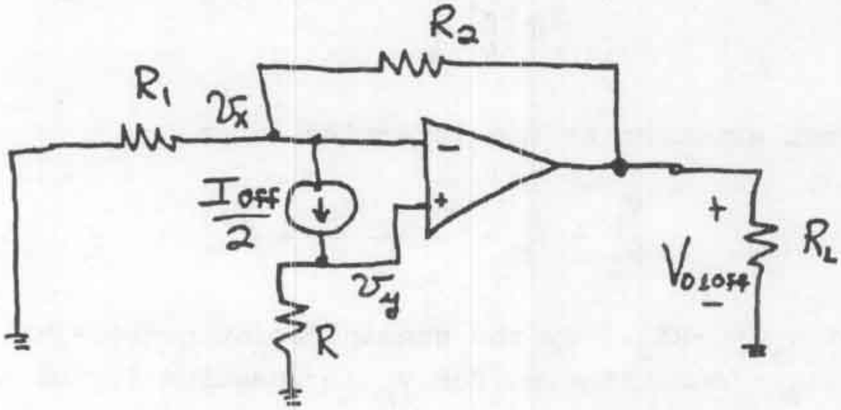


The voltage across R is zero. For the input V_{off} the circuit acts as the standard noninverting amplifier. Thus

$$V_{o,voff} = \left(1 + \frac{R_2}{R_1}\right) V_{off} = 11V_{off}$$

Thus $V_{o,off}$ ranges from -33 mV to +33 mV.

(d)



We have $v_y = RI_{off}/2$. Also because of the summing--point constraint we have $v_y = v_x$. Writing a current equation at the inverting input we have:

$$\frac{v_x}{R_1} + \frac{I_{off}}{2} + \frac{v_x - V_{o,ioff}}{R_2} = 0$$

Substituting $v_x = RI_{off}/2$ as well as $R = \frac{R_1 R_2}{R_1 + R_2}$, and solving we find:

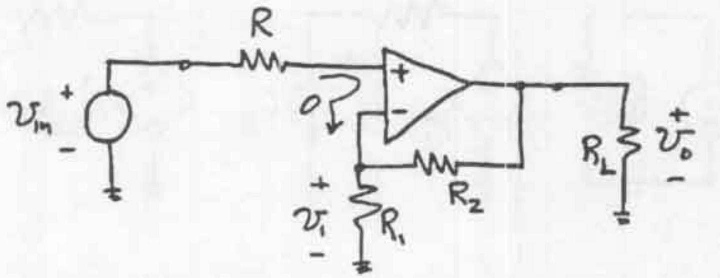
$$V_{o,ioff} = -R_2 I_{off} = (100\ k\Omega) \times (\pm 40\ nA) = \pm 4\ mV$$

Thus $V_{o,ioff}$ ranges from -4 mV to + 4 mV.

(e) By superposition, the output ranges from -37 mV to +37 mV.

Exercise 2.17

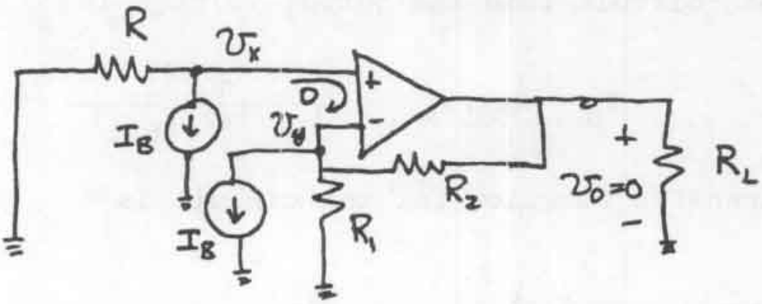
(a)



Because of the summing-point constraint, the voltage across R is zero. Thus R does not affect the gain.

$$v_{in} = v_1 = v_o \frac{R_1}{R_1 + R_2} \quad \Rightarrow \quad A_v = \frac{v_o}{v_{in}} = 1 + \frac{R_2}{R_1}$$

(b)



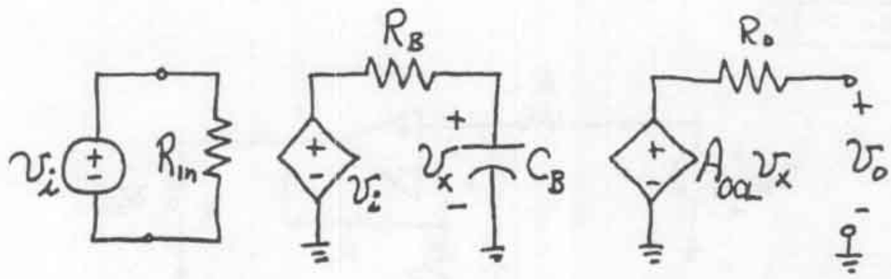
Note: With $v_o = 0$, R_2 appears to be in parallel with R_1.

$$v_x = -RI_B = v_y = -I_B \frac{R_1R_2}{R_1 + R_2}$$

Thus we want $R = R_1 || R_2 = \frac{R_1R_2}{R_1 + R_2}$

Exercise 2.18

The equivalent circuit is:



R_B and C_B act as a voltage divider and we have:

$$\mathbf{V}_x = \mathbf{V}_i \times \frac{1/(j2\pi fC_B)}{R_B + 1/(j2\pi fC_B)} = \frac{\mathbf{V}_i}{1 + j2\pi fR_BC_B} = \frac{\mathbf{V}_i}{1 + j(f/f_{BOL})}$$

With an open-circuit load the output voltage is

$$\mathbf{V}_o = A_{OOL}\mathbf{V}_x = \frac{A_{OOL}\mathbf{V}_i}{1 + j(f/f_{BOL})}$$

Thus the transfer function for the circuit is

$$\frac{\mathbf{V}_o}{\mathbf{V}_i} = \frac{A_{OOL}}{1 + j(f/f_{BOL})}$$

Exercise 2.19

See the solution of Exercise 2.18 for the circuit diagram in which we must have $R_{in} = 10$ MΩ and $R_o = 100$ Ω. For an open-circuit dc voltage gain of 90 dB we have:

$$90 = 20\log A_{OOL} \quad \Rightarrow \quad A_{OOL} = 10^{90/20} = 31.6 \times 10^3$$

$$f_{OOL} = \frac{\text{Gain-Bandwidth}}{A_{OOL}} = \frac{15 \times 10^6}{31.6 \times 10^3} = 474.7 \text{ Hz}$$

$$C_B = \frac{1}{2\pi R_B f_{OOL}} = \frac{1}{2\pi(1000)474.7} = 0.3353\ \mu\text{F}$$

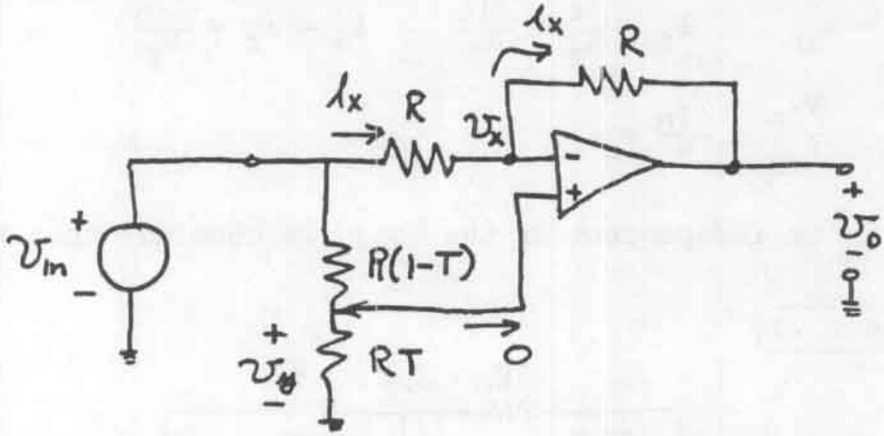
Exercise 2.20

The circuit file can be downloaded from the website for the text.

(a) From the SPICE results we find that $A_{0CL} = 1$, $f_{BCL} = 4$ MHz, and gain--bandwidth = 4 MHz.

(b) $|A_{0CL}| = 1$, $f_{BCL} = 2$ MHz, and gain--bandwidth = 2 MHz. Notice that the noninverting circuit performs best with respect to gain--bandwidth product.

Exercise 2.21



$$v_y = v_{in} \frac{RT}{R(1-T) + RT} = v_{in}T$$

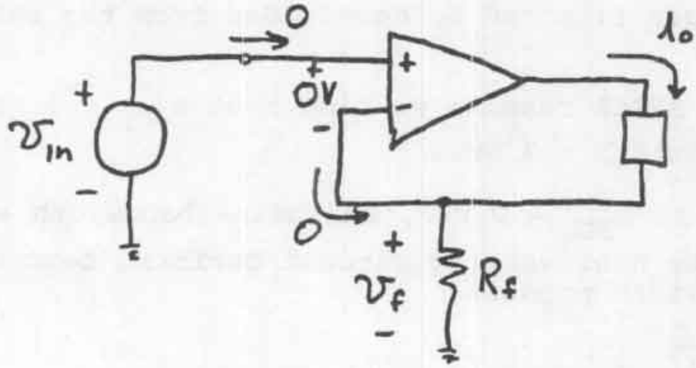
$$v_x = v_y \quad \text{(summing-point constraint)}$$

$$i_x = \frac{v_{in} - v_x}{R} = \frac{v_{in}}{R}(1-T)$$

$$v_o = -Ri_x + v_x = -v_{in}(1-T) + v_{in}T = v_{in}(2T - 1)$$

$$A_v = v_o/v_{in} = 2T - 1$$

Exercise 2.22

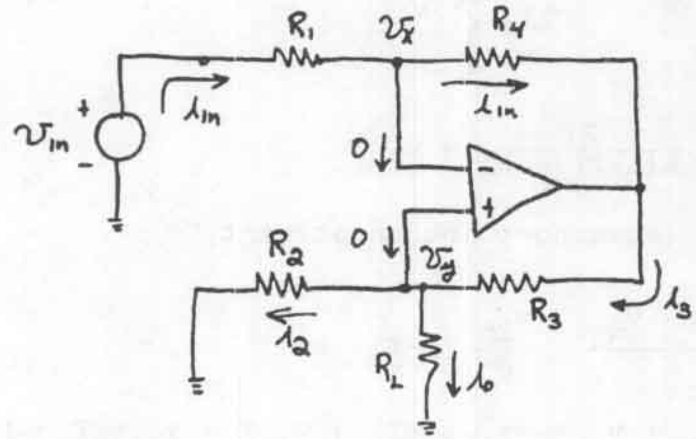


$v_f = v_{in}$ $\qquad i_f = \frac{v_f}{R_f} = \frac{v_{in}}{R_f}$ $\qquad i_o = i_f = \frac{v_{in}}{R_f}$

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{v_{in}}{0} = \infty$$

Because i_o is independent of the load, we conclude that $R_o = \infty$.

Exercise 2.23



$$v_x = v_y = v_{in} - R_1 i_{in}$$

$$R_4 i_{in} + R_3 i_3 = 0 \quad \Rightarrow \quad i_3 = -\frac{R_4}{R_3} i_{in}$$

$$i_o = i_3 - i_2 = -\frac{R_4}{R_3} i_{in} - \frac{v_y}{R_2} = -\frac{R_4}{R_3} i_{in} - \frac{v_{in} - R_1 i_{in}}{R_2}$$

Now if we have $R_4/R_3 = R_1/R_2$

$$i_o = -\frac{v_{in}}{R_2}$$

Exercise 2.24

(a) $$v_o(t) = -\frac{1}{RC}\int_0^t v_{in}(t)\,dt = -1000\int_0^t v_{in}(t)\,dt$$

$$v_o(t) = -1000\int_0^t 5\,dt = -5000\,t \qquad 0 < t < 1\text{ ms}$$

$$= -1000\int_0^{10^{-3}} 5\,dt - 1000\int_{10^{-3}}^t (-5)dt \qquad 1\text{ ms} < t < 3\text{ ms}$$

$$= -10 + 5000\,t \qquad 1\text{ ms} < t < 3\text{ ms}$$

etc.

The resulting waveform is shown in Figure 2.62 in the text.

(b) $$v_o(t) = -\frac{1}{RC}\int_0^t v_{in}(t)\,dt$$

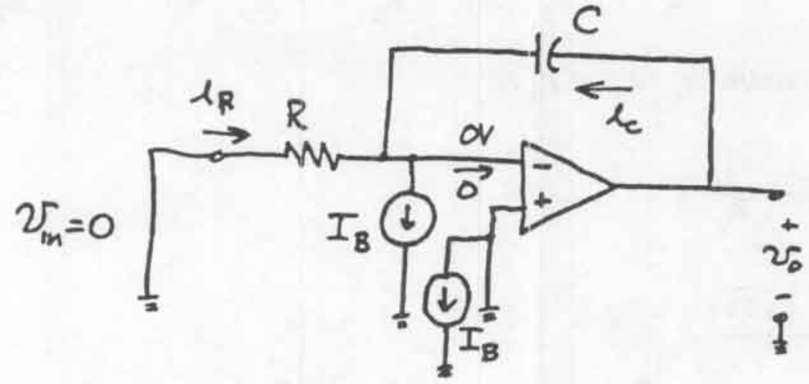
Notice that a peak-to-peak amplitude of 2 V implies a peak amplitude of 1 V. The negative peak amplitude occurs at $t = 1$ ms so we have:

$$V_{peak} = -1 = -\frac{1}{10^4 C}\int_0^{10^{-3}} 5\,dt$$

$$10^4 C = 5 \times 10^{-3}$$

$$C = 0.5\ \mu F$$

Exercise 2.25



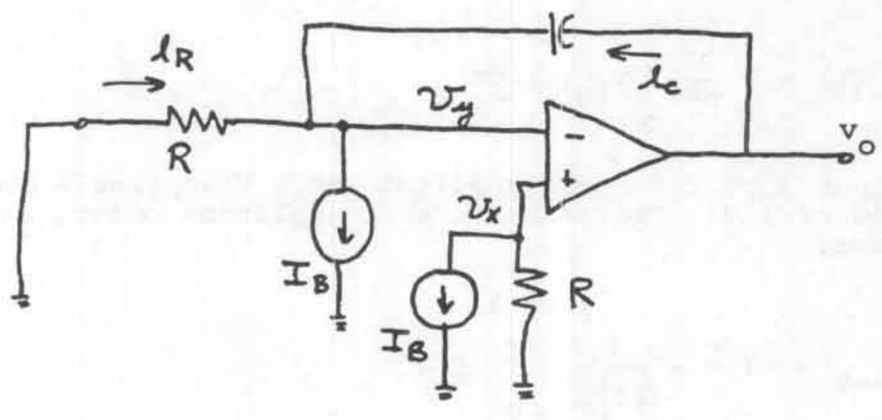
$i_R = 0/R = 0 \qquad i_C = I_B$

$$v_o = \frac{1}{C}\int_0^t i_C \, dt = \frac{1}{C}\int_0^t I_B \, dt = \frac{I_B}{C} t$$

(a) $v_o(t) = \dfrac{100 \times 10^{-9}}{10^{-8}} = 10t$

(b) $v_o(t) = \dfrac{100 \times 10^{-9}}{10^{-6}} = 0.1t$

Exercise 2.26

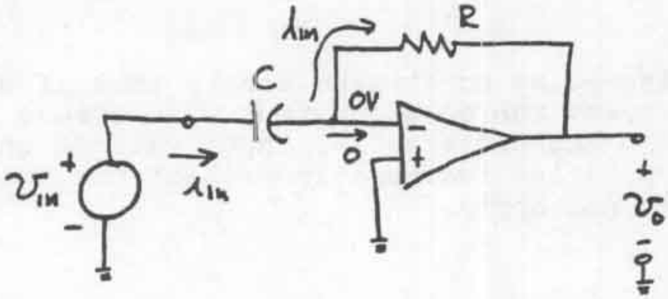


$v_y = v_x = -RI_B = -1 \text{ mV} \qquad i_R = -v_y/R = I_B$

$$i_C = I_B - i_R = 0 \qquad v_c = \frac{1}{C}\int_0^t i_C \, dt = \frac{1}{C}\int_0^t 0 \, dt = 0$$

$$v_o = v_y = -1 \text{ mV}$$

Exercise 2.27



$$i_{in} = C \frac{dv_{in}}{dt} \qquad v_o = -Ri_{in} = -RC \frac{dv_{in}}{dt}$$

Problem 2.1

Differential input voltage: $v_{id} = v_1 - v_2$

Common-mode input voltage: $v_{icm} = \frac{1}{2}(v_1 + v_2)$

Problem 2.2

$$v_{id} = v_1 - v_2 = 0.2\cos(20\pi t)$$

$$v_{icm} = \frac{1}{2}(v_1 + v_2) = 20\sin(120\pi t)$$

Problem 2.3

An ideal operational amplifier has the following characteristics:

- Infinite input impedance.
- Infinite open-loop gain A_{OL} for the differential signal.
- Zero gain for the common-mode signal.
- Zero output impedance.
- Infinite bandwidth.

Problem 2.4

Three pins are needed for each op amp: two input pins and an output pin. Thus we can have four op amps in a 14-pin package allowing two pins for power-supply connections common to all four op amps.

Problem 2.5

The summing-point constraint states that if negative feedback is present the op amp output will assume the value required to zero the differential input voltage and input currents. If positive feedback is present the summing-point constraint does not apply.

Problem 2.6

The steps in analyzing linear op-amp circuits are:

1. Verify that negative feedback is present. Usually this takes the form of a resistor network connected to the output terminal and to the inverting input terminal.

2. Assume that the differential input voltage and the input current of the op amp are forced to zero. (This is the summing-point constraint.)

3. Apply standard circuit analysis principles, such as Kirchhoff's laws and Ohm's law, to solve for the quantities of interest.

Problem 2.7

In a shower we use negative feedback to adjust water temperature. If it is too hot we increase the cold-water flow or reduce the hot-water flow. We adjust until the difference between actual temperature and desired temperature is driven to zero.

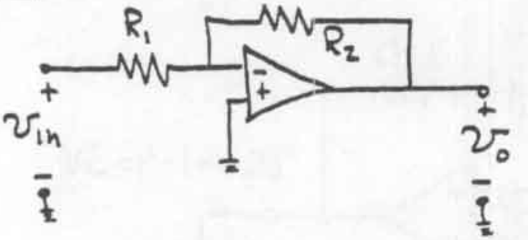
In driving an automobile on a two-lane highway in the United States we adjust the position of our vehicle to remain centered in the right-hand lane. If we are too close to the edge of the highway we steer toward the center, if we are too close to the center we steer to the right.

Problem 2.8

Positive feedback is a problem when we have a fire in a building. When a fire first starts heat is created which vaporizes additional fuel increasing the size of the fire. Usually positive feedback is self limiting. In the case of a building fire, the fire dies out when the building is totally consumed.

When our children behave well we give them positive feedback encouraging them to continue their good behavior.

Problem 2.9

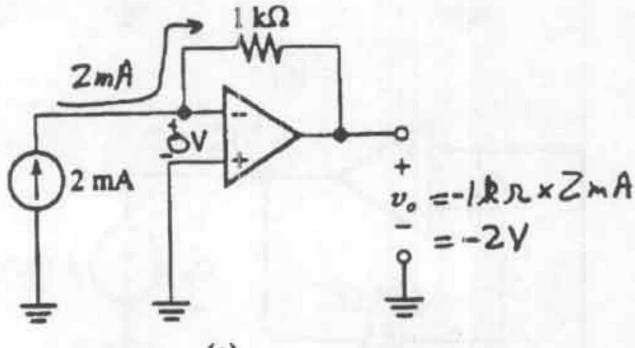


$$A_v = -\frac{R_2}{R_1}$$

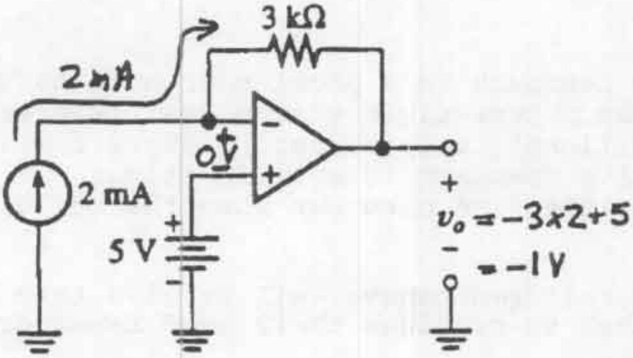
$$R_{in} = R_1$$

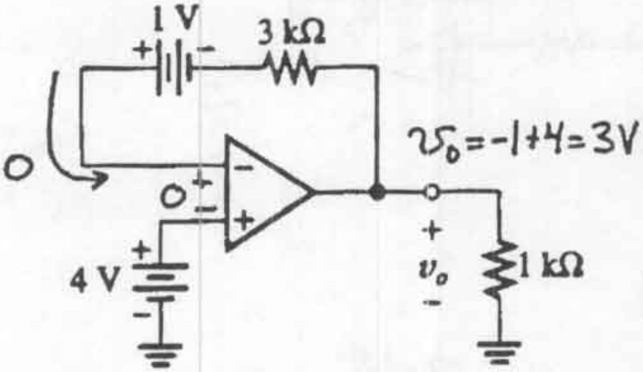
$$R_o = 0$$

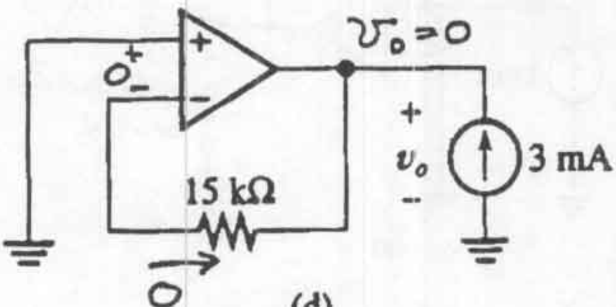
Problem 2.10

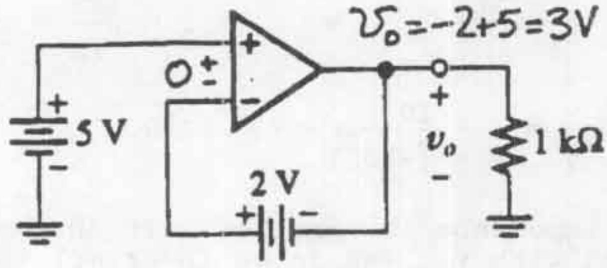


(a)


3 kΩ
2mA
2 mA
0V
5 V
vo = −3x2+5
= −1V
(b)

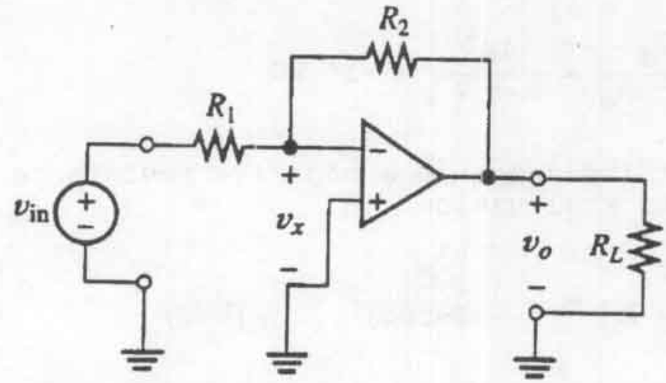

1 V
3 kΩ
v0 = −1+4 = 3V
0
0
4 V
vo
1 kΩ
(c)


v0 = 0
0
15 kΩ
vo
3 mA
0
(d)



(c)

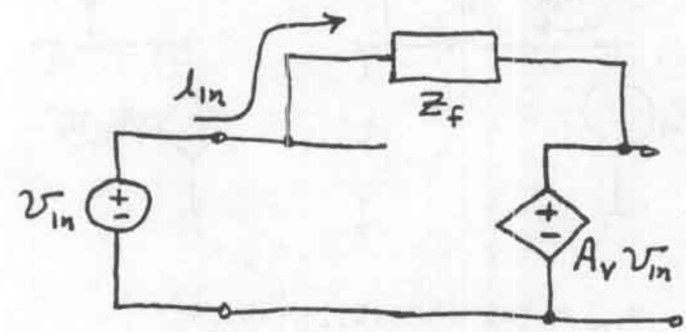
Problem 2.11



Notice that $A_v = -R_2/R_1 = -10$. For $v_o = 12$ V, we have $v_{in} = v_o/A_v = 12/(-10) = -1.2$ V and $v_x = v_o/(-A_{OL}) = 12/(-10^4) = -1.2$ mV. Thus v_x is 1000 times less than v_{in}, and v_x can be assumed to be zero with sufficient accuracy for most applications. Thus we are justified in using the summing-point constraint for this circuit.

Problem 2.12

(a)



$$I_{in} = \frac{V_{in} - A_v V_{in}}{Z_f} \quad \Rightarrow \quad Z_{in} = \frac{V_{in}}{I_{in}} = \frac{Z_f}{1 - A_v}$$

(b) $$Z_{in} = \frac{Z_f}{1 - A_v} = \frac{10^4}{1 - (-10^5)} \cong 0.10\ \Omega$$

The input impedance is very low. If an impedance were placed in series with v_{in} (as in an inverter) the input voltage to the op amp would be driven to zero as the op amp open-loop gain approaches infinity (just as we assume when we use the summing-point constraint).

(c) $$Z_{in} = \frac{Z_f}{1 - A_v} = \frac{10^4}{1 - 2} = -10\ k\Omega$$

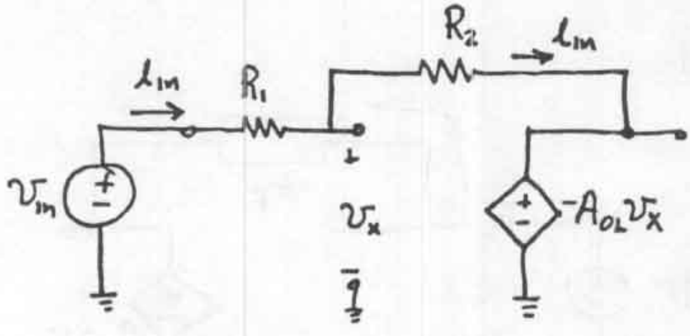
The input impedance is a negative resistance. This is a positive feedback situation.

(d) $$Z_{in} = \frac{Z_f}{1 - A_v} = \frac{\frac{1}{j\omega C}}{1 - (-100)} = \frac{1}{j\omega(99C)}$$

The input impedance is that of a 99-pF capacitance. This situation often occurs in amplifiers because of device capacitances and is a significant problem when extended high-frequency response is needed.

Problem 2.13

The equivalent circuit is:



$$V_{in} = (R_1 + R_2)I_{in} - A_{OL}V_x \tag{1}$$

$$V_x = V_{in} - R_1 I_{in} \qquad (2)$$

Using Equation (2) to substitute for V_x in Equation (1) and solving for the input impedance, we find

$$Z_{in} = \frac{V_{in}}{I_{in}} = R_1 + \frac{R_2}{1 + A_{OL}}$$

Evaluating for $R_1 = 1\ k\Omega$, $R_2 = 10\ k\Omega$, and $A_{OL} = 10^4$, we find

$$Z_{in} = 1001\ \Omega$$

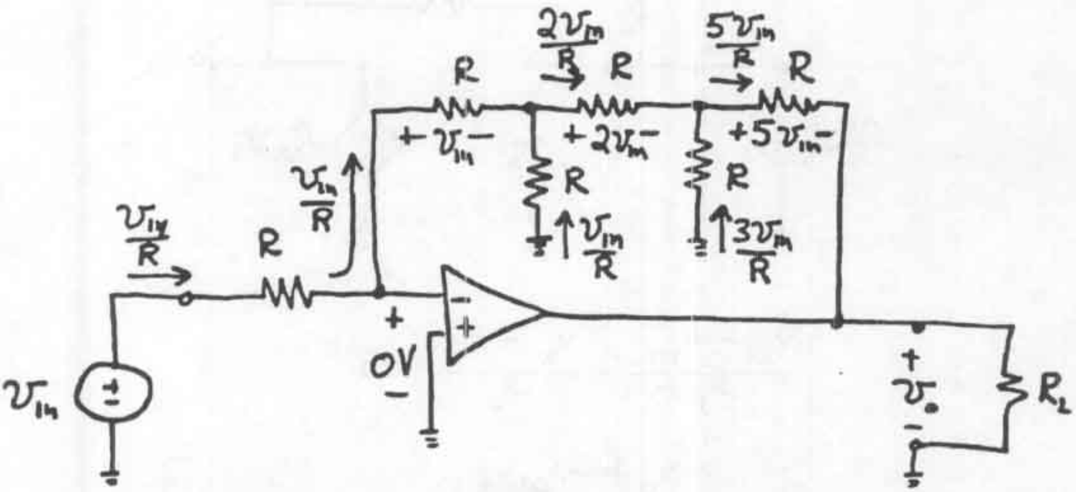
The input impedance assuming infinite A_{OL} is

$$Z_{in} = R_1 = 1000\ \Omega$$

The percentage difference between the two answers is 0.1%

Problem 2.14

Starting from the input and working toward the output we can determine the voltages and currents shown below:



Eventually we determine that $v_o = 8v_{in}$ so we have a closed loop voltage gain of 8.

Problem 2.15

The circuit diagram for the inverting amplifier is shown in Figure 2.5 in the text. The gain of an inverting amplifier is $A_v = -R_2/R_1$. The largest gain magnitude occurs if R_2 is 1% high and R_1 is 1% low in which case we have

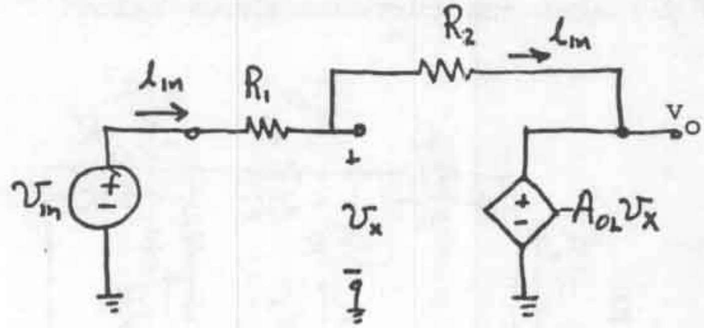
$$A_v = -\frac{1.01R_{2nom}}{0.99R_{1nom}} = 1.020\ A_{vnom}$$

in which R_{1nom} is the nominal value of R_1, R_{2nom} is the nominal value of R_2 and A_{vnom} is the nominal gain.

Similarly, for the opposite extreme we obtain $A_v = 0.980A_{vnom}$. Thus the tolerance of the closed-loop gain is ±2%.

Problem 2.16

The equivalent circuit is:



$$\frac{v_x - v_{in}}{R_1} + \frac{v_x - v_o}{R_2} = 0 \qquad (1)$$

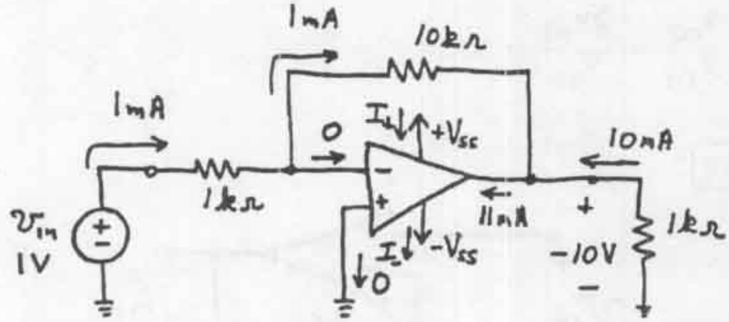
$$v_o = -A_{OL}v_x \qquad (2)$$

Solving Equation (2) for v_x, substituting into Equation (1), and applying algebra yields

$$A_v = \frac{-R_2A_{OL}}{R_2 + R_1 + A_{OL}R_1}$$

For $R_1 = 1\ k\Omega$, $R_2 = 10\ k\Omega$ and $A_{OL} = 10^4$ we obtain A_v -9.989. For $A_{OL} = 10^5$, we obtain $A_v = -9.998$. As A_{OL} approaches infinity, A_v approaches $-R_2/R_1 = 10$.

Problem 2.17

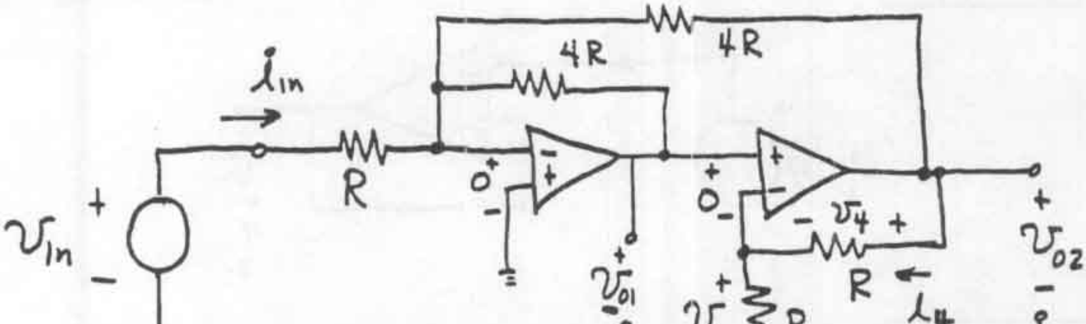


Kirchhoff's current law may not seem to be satisfied for the op-amp terminals if we do not consider the power-supply terminals. However if we considered the power-supply currents, the equation

$$I_+ + 11\ \text{mA} = I_-$$

would be satisfied. Not enough information is given in the problem to determine the power-supply currents.

Problem 2.18



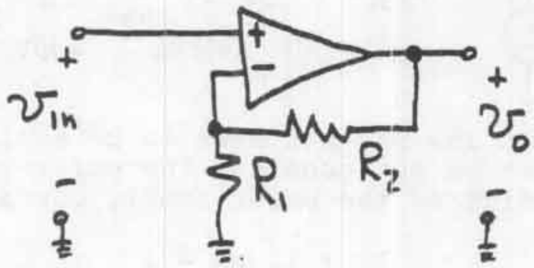
$$v_{o1} = v_3 \qquad i_{in} = \frac{v_{in}}{R} \qquad i_4 = i_3 = v_{o1}/R$$

$$v_{o2} = v_3 + v_4 = 2v_{o1} \qquad i_{in} + \frac{v_{o1}}{4R} + \frac{v_{o2}}{4R} = 0$$

$$\frac{v_{in}}{R} + \frac{v_{o1}}{4R} + \frac{2v_{o1}}{4R} = 0 \quad \Rightarrow \quad A_1 = \frac{v_{o1}}{v_{in}} = -\frac{4}{3}$$

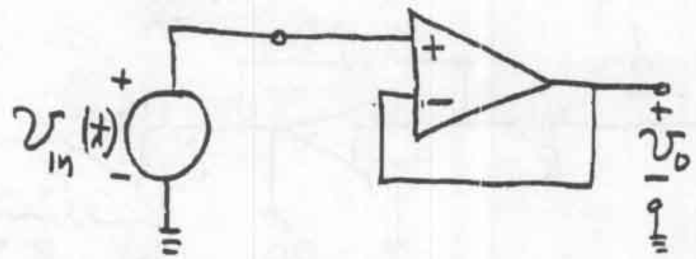
$$A_2 = \frac{v_{o2}}{v_{in}} = \frac{2v_{o1}}{v_{in}} = 2A_1 = -\frac{8}{3}$$

Problem 2.19



$$A_v = 1 + R_2/R_1 \qquad R_{in} = \infty \qquad R_o = 0$$

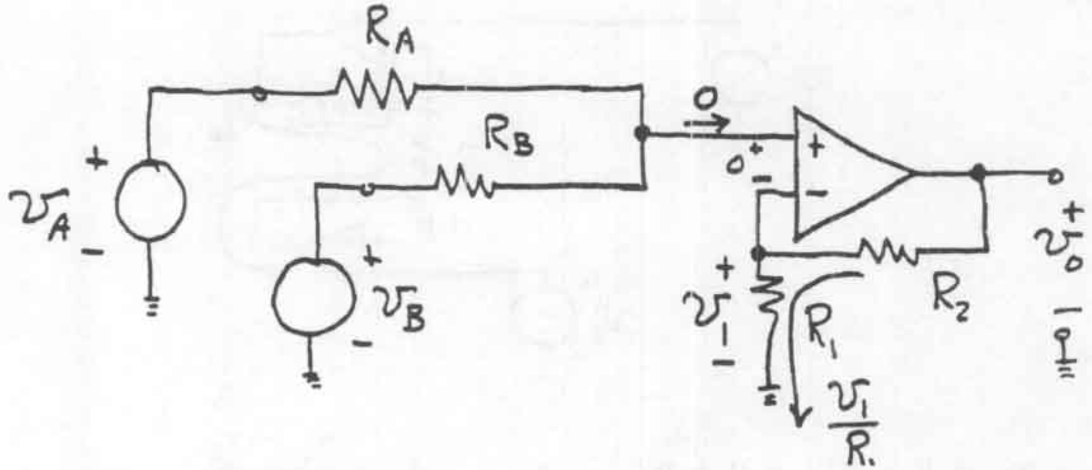
Problem 2.20



Problem 2.21

The voltage follower has a very large input impedance (ideally infinite) and a very low output impedance (ideally 0). If the source impedance is much larger than the load impedance and the load is connected directly to the source, the load voltage is much less than the open-circuit source voltage. By using the voltage follower, the load voltage can be nearly equal to the open-circuit source voltage.

Problem 2.22



$$\frac{v_1 - v_A}{R_A} + \frac{v_1 - v_B}{R_B} = 0 \quad \Rightarrow \quad v_1 = \frac{v_A R_B + v_B R_A}{R_A + R_B}$$

$$v_o = v_1 + R_2 \frac{v_1}{R_1} = \frac{R_1 + R_2}{R_1} v_1$$

$$v_o = \frac{R_1 + R_2}{R_1} \times \frac{v_A R_B + v_B R_A}{R_A + R_B}$$

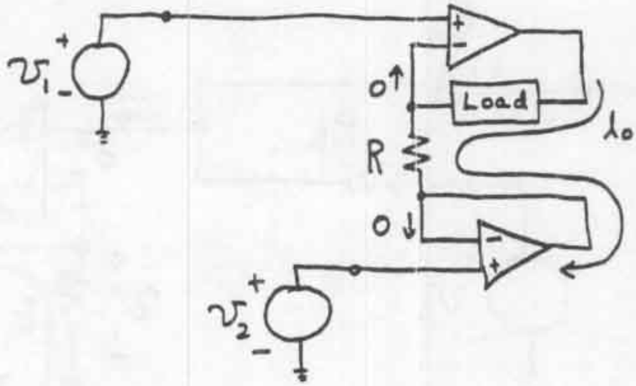
$$v_o = A_A v_A + A_B v_B$$

where $A_A = \dfrac{R_1 + R_2}{R_1} \times \dfrac{R_B}{R_A + R_B}$

and $A_B = \dfrac{R_1 + R_2}{R_1} \times \dfrac{R_A}{R_A + R_B}$

Problem 2.23

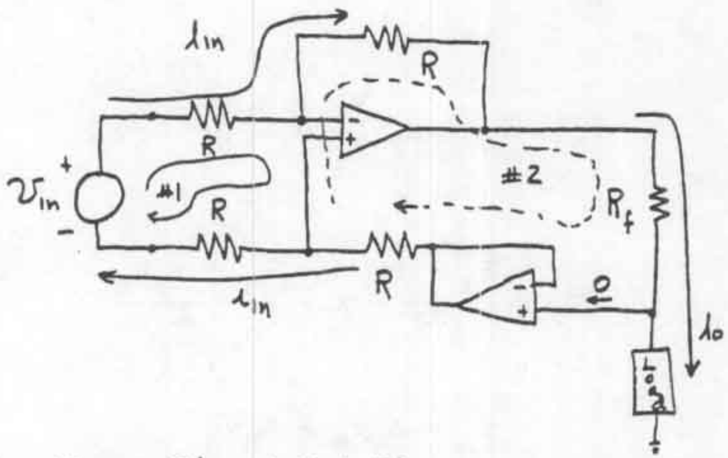
(a)



$$v_1 = 0 + Ri_o + 0 + v_2 \quad \Rightarrow \quad i_o = \frac{v_1 - v_2}{R}$$

Because i_o is independent of the load we conclude that the output impedance is infinite.

(b)



Loop 1: $v_{in} = Ri_{in} + 0 + Ri_{in}$

Loop 2: $Ri_{in} + R_f i_o + Ri_{in} = 0$

Solving: $i_o = -v_{in}/R_f$

Because i_o is independent of the load, we conclude that the output impedance is infinite.

Problem 2.24

(a) $A_v = \frac{V_o}{V_{in}} = -\frac{R_2}{R_1} \qquad P_{in} = \frac{V_s^2}{R_1} \qquad P_o = \frac{V_o^2}{R_L} = \frac{R_2^2 V_s^2}{R_1^2 R_L}$

$$G = \frac{P_o}{P_{in}} = \frac{R_2^2}{R_1 R_L}$$

(b) $P_{in} = 0$ because $I_{in} = 0$. Therefore $G = P_o/P_{in} = \infty$. Thus the noninverting amplifier has the higher power gain.

Problem 2.25

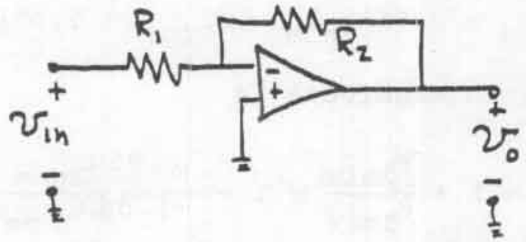
(a) $v_o = -R_f i_{in}$

(b) Because v_o is independent of R_L, the output behaves as an ideal voltage source and the output resistance is zero.

(c) The input voltage is zero because of the summing-point constraint. Therefore $R_{in} = 0$.

(d) This is an ideal transresistance amplifier.

Problem 2.26



Because $A_v = -R_2/R_1$, we select the nominal resistances such that $R_{2nom} = 2R_{1nom}$. Given 5%-tolerances we have

$$R_{1min} = 0.95R_{1nom} \qquad R_{1max} = 1.05R_{1nom}$$

$$R_{2min} = 0.95R_{2nom} \qquad R_{2max} = 1.05R_{2nom}$$

Then the minimum gain magnitude is

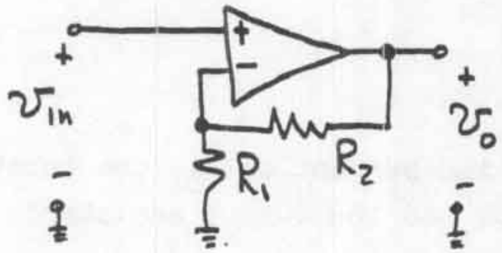
$$|A_v|_{min} = \frac{R_{2min}}{R_{1max}} = \frac{0.95R_{2nom}}{1.05R_{1nom}} = 1.81$$

Similarly

$$|A_v|_{max} = \frac{R_{2max}}{R_{1min}} = \frac{1.05R_{2nom}}{0.95R_{1nom}} = 2.21$$

The tolerances of the gain magnitude are -9.5% and +10.5%.

Problem 2.27



Because $A_v = 1 + R_2/R_1$, we select the nominal resistances such that $R_{2nom} = R_{1nom}$. Given 5%-tolerances we have

$$R_{1min} = 0.95R_{1nom} \quad R_{1max} = 1.05R_{1nom}$$

$$R_{2min} = 0.95R_{2nom} \quad R_{2max} = 1.05R_{2nom}$$

Then the maximum gain magnitude is

$$|A_v|_{min} = 1 + \frac{R_{2min}}{R_{1max}} = 1 + \frac{0.95R_{2nom}}{1.05R_{1nom}} = 1.905$$

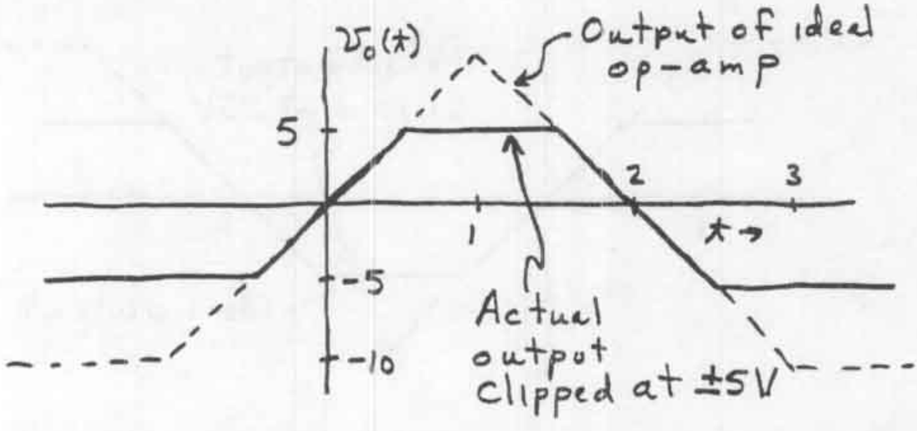
Similarly

$$|A_v|_{max} = 1 + \frac{R_{2max}}{R_{1min}} = 1 + \frac{1.05R_{2nom}}{0.95R_{1nom}} = 2.105$$

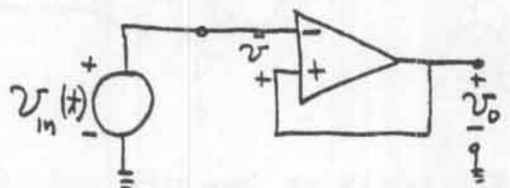
The tolerances of the gain magnitude are -4.75% and +5.25%.

Problem 2.28

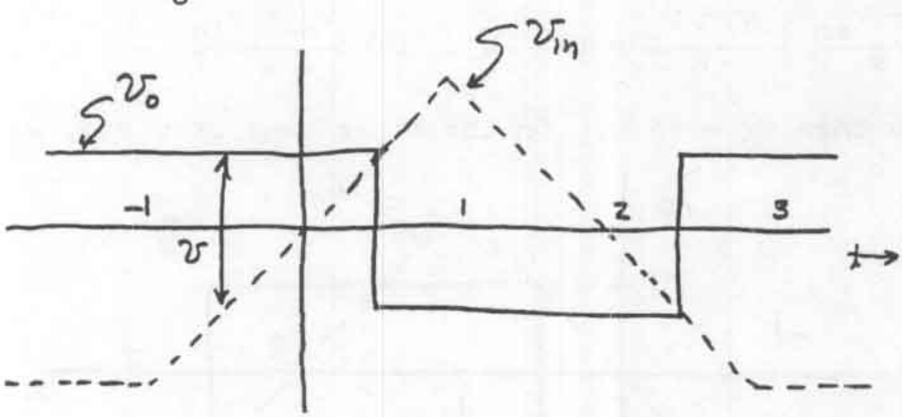
(a) This circuit has negative feedback. For an ideal op amp we have $v_o(t) = v_{in}(t)$.



(b) This circuit has positive feedback. The summing-point constraint does not apply. Instead either $v_o = +5$ V or $v_o = -5$ V.

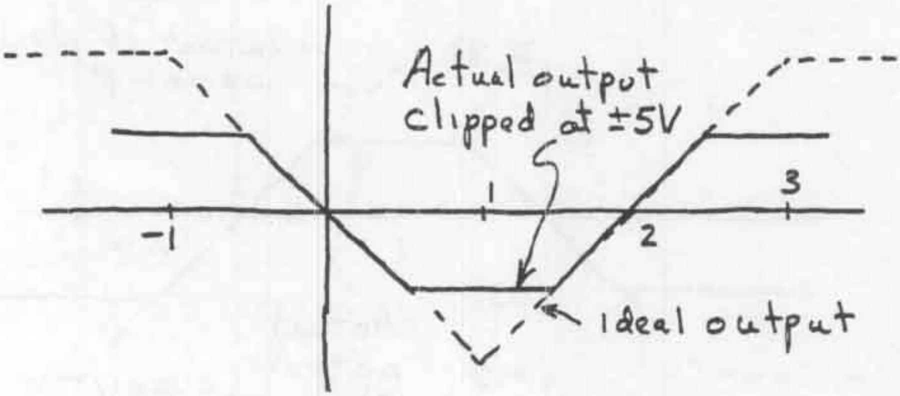


Notice that $v = v_o - v_{in}$. If $v > 0$, $v_o = +5$ V. On the other hand if $v < 0$, $v_o = -5$ V.

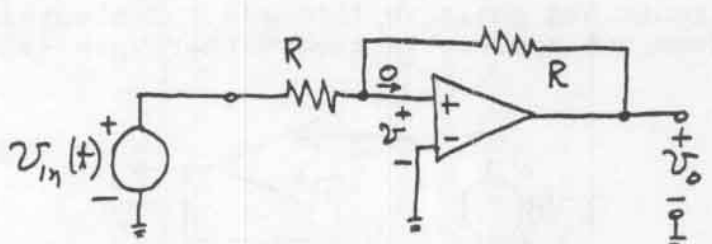


Problem 2.29

(a) This circuit has negative feedback. For an ideal op amp we have $v_o(t) = -v_{in}(t)$.



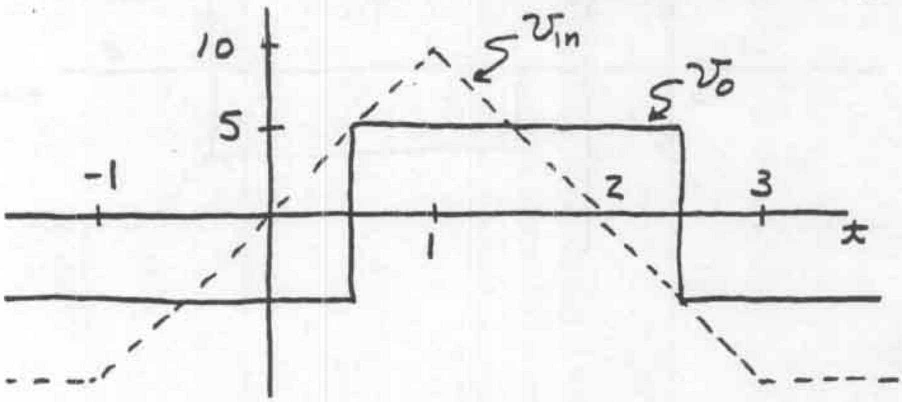
(b)



This circuit has positive feedback and the summing-point constraint does not apply. Writing a current equation at the noninverting input of the op amp yields

$$\frac{v - v_{in}}{R} + \frac{v - v_o}{R} = 0 \quad \Rightarrow \quad v = \frac{v_o + v_{in}}{2}$$

If $v > 0$ then $v_o = +5$ V. On the other hand if $v < 0$, $v_o = -5$.



Problem 2.30

The sheet resistances of the various layers are commonly optimized for purposes, such as the base regions of BJTs, other than fabricating resistors. Adding more steps to the process to create layers optimized for resistors would reduce yield and increase cost.

Problem 2.31

Very small resistances imply large currents and high power dissipation. Very large resistances are subject to stray coupling of undesired signals. Furthermore, resistances of either extreme are likely to require excessive chip area because $R = R_{\square}L/W$ and we need to have $L \cong W$ for minimum area.

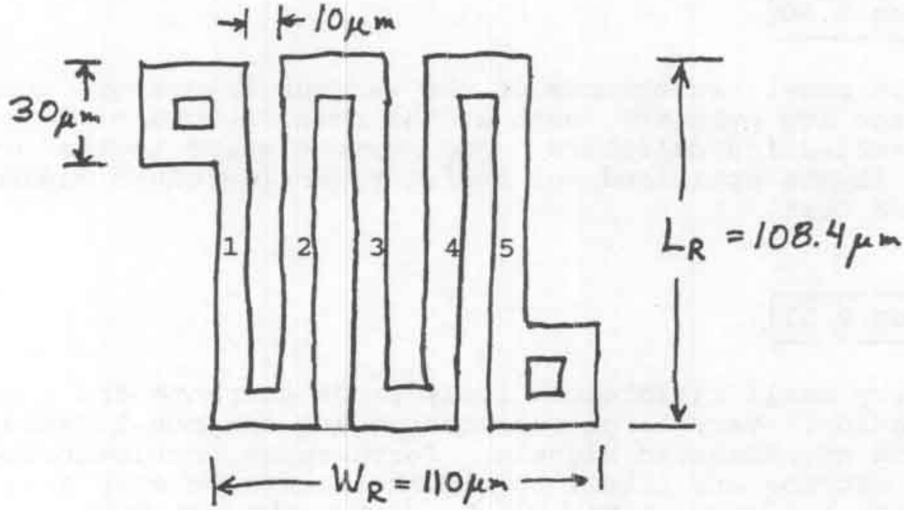
Problem 2.32

Doubling the thickness of the layer creates a second identical resistor above or below the original resistor. The resistors are electrically in parallel. Thus the resistance is reduced by a factor of 2. If we double the thickness of a 200-Ω layer, the sheet resistance $R_{\square}$ is reduced to 100 Ω.

Problem 2.33

We should choose the width of the conductors to be $W = 10\ \mu m$ to minimize the area consumed. For a resistor composed of a single straight conductor, we would have $L = WR/R_{\square} = 10(10^4/200) = 500\ \mu m$. Including the guard strips the area consumed is $(20\ \mu m) \times L = 10^4\ \mu m^2$.

Because we want the resistor to occupy an approximately square area, we need $W_R = L_R \cong \sqrt{A} = 100\ \mu m$. Thus, we need $W_R/(20\ \mu m) = 5$ or 6 conductors. We propose the layout composed of 5 conductors:



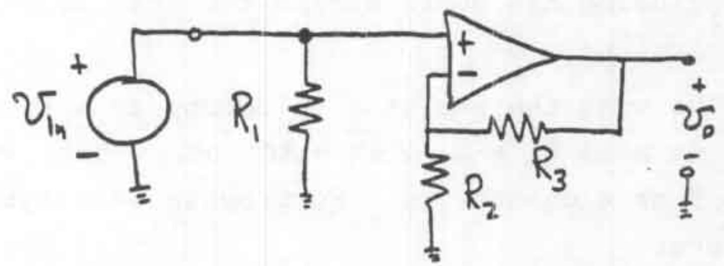
For this layout, the resistance is the sum of:

two end pads:	$2 \times 0.65 \times 200 = 260\ \Omega$
eight corners:	$8 \times 0.56 \times 200 = 896\ \Omega$
four ends:	$4 \times 200 = 800\ \Omega$
Conductors 1 and 5:	$2 \times [(L_R - 40)/10] \times 200 = 40L_R - 1600$
Conductors 2, 3, and 4:	$3 \times [(L_R - 20)/10] \times 200 = 60L_R - 1200$
Total	$100L_R - 844$

Thus we need $10^4\ \Omega = 100L_R - 844$ which yields $L_R = 108.4\ \mu m$

Problem 2.34

Here is one solution:



$R_{in} = R_1 = 10\ k\Omega \quad R_2 = 20\ k\Omega \quad R_3 = 180\ k\Omega$

Problem 2.35

A simple answer is the standard inverter shown in Figure 2.5 in the text with R_1 = 1 kΩ and R_2 = 100 kΩ for a total resistance of 101 kΩ.

A better answer is the circuit shown in Figure 2.6 in the text with $R_1 = R_3$ = 1 kΩ and $R_2 = R_4$ = 9.05 kΩ for a total resistance of 20.1 kΩ. (See the analysis of this circuit in Example 2.1 in the text.)

Very likely still better answers exist.

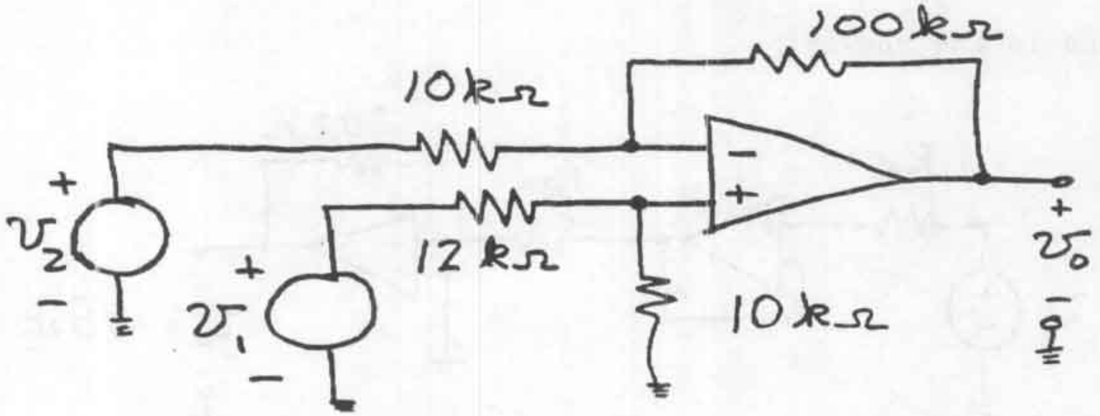
Problem 2.36

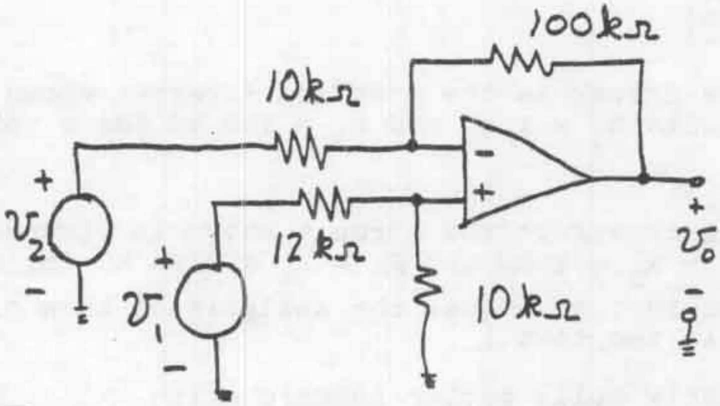
A good answer is to cascade two noninverting amplifiers like the one shown in Figure 2.11 in the text. Each amplifier should have R_1 = 1 kΩ and R_2 = 9 kΩ. The total resistance is 20 kΩ and two op amps are used. The total area consumed is that of 4 op amps. (We assume that area is proportional to resistance.)

Another good answer is the circuit of Figure 2.15 analyzed in Exercise 2.6 with R_1 = 1 kΩ and R_2 = 8.56 kΩ for a total area equal to nearly 3 op amps.

Problem 2.37

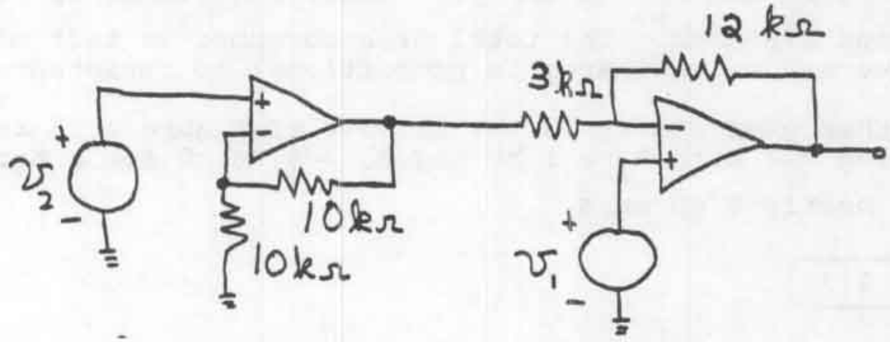
Here are two answers:





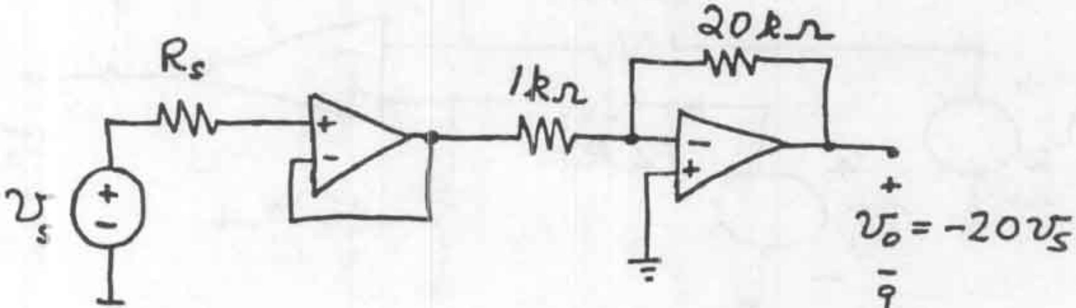
Problem 2.38

Two possibilities are to place unity-gain voltage followers between the sources and the inputs of the circuits designed for Problem 2.37. A better answer that uses fewer op amps is:



Problem 2.39

Here is one answer:



Problem 2.40

Op amp imperfections in the linear range of operation include:

- finite input impedance
- nonzero output impedance
- finite open-loop gain
- finite bandwidth
- nonzero common-mode gain

Problem 2.41

For the noninverting amplifier with a given op amp, the product of dc gain and closed-loop bandwidth is constant as the dc gain is changed.

Problem 2.42

(a) Refer to Figure P2.42 in the text.

$$v_s = R_{in} i_s + R_o i_s + A_{OL}(R_{in} i_s)$$

$$v_o = R_o i_s + A_{OL}(R_{in} i_s)$$

$$A_{vs} = \frac{v_o}{v_s} = \frac{R_o + A_{OL} R_{in}}{R_{in} + R_o + A_{OL} R_{in}}$$

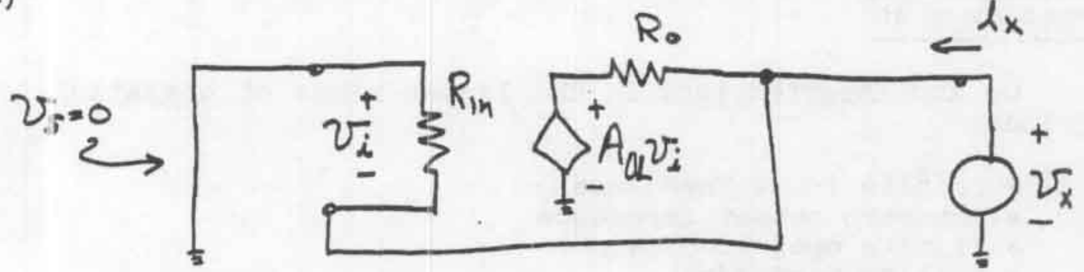
$$A_{vs} = \frac{25 + 10^5 \times 10^6}{10^6 + 25 + 10^5 \times 10^6} = 0.99999$$

The gain would be 1.00000 for an ideal op amp.

(b) $Z_{in} = \frac{v_s}{i_s} = R_{in} + R_o + A_{OL} R_{in} = 10^{11}\ \Omega$

In comparison, we would have $Z_{in} = \infty$ for an ideal op amp.

(c)



$v_i = -v_x \qquad i_x = \frac{v_x}{R_{in}} + \frac{v_x - A_{OL}v_i}{R_o} \qquad Z_o = \frac{v_x}{i_x} = \frac{1}{\frac{1}{R_{in}} + \frac{1 + A_{OL}}{R_o}}$

Evaluating we find $Z_o = 2.5 \times 10^{-4}\ \Omega$ compared to $Z_o = 0$ for an ideal op amp.

Problem 2.43

(a) Refer to Figure P2.43 in the text. Writing current equations at the input terminal of the op amp and at the output terminal we have:

$$\frac{v_s + v_i}{R_1} + \frac{v_o + v_i}{R_2} + \frac{v_i}{R_{in}} = 0 \qquad (1)$$

$$\frac{v_o + v_i}{R_2} + \frac{v_o - A_{OL}v_i}{R_o} = 0 \qquad (2)$$

Now we solve Equation (1) for v_i, substitute into Equation (2), and use algebra to obtain:

$$A_{vs} = \frac{v_o}{v_s} = \frac{-R_2}{R_1\left[1 + \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_{in}}\right)\frac{R_oR_2 + R_2^2}{A_{OL}R_2 - R_o}\right]}$$

Evaluating we find $A_{vs} = -9.9989$ compared to $A_{vs} = -10$ for an ideal op amp.

(b) From the circuit we can write:

$$v_s = R_1 i_s - v_i \tag{3}$$

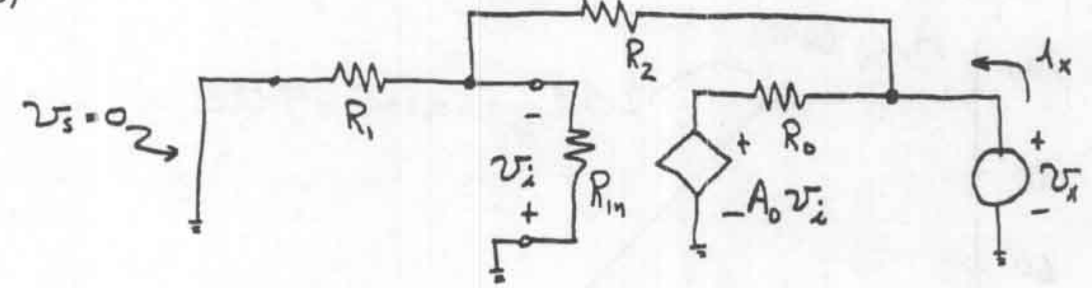
$$v_i + (R_1 + R_o)\left(\frac{v_i}{R_{in}} + i_s\right) + A_{OL} v_i = 0 \tag{4}$$

Now we solve Equation (3) for v_i, substitute into Equation (4), and use algebra to obtain:

$$Z_{in} = \frac{v_s}{i_s} = R_1 + \frac{R_2 + R_o}{1 + A_{OL} + \dfrac{R_2 + R_o}{R_{in}}}$$

Evaluating we find $Z_{in} = 1.0001$ kΩ compared to $Z_{in} = 1.0000$ kΩ for an ideal op amp.

(c)



$$v_i = \frac{R_{in}||R_1}{R_2 + R_{in}||R_1} v_x$$

$$i_x = \frac{v_x}{R_2 + R_{in}||R_1} + \frac{v_x - A_{OL} v_i}{R_o}$$

$$Z_o = \frac{v_x}{i_x} = \frac{1}{\dfrac{1}{R_2 + R_{in}||R_1} + \dfrac{1}{R_o}\left(1 + \dfrac{A_{OL}(R_{in}||R_1)}{R_2 + R_{in}||R_1}\right)}$$

Evaluating we find Z_o = 2.75 mΩ compared to Z_o = 0 for an ideal op amp.

Problem 2.44

Equation 2.39 states:

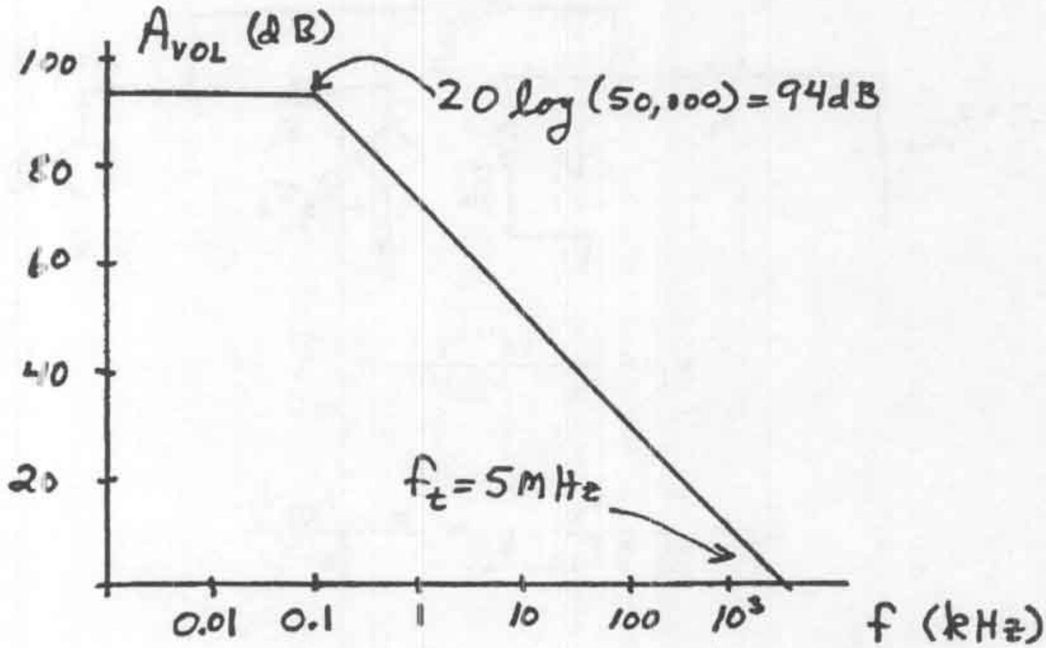
$$f_t = A_{OCL}f_{BCL} = A_{OOL}f_{BOL}$$

Solving for f_{BCL} we have

$$f_{BCL} = \frac{f_t}{A_{OCL}}$$

For A_{OCL} = 10 we find f_{BCL} = 1.5 MHz. For A_{OCL} = 100, we have f_{BCL} = 150 kHz.

Problem 2.45



Problem 2.46

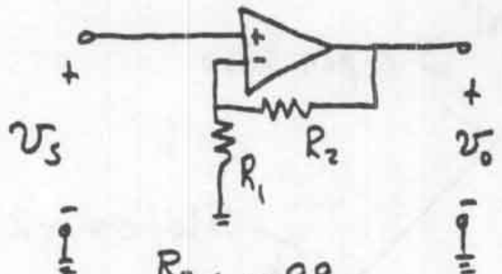
$$A_{OL}(f) = \frac{A_{0OL}}{1 + j(f/f_{BOL})} = \frac{2 \times 10^5}{1 + j(f/5)}$$

Evaluating we find:

Frequency	$\lvert A_{OL} \rvert$	Phase
100	9988	-87.14°
1 kHz	1000	-89.71°
1 MHz	1	-90.00°

Problem 2.47

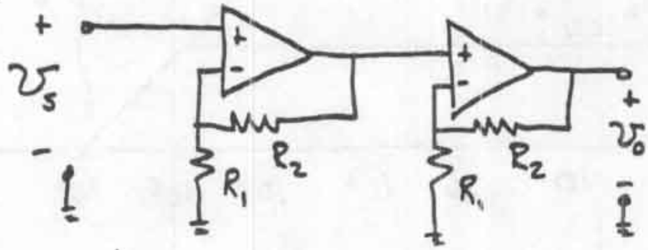
Alternative 1:



$R_2/R_1 = 99$

The half-power bandwidth is $f_{BCL} = f_t/A_{0CL} = 10^6/100 = 10$ kHz

Alternative 2:



$R_2/R_1 = 9$

For each stage we have $f_{BCL} = f_t/A_{0CL} = 10^6/10 = 100$ kHz

$$A_{CL}(f) = \frac{A_{0CL}}{1 + j(f/f_{BCL})} = \frac{10}{1 + j(f/10^5)}$$

The overall gain is

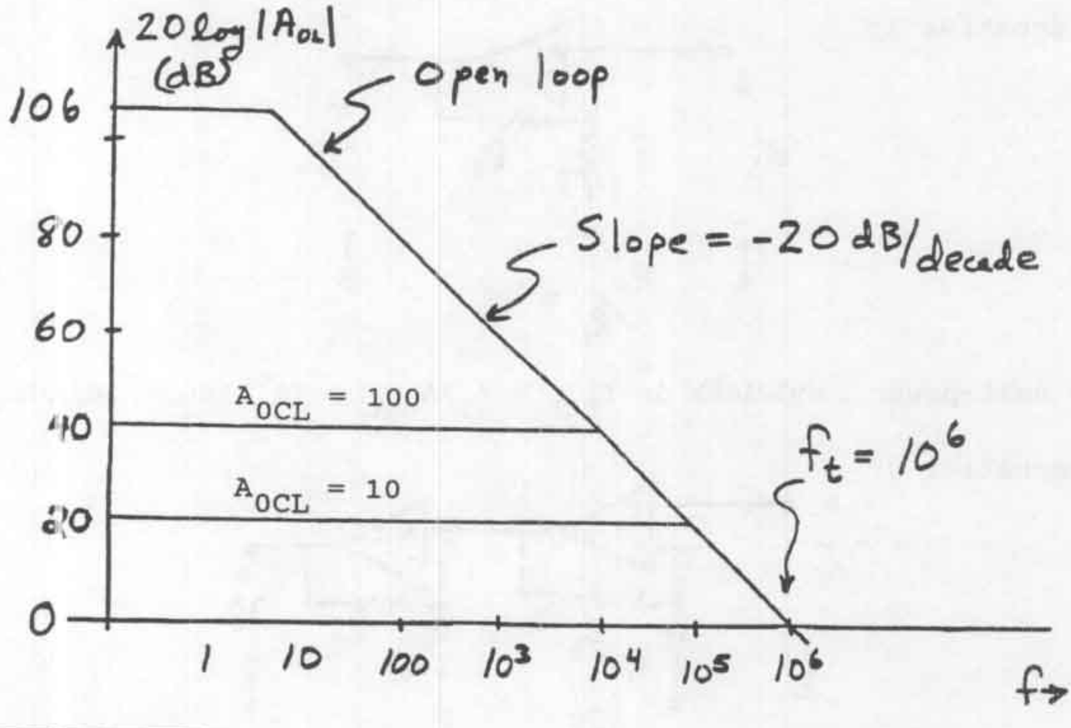
$$A(f) = \left[\frac{10}{1 + j(f/10^5)} \right]^2$$

At the half-power frequency f_H we have:

$$\frac{100}{\sqrt{2}} = \frac{100}{1 + (f_H/10^5)^2}$$

Solving we find f_H = 64.4 kHz compared with 10 kHz for the single stage amplifier.

Problem 2.48



Problem 2.49

The slew-rate limitation is the maximum rate at which the op-amp output can increase or decrease.

Full-power bandwidth is the maximum frequency for which a full-amplitude sine wave output does not experience slew-rate limiting.

Problem 2.50

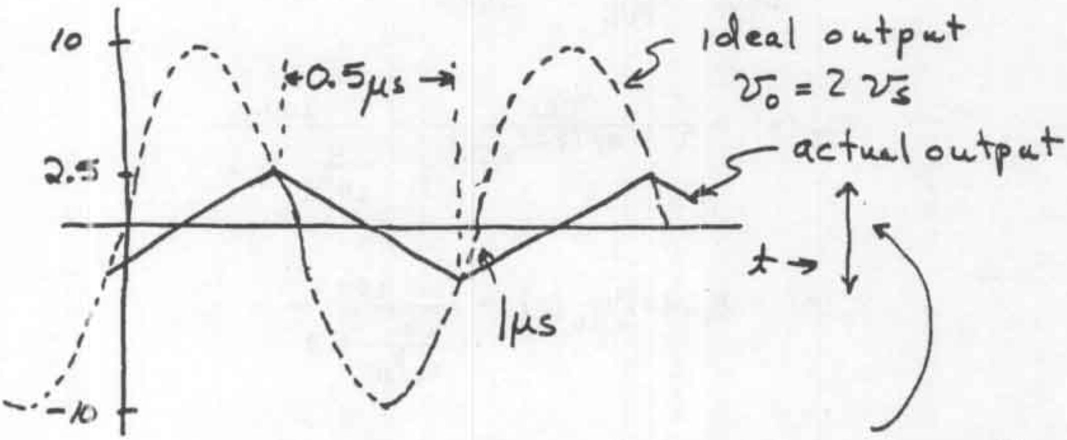
(a) $f_{FP} = \frac{SR}{2\pi V_{om}} = \frac{10^7}{2\pi 10}$

$= 159$ kHz

(b) 10 V (Amplitude limitation of the op amp.)

(c) $V_{om} = 20$ mA $\times$ 100 Ω = 2 V (Limited by current capability of the op amp.)

(d) $V_{om} = \frac{SR}{2\pi f} = \frac{10^7}{2\pi 10^6} = 1.59$ V



peak-to-peak amplitude = 0.5μs × 10^7 V/s
= 5 V

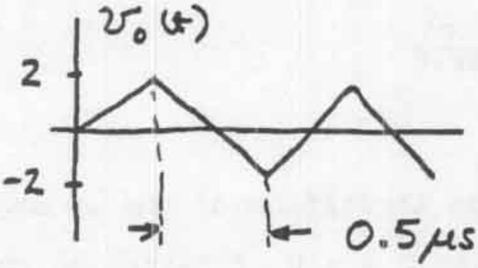
Problem 2.51

$$SR = 2\pi f V_{om}$$

$$= 2\pi 10^5 \times 5$$

$$= 3.14 \times 10^6 = 3.14 \text{ V/}\mu\text{s}$$

Problem 2.52



$$SR = \frac{4\ V}{0.5\ \mu s} = 8\ V/\mu s$$

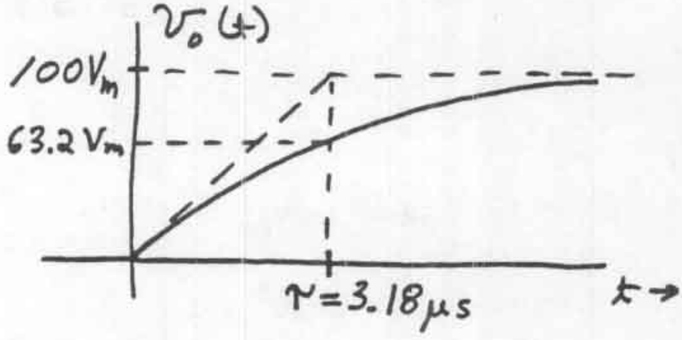
Problem 2.53

$$f_{0CL} = \frac{f_t}{A_{0CL}} = \frac{5 \times 10^6}{100} = 50\ kHz$$

$$A_{CL}(s) = \frac{A_{0CL}}{1 + s/(2\pi f_{BCL})} = \frac{100}{\dfrac{s}{10^5\pi} + 1}$$

$$V_o(s) = A_{CL}(s)V_{in}(s) = \frac{100}{\dfrac{s}{10^5\pi} + 1} \times \frac{V_m}{s}$$

$$v_o(t) = 100V_m - 100V_m \exp(-\pi 10^5 t)$$



$$\frac{dv_o(t)}{dt} = 100V_m(\pi 10^5)\exp(-\pi 10^5 t)$$

$$\left|\frac{dv_o(t)}{dt}\right|_{max} = \pi 10^7 V_m \qquad \text{(at } t = 0\text{)}$$

$$\pi 10^7 V_m = SR = 10^6 \quad \Rightarrow \quad V_m = 31.8 \text{ mV}$$

Problem 2.54

The circuit shown in Figure P2.54 is an inverting amplifier with a closed loop dc gain of -10.

(a) $f_{FP} = \frac{SR}{2\pi V_{om}} = \frac{10^6}{2\pi 10} = 15.9$ kHz

(b) Notice that the output of the op amp must supply current to R_2 as well as to R_L. Thus we have:

$$V_{om} = (25 \text{ mA}) \times R_L||R_2 = 2.498 \text{ V}$$

(c) $V_{om} \doteq 10$ V (limited by maximum range of output voltage)

(d) $V_{om} = \frac{SR}{2\pi f} = \frac{10^6}{2\pi 10^5} = 1.59$ V (limited by slew rate)

Problem 2.55

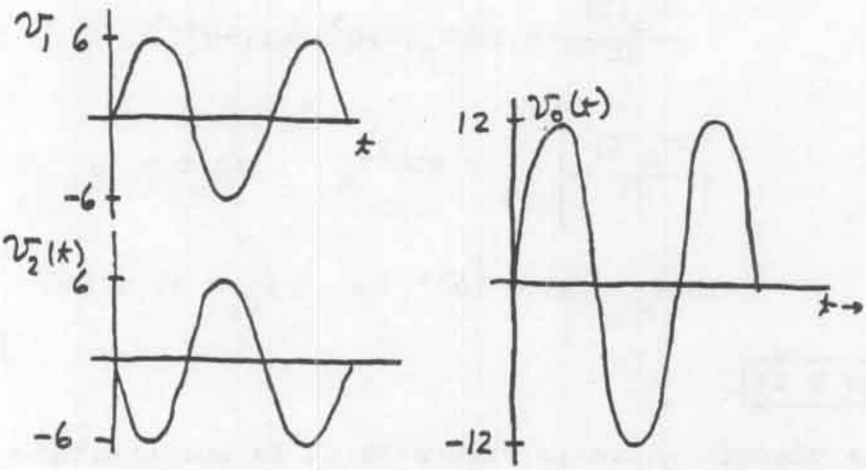
(a) Refer to the circuit shown in Figure P2.55 in the text. Notice that the upper op amp is configured as a noninverting amplifier with a gain of 2. The lower op amp is configured as an inverting amplifier with a gain of -2. Thus we have

$$v_2(t) = -2v_s(t)$$

$$v_1(t) = 2v_s(t)$$

$$v_o(t) = v_1(t) - v_2(t) = 4v_s(t) \quad \Rightarrow \quad A_{vs} = \frac{v_o}{v_s} = 4$$

(b)



(c) $v_o(t)$ is clipped when it reaches amplitudes of ±28 V.

Problem 2.56

See Figure 2.33 in the text.

Problem 2.57

Lower bias and offset currents are the main advantages of a FET-input op amp compared to a BJT-input op amp.

Problem 2.58

Following the approach of Example 2.10 in the text, we obtain:

Offset voltage: $V_o = (1 + R_2/R_1) \times (\pm 4 \text{ mV})$

$= \pm 44$ mV

Bias current: $V_o = R_2 I_B = 20$ mV

Offset current: $V_o = R_2 I_{off}/2 = \pm 2.5$ mV

Total: V_o ranges from -26.5 mV to +66.5 mV

Problem 2.59

The problem with the circuit shown in Figure P2.59 is that the bias current of the op amp must flow through the coupling capacitor. The voltage across the capacitor ramps up (or down) until the op amp reaches its maximum output. A solution is to connect a large resistance from the noninverting input to ground to provide a path for the bias current. To minimize the effect of the bias current, the resistance should be 50 kΩ. However, this may make the input impedance too small, depending on the application.

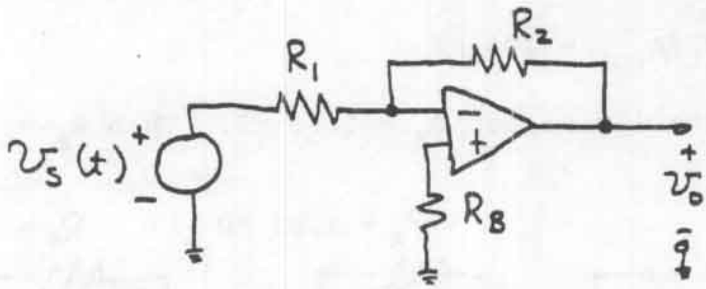
Problem 2.60

(a) $V_o = V_{off}(1 + R_2/R_1) \Rightarrow \pm 100\text{ mV} = V_{off} \times 11 \Rightarrow$

$V_{off} = \pm 9.09\text{ mV}$

(b) $V_o = I_B R_2 \Rightarrow I_B = (\pm 100\text{ mV})/(100\text{ k}\Omega) \Rightarrow I_B = \pm 1\ \mu A$

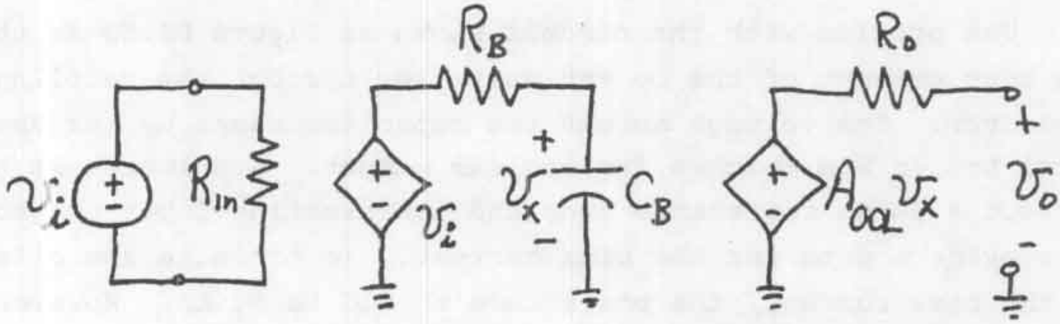
(c)



$R_B = R_1 || R_2 = 9.09\text{ k}\Omega$

(d) $V_o = I_{off} R_2 \Rightarrow I_{off} = (\pm 100\text{ mV})/R_2 = \pm 1\ \mu A$

Problem 2.61



Problem 2.62

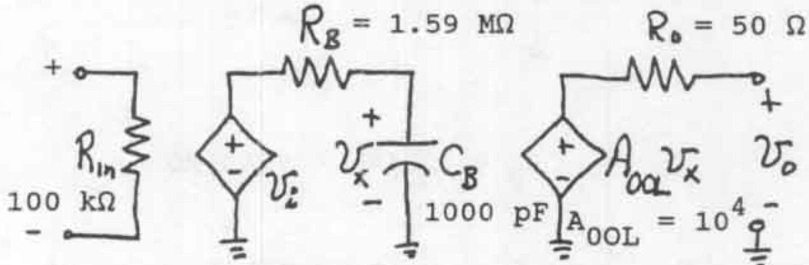
A macromodel is a relatively simple circuit that models the external behavior of an op amp. A macromodel usually does not resemble the actual internal circuit of the op amp. The advantage of a macromodel is that simulations run faster and require less memory than if the actual internal circuit was used in the simulation.

Problem 2.63

$80 = 20\log|A_{OOL}| \Rightarrow A_{OOL} = 10^{80/20} = 10^4$

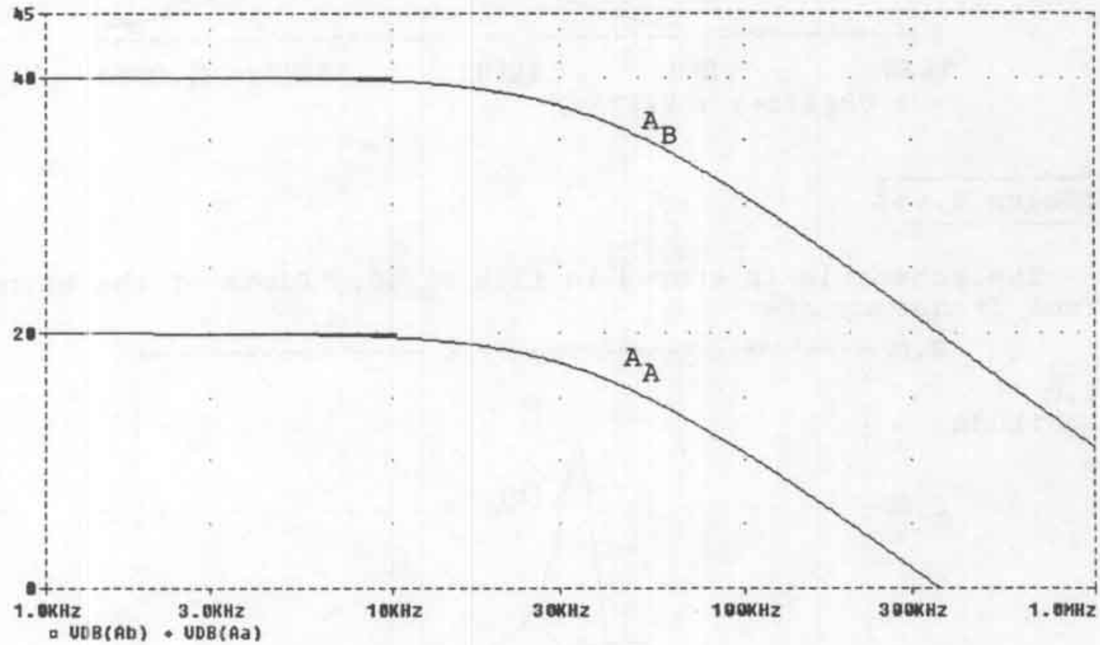
$f_{BOL} = f_t/A_{OOL} = 100$ Hz

We arbitrarily select $C_B = 1000$ pF. Then $R_B = 1/(2\pi f_{BOL} C_B)$ $= 1.59$ MΩ.



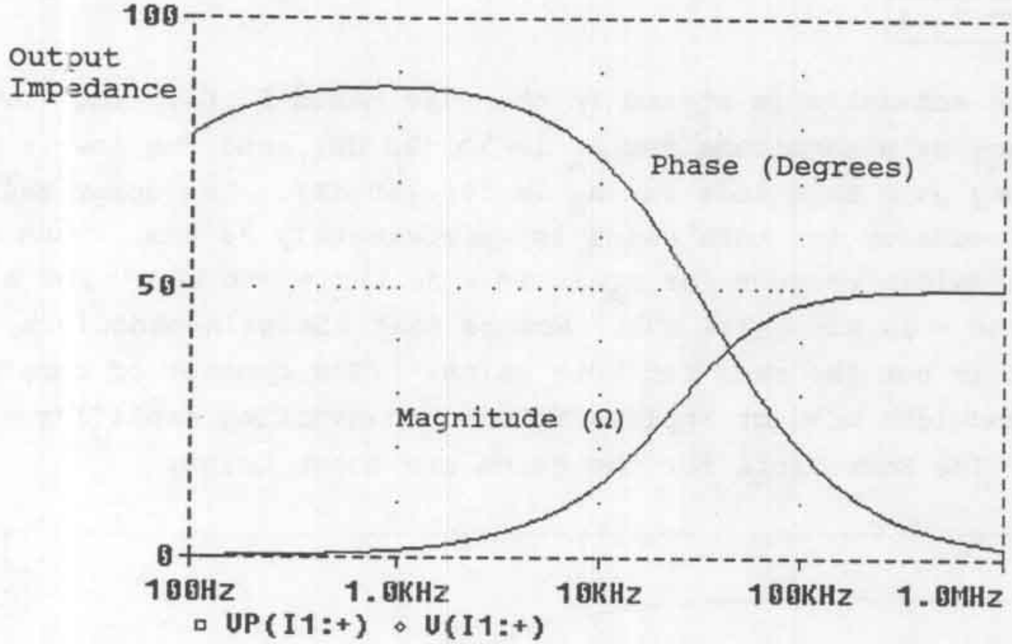
Problem 2.64

The schematic is stored in the file named P2_64. The low-frequency gain magnitude for A_A is 10 (20 dB), and the low-frequency gain magnitude for A_B is 100 (40 dB). The upper half-power frequency for both gains is approximately 36 kHz. Thus the gain-bandwidth product for A_A is 10 × 36 kHz = 360 kHz. For A_B it is 100 × 36 kHz = 3.6 MHz. Notice that the gain-bandwidth product is not the same for both gains. (The concept of constant gain-bandwidth product applies to the noninverting amplifier only.) The Bode plots for the gains are shown below.



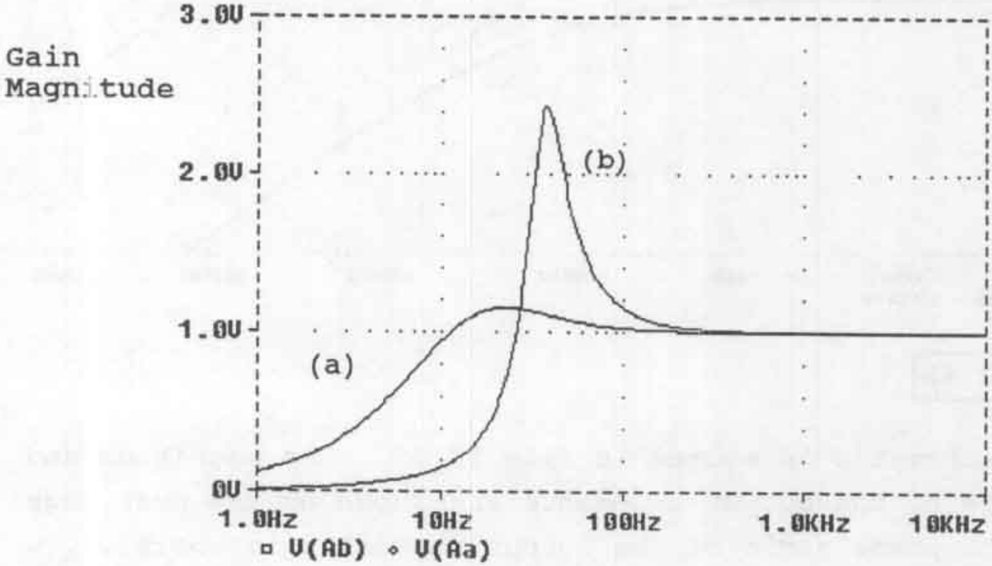
Problem 2.65

The schematic is stored in file P2_65. The magnitude and phase plots of the output impedance are shown on the next page. Because the phase angle of the output impedance is positive, we say that the output impedance is inductive. Notice that at higher frequencies the output impedance of the circuit approaches that of the op amp alone which is 50 Ω.



Problem 2.66

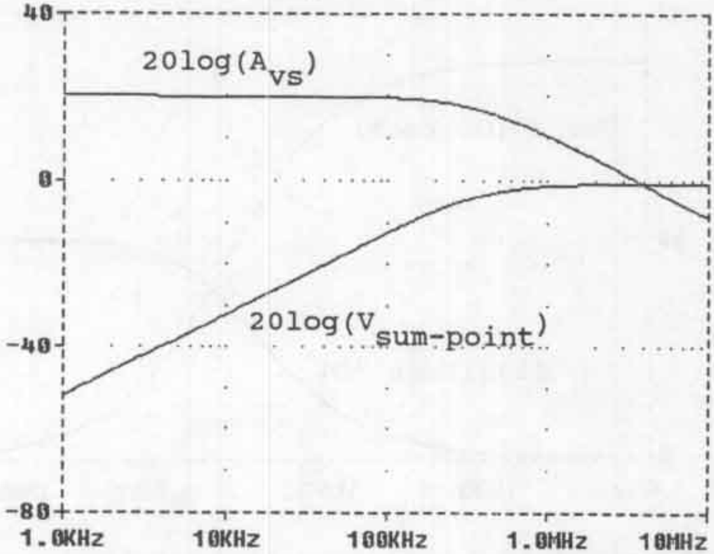
The schematic is stored in file P2_66. Plots of the gains versus frequency are:



Usually a gain curve that displays a high peak such as the curve for part b is not desirable. For example if these were amplifiers for audio signals, amplifier b would amplify the low notes out of proportion to higher notes.

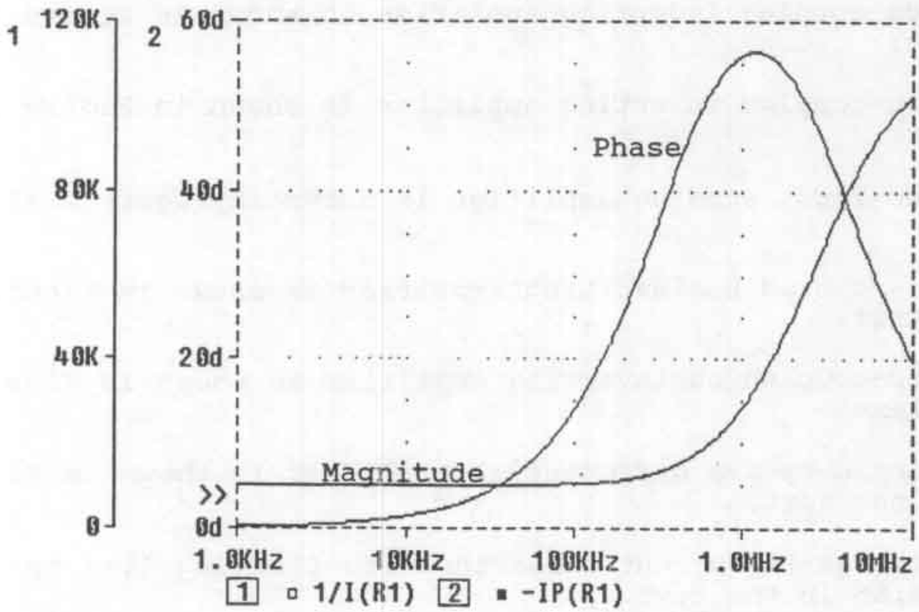
Problem 2.67

The simulation is stored in file P2_67. Plots of $20\log(A_{vs}) = 20\log(V_{out})$ and $20\log(V_{sum\text{-}point})$ are:



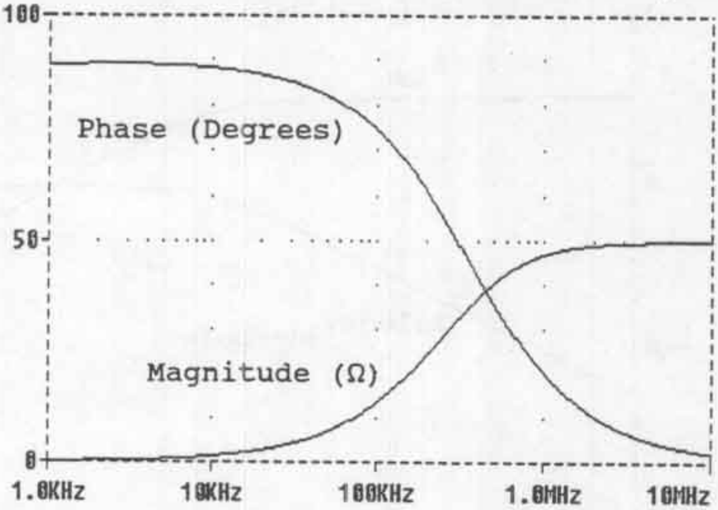
Because the source voltage is 1 V (0 dB) the voltage at the summing point must be -40 dB or less to be less than 1% of V_s. This is true for frequencies less than about 4 kHz.

Plots of the input impedance magnitude and phase are:



At low frequencies the input impedance is 10 kΩ resistive as predicted by the theory for an ideal op amp. However at higher frequencies the input impedance becomes capacitive and larger in magnitude.

Plots of the output impedance magnitude and phase are:



The ideal-op amp analysis predicts zero output impedance. The actual output impedance is very low at low frequencies but approaches 50 Ω resistive at high frequencies.

Problem 2.68

(a) A dc-coupled inverting amplifier is shown in Figure 2.47 in the text.

(b) An ac-coupled inverting amplifier is shown in Figure 2.48 in the text.

(c) A two-input summing amplifier is shown in Figure 2.49 in the text.

(d) A dc-coupled noninverting amplifier is shown in Figure 2.50 in the text.

(e) An ac-coupled noninverting amplifier is shown in Figure 2.51 in the text.

(f) A single-op-amp differential amplifier is shown in Figure 2.53 in the text.

(g) A voltage-to-current converter with floating load is shown in Figure 2.55 in the text.

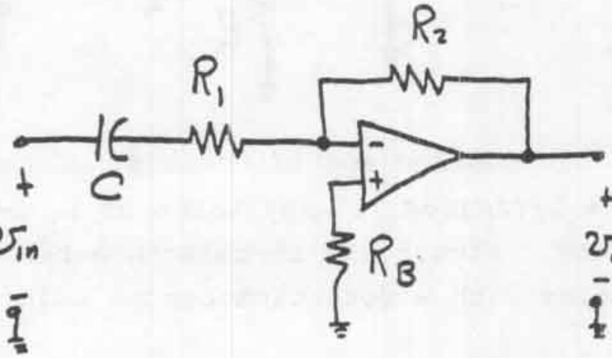
(h) A current-to-voltage converter is shown in Figure 2.57 in the text.

(i) A current amplifier is shown in Figure 2.58 in the text.

Problem 2.69

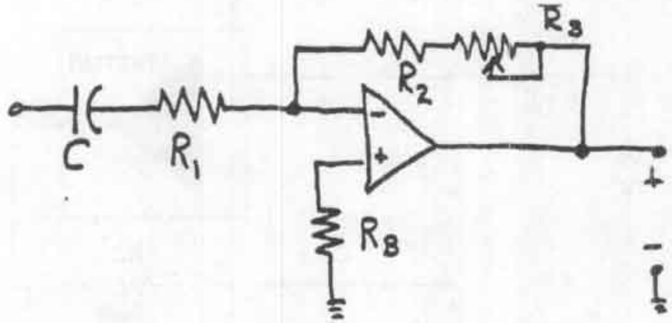
Many correct answers exist. Here are two solutions:

Solution 1



In this circuit use 1%-tolerance resistors. We need $R_2 = 10 R_1$, $R_B = R_2$, If we choose the capacitance such that $C > 1/(2\pi 100 R_1)$ we will find in the simulation that the gain is within 5% of the desired value at 1 kHz. One suitable choice of component values is $R_1 = 20$ kΩ, $R_2 = R_B = 200$ kΩ, C = 0.1 μF, and the LF411 op amp.

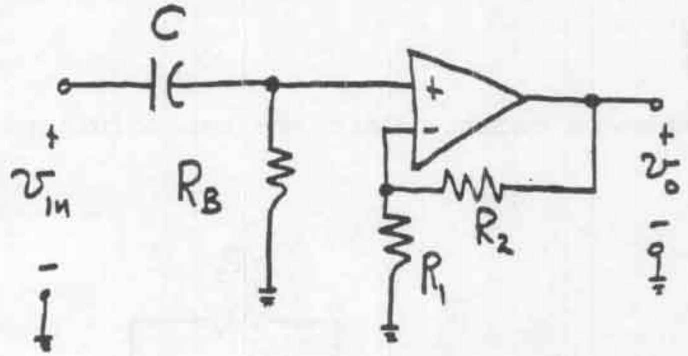
Solution 2



In this circuit use 5%-tolerance resistors and adjust the gain to within 5% by use of the potentiometer. Use the LF411 op amp, $R_1 = 20$ kΩ ± 5%, $R_2 = 180$ kΩ ± 5%, C = 0.1 μF, $R_3 = 50$ kΩ potentiometer, and $R_B = 200$ kΩ ±5%.

Problem 2.70

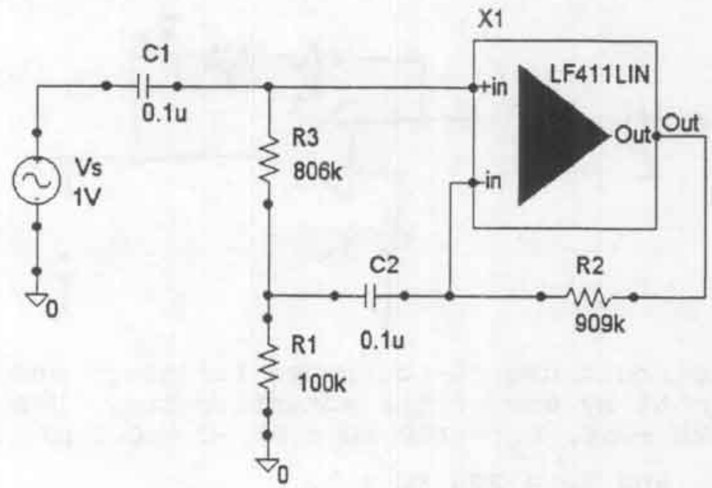
Many correct answers exist. Here is one of them:



To achieve the desired specifications, we need $R_2 = 9R_1$, $R_B = R_1 || R_2$, and $C \geq 1/(2\pi 100 R_B)$. Any value of R_1 between 1 kΩ and 100 kΩ is suitable. Either use 1%-tolerance resistors or use 5%-tolerance resistors with a potentiometer to adjust the gain magnitude.

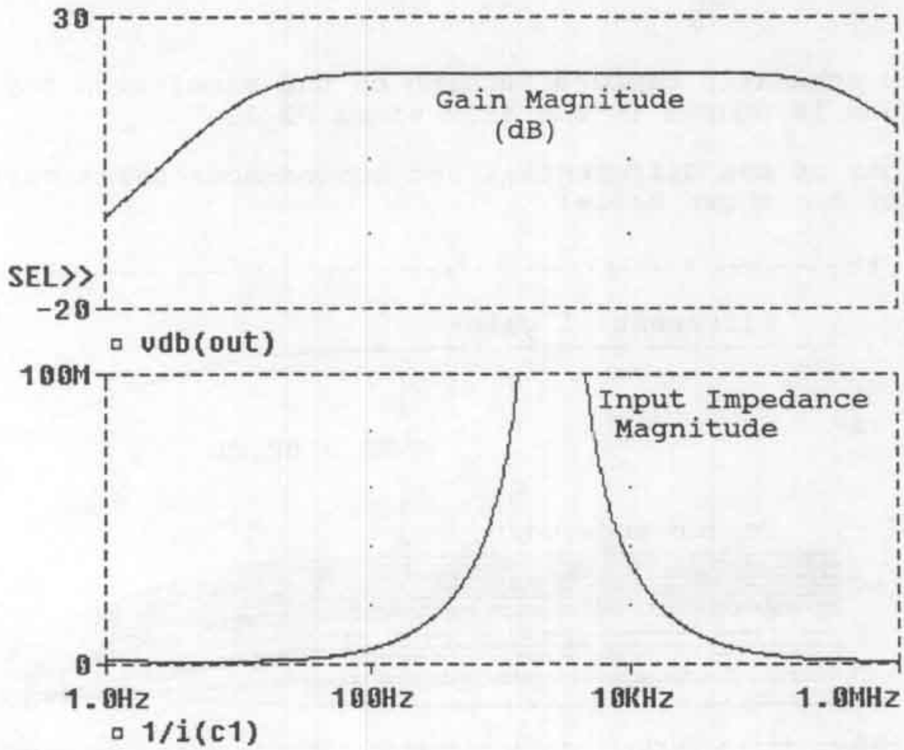
Problem 2.71

Resistors of 20 MΩ or more are usually impractical. Thus we need to select a circuit that makes a smaller resistance appear large. One approach is to use a circuit similar to Figure 2.52 in the text:



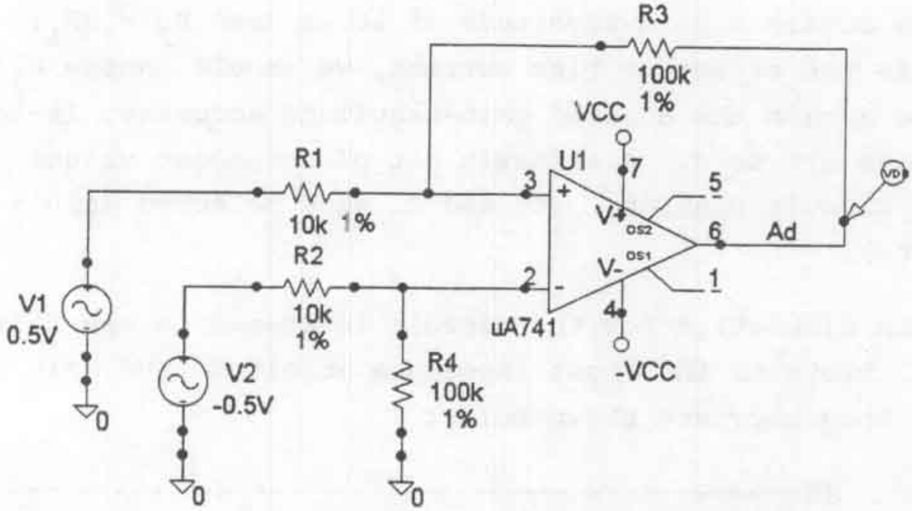
To attain a gain magnitude of 10 we need $R_2 = 9R_1$. To minimize the effect of bias current, we should choose $R_1 + R_3 = R_2$. To attain the desired gain-magnitude accuracy, 1%-tolerance resistors are used. A suitable set of component values is shown on the circuit diagram. (C_1 and C_2 were selected mainly by trial and err.)

The simulation for the circuit is stored in the file named P2_71. Plots of the input impedance magnitude and gain magnitude versus frequency are shown below:



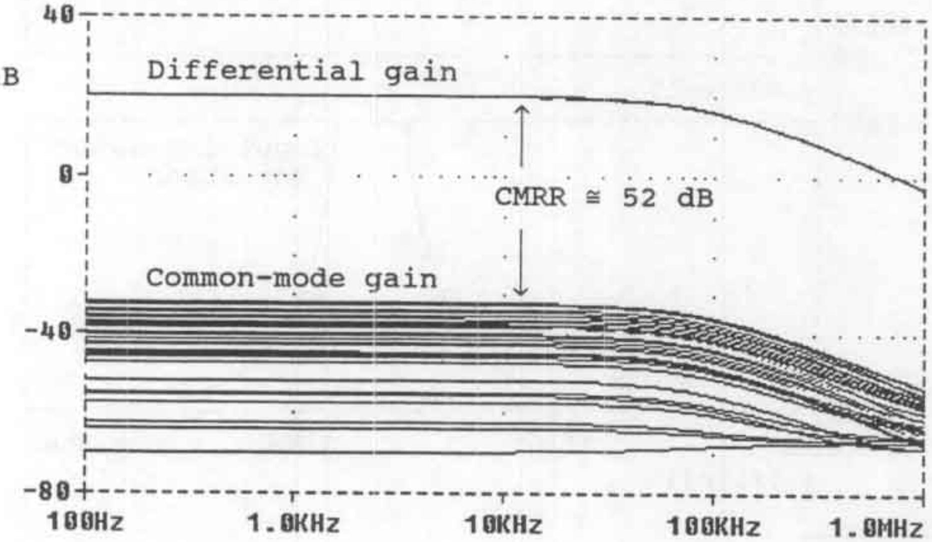
Problem 2.72

Here is the circuit and a suitable set of component values:



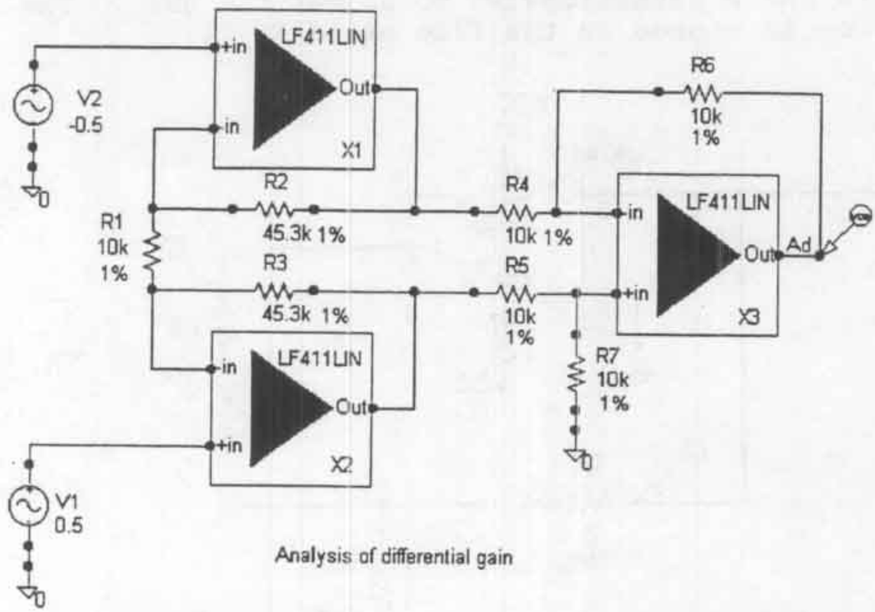
The schematic capture version of the simulation for 40 Monte Carlo runs is stored in the file named P2_72.

Plots of the differential and common-mode gains versus frequency are shown below:



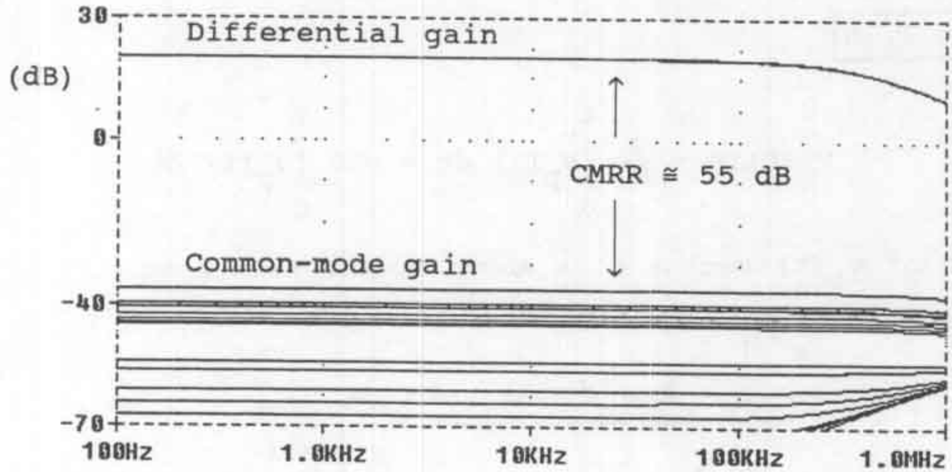
Problem 2.73

The circuit diagram is shown below. Choose R_1 in the range from 1 kΩ to 200 kΩ. To attain a gain of 10 we need $R_2 = R_3 = 4.5 \times R_1$. Then choose $R_4 = R_5 = R_6 = R_7$ in the range from about 1 kΩ to 1 MΩ.



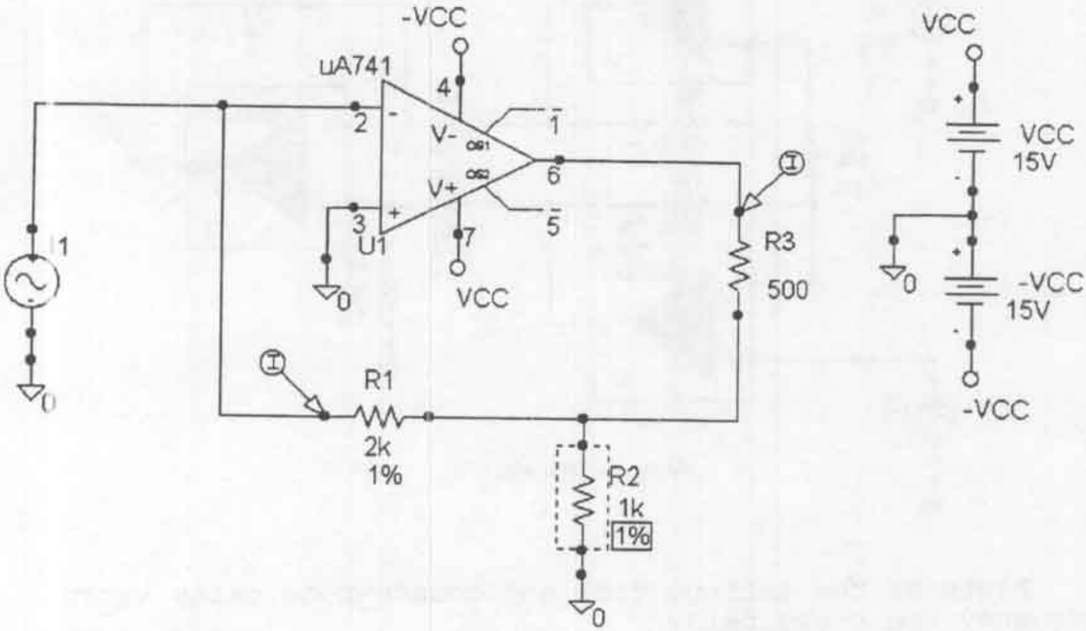
Analysis of differential gain

Plots of the differential and common-mode gains versus frequency are shown below:



Problem 2.74

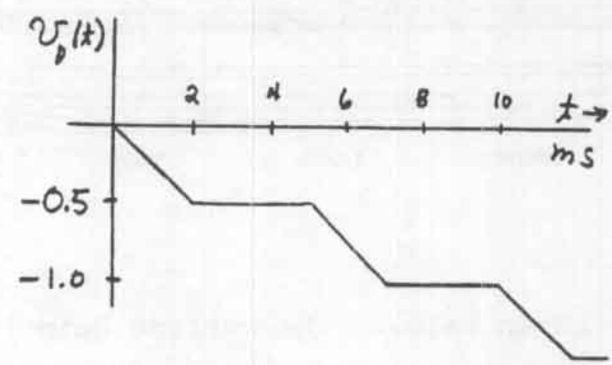
The circuit is shown below. The current gain is $A_i = -(1 + R_1/R_2)$. Thus for a current gain magnitude of 3 we need to choose $R_1 = 2R_2$. A good choice of values is $R_1 = 2\ k\Omega \pm 1\%$ and $R_2 = 1\ k\Omega \pm 1\%$. Another alternative would be to use 5%-tolerance resistors and a potentiometer to adjust the gain. The PSpice simulation is stored in the file named P2_74.



Problem 2.75

$$v_o(t) = -\frac{1}{RC}\int_0^t v_p(t)\,dt = -50\int_0^t v_p(t)\,dt$$

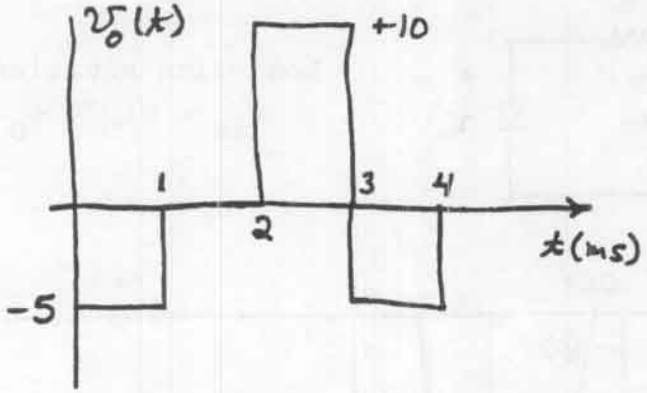
The plot of $v_o(t)$ versus t is shown on the next page.



Each input pulse reduces $v_o(t)$ by 0.5 V. Thus 20 pulses will result in $v_o(t)$ = -10 V.

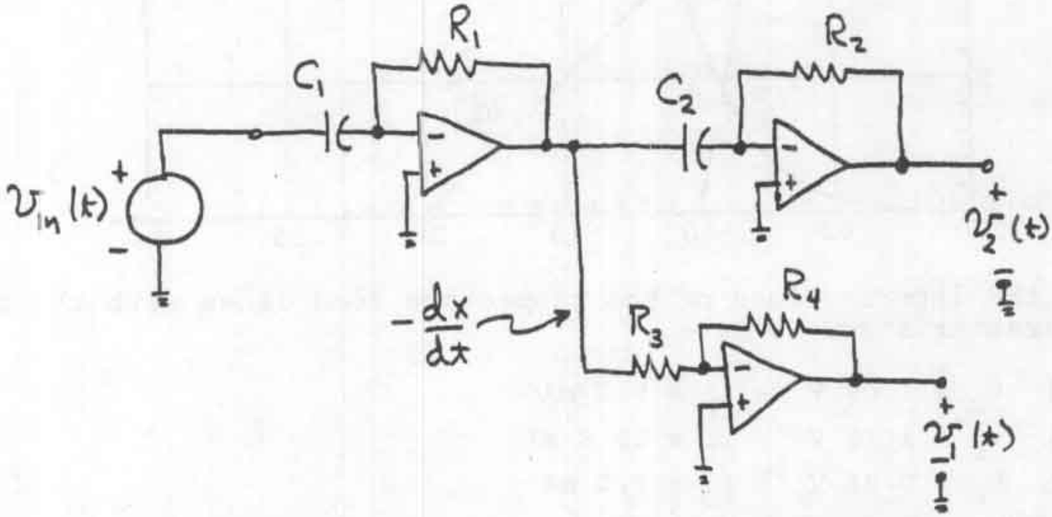
Problem 2.76

$$v_o(t) = -RC\frac{dv_{in}}{dt} = -10^{-3}\frac{dv_{in}}{dt}$$



Problem 2.77

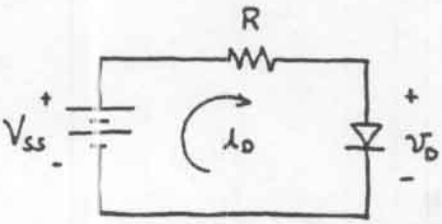
Let x(t) = displacement in meters. Then $v_{in} = 10x(t)$, and we need $v_1(t) = dx/dt = 0.1dv_{in}/dt$ and $v_2(t) = d^2x/dt^2 = dv_1/dt$.



We need $R_1C_1 = 0.1$, $R_2C_2 = 1$ and $R_3 = R_4$. Suitable values are $R_1 = R_2 = 1$ MΩ, $C_1 = 0.1$ μF, $C_2 = 1.0$ μF, and $R_3 = R_4 = 10$ kΩ. LF411 op amps are a good choice because they have relatively small bias currents.

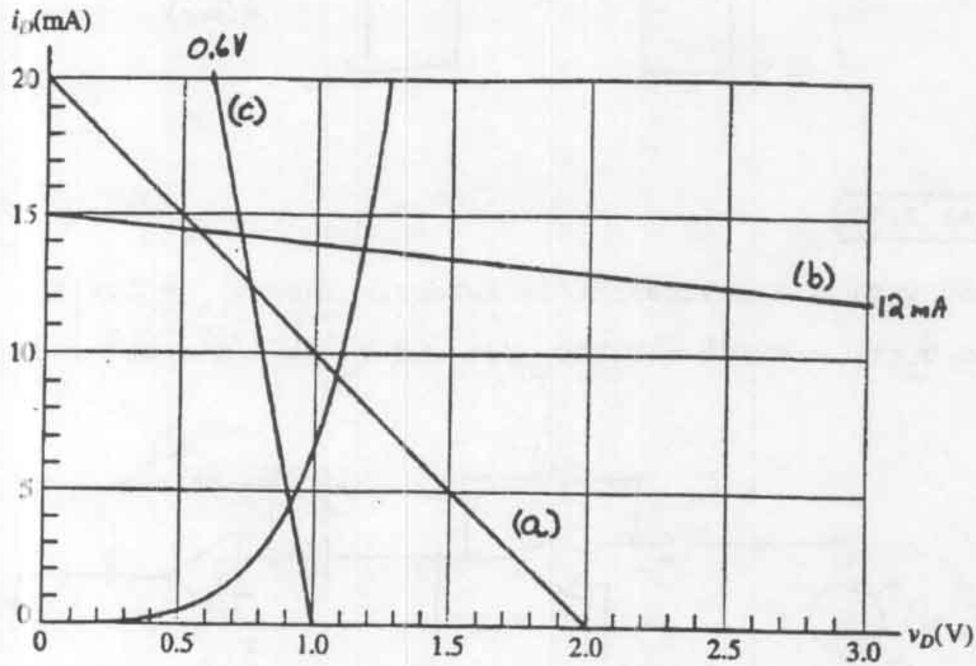
Chapter 3

Exercise 3.1



Load-line equation:

$$V_{SS} = Ri_D + v_D$$



At the intersections of the respective load lines with the diode characteristic, we have

(a) $v_D \cong 1.08$ V $\quad i_D \cong 9.2$ mA

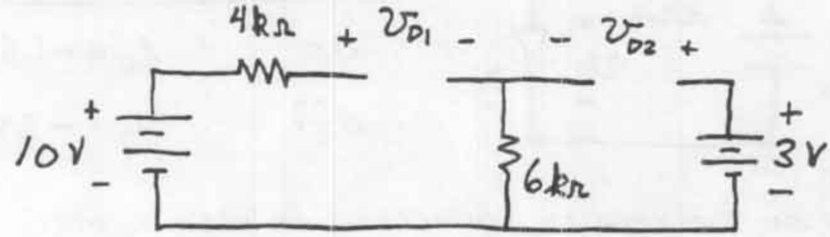
(b) $v_D \cong 1.18$ V $\quad i_D \cong 13.8$ mA

(c) $v_D \cong 0.91$ V $\quad i_D \cong 4.5$ mA

Exercise 3.2

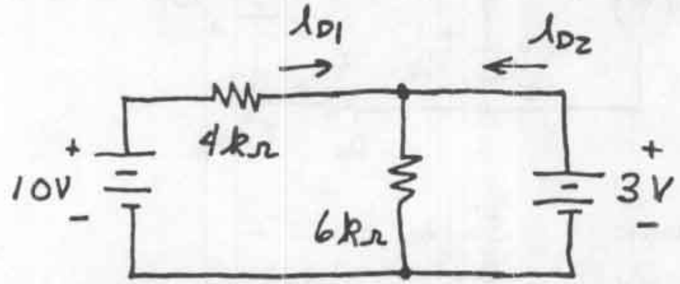
The equivalent circuit is shown on the next page. Solving for the voltages across the diodes we obtain v_{D1} = 10 V and v_{D2} =

3 V. However $v_{D1} > 0$ and $v_{D2} > 0$ are not consistent with the assumption that the diodes are off.



Exercise 3.3

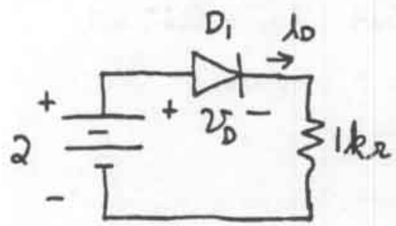
Assuming that the diodes are on, the equivalent circuit is:



Solving for the currents, we determine that $i_{D1} = (10 - 3)/4000 = 1.75$ mA and $i_{D2} = 3/6000 - i_{D1} = -1.25$ mA. However $i_{D2} < 0$ is inconsistent with the assumption that D_2 is on.

Exercise 3.4

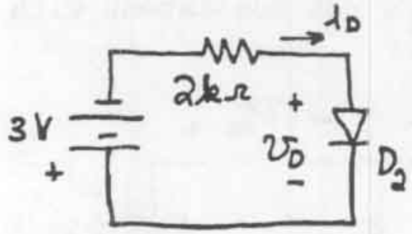
(a)



Assume D_1	Solve for v_D or i_D
on	$i_D = 2$ mA
off	$v_D = +2$ V

$v_D = +2$ is inconsistent with the assumption that D_1 is off. On the other hand, $i_D = 2$ mA is consistent with the assumption that D_1 is on. Thus we conclude that D_1 is on and $i_D = 2$ mA.

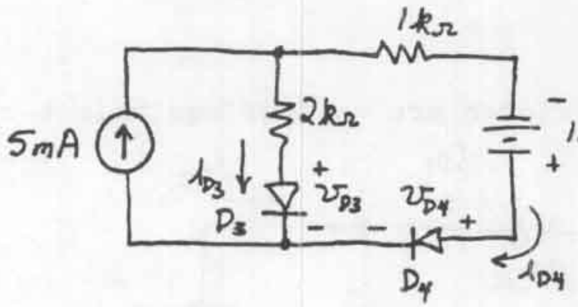
(b)



Assume D_2	Solve for v_D or i_D
on	$i_D = -1.5 mA$
off	$v_D = -3 V$

In this case the results are consistent with D_2 off.

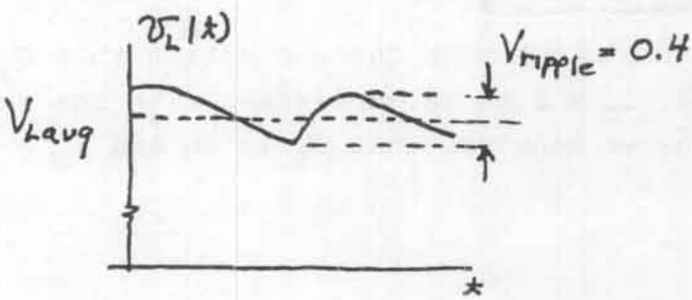
(c)



Assume D_3	Assume D_4	Solve circuit for v_D's and i_D's
off	off	impossible — no closed path for 5mA
off	on	$i_{D4} = 5mA$ $v_{D3} = -5V$
on	off	$i_{D3} = 5mA$ $v_{D4} = 20V$
on	on	$i_{D3} = -1.67mA$ $i_{D4} = 6.67mA$

Thus we conclude that D_3 is off and D_4 is on.

Exercise 3.5



$$V_{Lavg} \cong \frac{V_{Lmax} - V_{Lmin}}{2} = 15 \text{ V} \quad \Rightarrow \quad V_{Lmax} = 15.2 \text{ V}$$

$$C = \frac{I_L T}{2V_r} = \frac{0.1(1/60)}{2 \times 0.4} = 2083 \ \mu\text{F}$$

$$V_{Lmax} \cong V_{m,secondary} - 2V_{diode}$$

$$V_{m,secondary} = 15.2 + 2(0.7) = 16.6 \text{ V}$$

$$V_{m,primary} = 110\sqrt{2} = 155.6 \text{ V}$$

$$n = \frac{V_{m,primary}}{V_{m,secondary}} = \frac{155.6}{16.6} = 9.37$$

Exercise 3.6

We determine the capacitance as in Exercise 3.5 resulting in $C = 2083\ \mu\text{F}$. In this case we have $V_{m,secondary} = V_{Lmax} + V_{diode} = 15.2 + 0.7 = 15.9$ V. Then the required turns ratio is

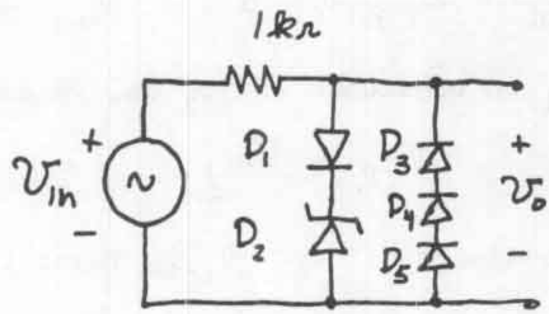
$$n = \frac{V_{m,primary}}{V_{m,secondary}}$$

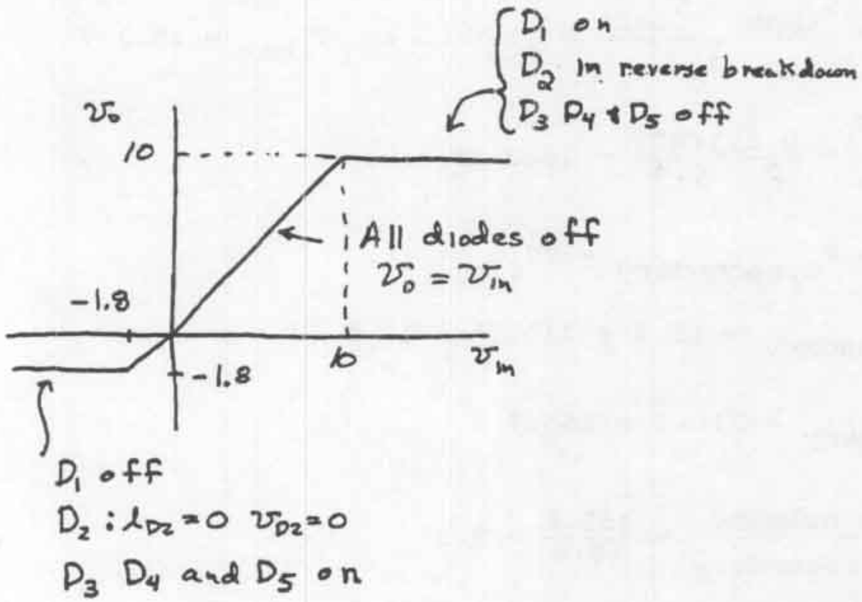
$$= \frac{155.6}{15.9}$$

$$= 9.78$$

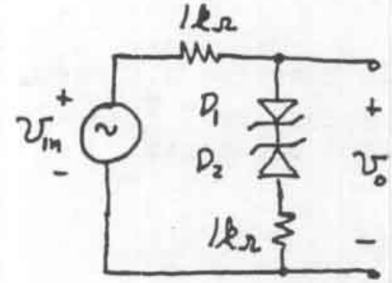
Exercise 3.7

(a)

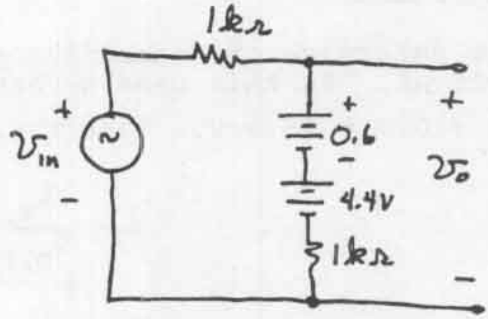




(b)



Original circuit



Equivalent circuit with D_1 on and D_2 in breakdown.

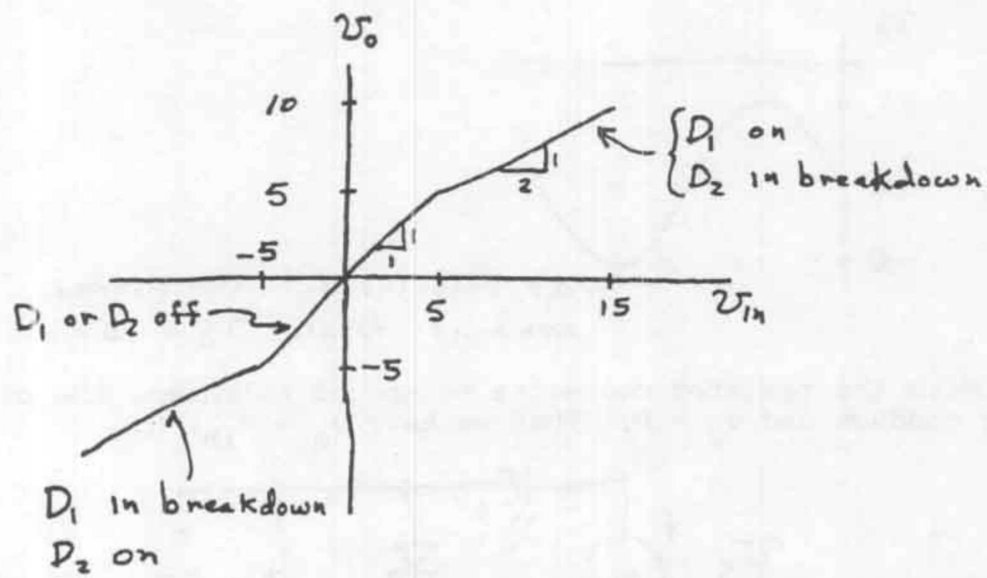
From the equivalent circuit we have

$$\frac{v_o - 5}{1\ k\Omega} + \frac{v_o - v_{in}}{1\ k\Omega} = 0 \quad \Rightarrow \quad v_o = \frac{v_{in} + 5}{2}$$

Similarly with D_1 in breakdown and D_2 on, we determine that

$$v_o = \frac{v_{in} - 5}{2}$$

Finally with both diodes off $v_o = v_{in}$. These results are plotted on the next page.

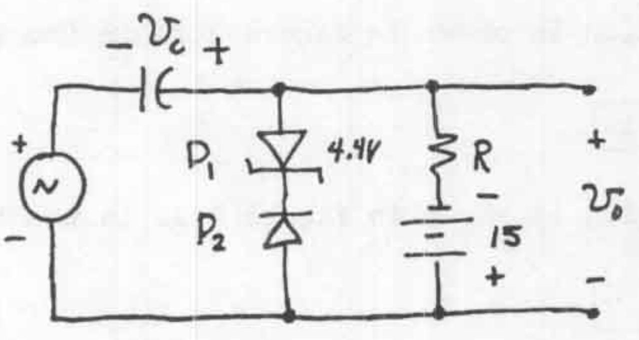


Exercise 3.8

See the answers shown in Figure 3.18 in the book.

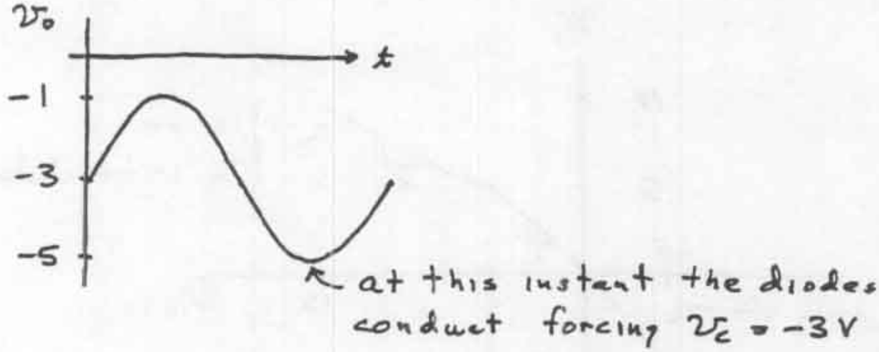
Exercise 3.9

(a)

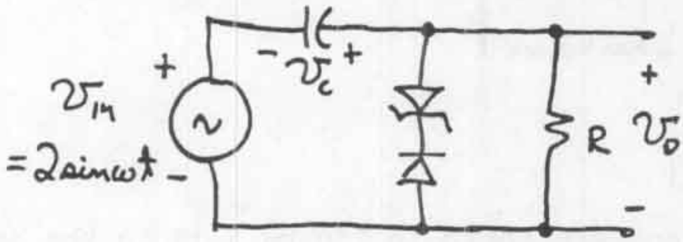


With $v_{in} = 0$, D_1 is in breakdown and D_2 is on. Thus the output voltage $v_o = -5$ V in steady-state conditions.

(b) For $v_{in} = 2\sin(\omega t)$ under steady-state conditions, the output is shown on the next page.



(c) With the resistor connected to ground as shown, the diodes never conduct and $v_c = 0$. Thus we have $v_o = v_{in}$.



Exercise 3.10

A solution is shown in Figure 3.21 in the book.

Exercise 3.11

A solution is shown in Figure 3.22 in the book.

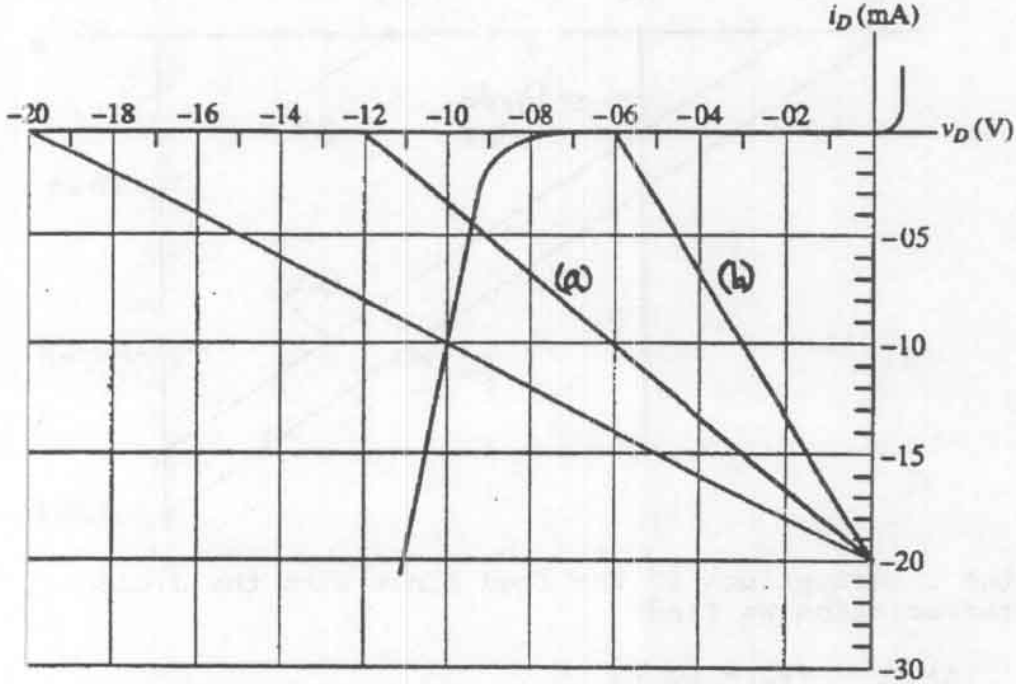
Exercise 3.12

We follow the procedure used in Example 3.5 in the book. For part (a) with R_L = 1200 Ω, we have

$$V_T = V_{SS} \frac{R_L}{R + R_L} = 24 \frac{1200}{1200 + 1200} = 12 \text{ V}$$

$$R_T = \frac{RR_L}{R + R_L} = \frac{1200 \times 1200}{1200 + 1200} = 600 \ \Omega$$

Similarly for part (b) with $R_L = 400\ \Omega$ we obtain $V_T = 6$ V and $R_T = 300\ \Omega$. Now we construct the load lines.



At the intersections of the load lines with the diode characteristics we find the answers:

(a) $v_L = -v_D \cong 9.4$ V
(b) $v_L = -v_D \cong 6.0$ V

Exercise 3.13

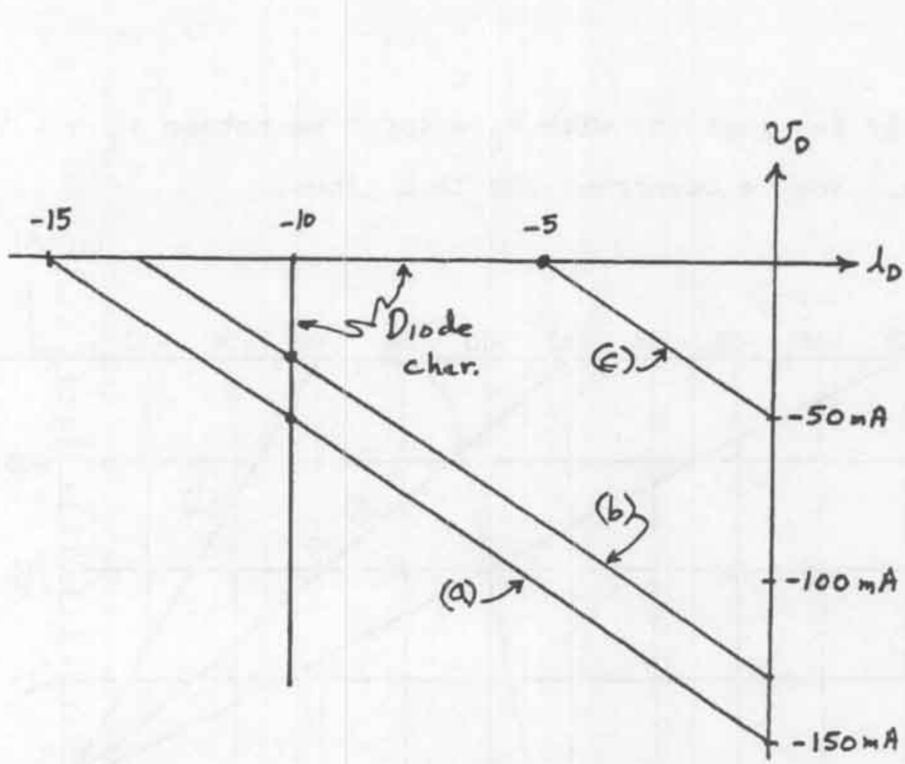
The load line equation is

$$15 = 100(i_L - i_D) - v_D$$

Substituting the values of i_L for the various parts, we have

(a) $15 = -100i_D - v_D$
(b) $13 = -100i_D - v_D$
(c) $5 = -100i_D - v_D$

We use these equations to plot the load lines as shown on the next page.



At the intersections of the load lines with the diode characteristics we find:

(a) $v_o = -v_D \cong 10$ V
(b) $v_o = -v_D \cong 10$ V
(c) $v_o = -v_D \cong 5$ V

Exercise 3.14

Equation 3.21 states: $r_d = \frac{nV_T}{I_{DQ}}$. Furthermore at a temperature of 300 K, we have $V_T \cong 26$ mV. Substituting values and evaluating, we obtain (a) $r_d = 260\ \Omega$, (b) $r_d = 26\ \Omega$, (c) $r_d = 2.6\ \Omega$.

Exercise 3.15

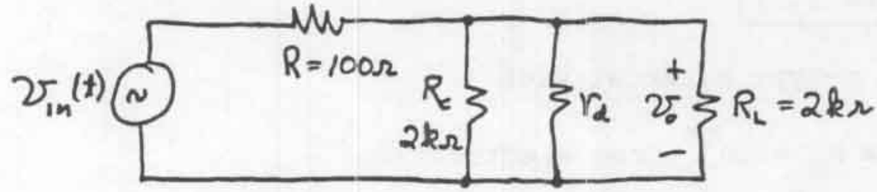
(a) First we compute the Q-point diode current. Refer to the dc circuit shown in Figure 3.34 in the book.

$$I_{DQ} \cong \frac{V_C - 0.6}{R_C} = \frac{1.6 - 0.6}{2\ k\Omega} = 0.5 \text{ mA}$$

Then we can determine the small-signal resistance of the diode:

$$r_d = \frac{nV_T}{I_{DQ}} = \frac{26 \text{ mV}}{0.5 \text{ mA}} = 52\ \Omega$$

Assuming that the input signal is ac and that the impedance of the capacitor is negligible for the signal frequencies, the small-signal equivalent circuit is:



$$A_v = \frac{v_o}{v_{in}} = \frac{R_p}{R + R_p} \quad \text{where } R_p = R_C||R_L||r_d = 49.4\ \Omega$$

Evaluating we find that $A_v = 0.331$

(b) Using the same approach as in part (a) we find $I_{DQ} = 5$ mA, $r_d = 5.2\ \Omega$, $R_p = 5.17\ \Omega$ and $A_v = 0.0492$

Exercise 3.16

Because $v_D > 0.1$ V, we have $i_D \cong I_s\exp(v_D/nV_T)$. Solving for I_s, we have $I_s = i_D/\exp(v_D/nV_T) = (0.1 \times 10^{-3})/\exp(0.6/0.026) = 9.50 \times 10^{-15}$ A. Then for $v_D = 0.65$, we have

$$i_D = I_s\exp(v_D/nV_T) = 9.50 \times 10^{-15}\exp(0.65/0.026) = 0.684 \text{ mA}$$

and for $v_D = 0.7$ we have

$$i_D = I_s\exp(v_D/nV_T) = 9.50 \times 10^{-15}\exp(0.70/0.026) = 4.68 \text{ mA}$$

Exercise 3.17

Suppose that for v_{D1} we have a current of i_{D1} and at $v_{D2} = v_{D1} + \Delta v_D$ the current is $i_{D2} = 2i_{D1}$ then we can write:

$$i_{D2} = I_s\exp[(v_{D1} + \Delta v_D)/nV_T] = 2i_{D1} = 2I_s\exp(v_{D1}/nV_T)$$

$$I_s\exp(v_{D1}/nV_T)\exp(\Delta v_D/nV_T) = 2I_s\exp(v_{D1}/nV_T)$$

$$\exp(\Delta v_D/nV_T) = 2$$

$$\Delta v_D = nV_T \ln(2) = 18 \text{ mV}$$

Similarly for $i_{D2} = 10 i_{D1}$ we find $\Delta v_D = nV_T \ln(10) = 59.9$ mV

Exercise 3.18

We have n-type material with

$$n \cong N_D = 10^{16} \text{ free electrons/cm}^3$$

$$pn = n_i^2$$

$$p = n_i^2/n = (1.45 \times 10^{10})^2/10^{16} = 2.1 \times 10^4 \text{ holes/cm}^3$$

Exercise 3.19

$$\varepsilon = \varepsilon_r \varepsilon_0 = 11.9 \times 8.85 \times 10^{-12} = 1.05 \times 10^{-10} \quad \text{F/m}$$

$$d = \frac{\varepsilon A}{C} = \frac{1.05 \times 10^{-10} \times (20 \times 10^{-6} \times 30 \times 10^{-6})}{10^{-12}}$$

$$d = 6.32 \times 10^{-8} \text{ m}$$

Exercise 3.20

$$C_j = \frac{C_{j0}}{[1 - (V_{DQ}/\phi_0)]^m} = \frac{5 \text{ pF}}{[1 - (V_{DQ}/0.8)]^{0.5}}$$

(a) $$C_j = \frac{5 \text{ pF}}{[1 - (-5/0.8)]^{0.5}} = 1.86 \text{ pF}$$

(b) $$C_j = \frac{5 \text{ pF}}{[1 - (-50/0.8)]^{0.5}} = 0.627 \text{ pF}$$

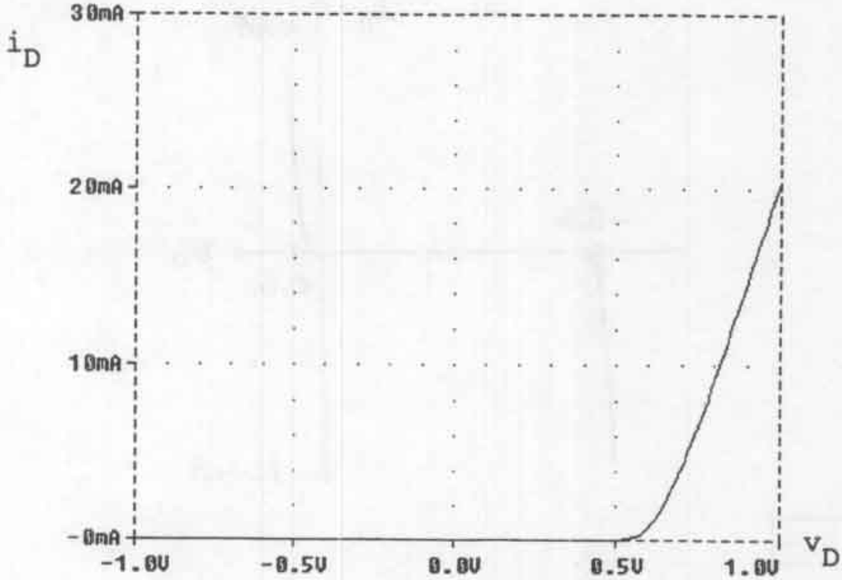
Exercise 3.21

$$r_d = \frac{nV_T}{I_{DQ}} = \frac{1(0.026)}{5 \times 10^{-3}} = 5.2 \ \Omega$$

$$C_{dif} = \frac{\tau_T I_{DQ}}{V_T} = \frac{10 \times 10^{-9} \times 5 \times 10^{-3}}{26 \times 10^{-3}} = 1920 \text{ pF}$$

Exercise 3.22

The simulation is stored in the file named Exer3_22. The resulting diode characteristic is:



Exercise 3.23

The simulation is stored in the file named Exer3_23. Results may vary from those shown in Figure 3.53 depending on the model used for the diode.

Problem 3.1

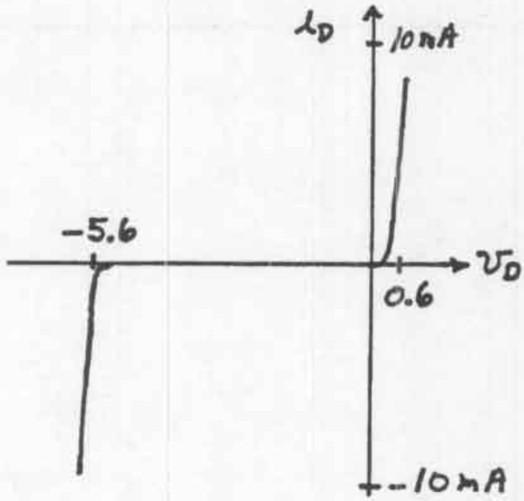
See Figure 3.1a in the book.

Problem 3.2

See Figures 3.1b and 3.2 in the book.

Problem 3.3

A Zener diode is a diode that is intended to be operated in reverse breakdown. It is used as a voltage reference. They are also called breakdown diodes or avalanche diodes (although strictly speaking avalanche diodes and zener diodes are distinct because breakdown is due to different physical mechanisms). A sketch of the volt-ampere characteristic for a 5.6-V Zener diode is:



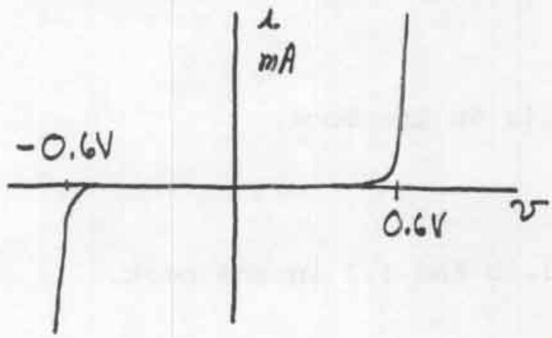
Problem 3.4

$$v_D = 0.6 - 2 \times 10^{-3} \times (175 - 25)$$

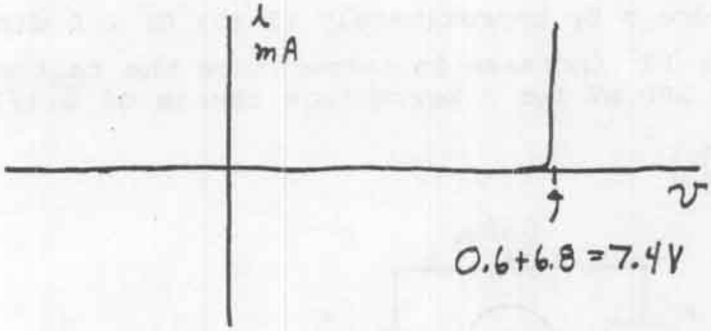
$$= 0.3 \text{ V}$$

Problem 3.5

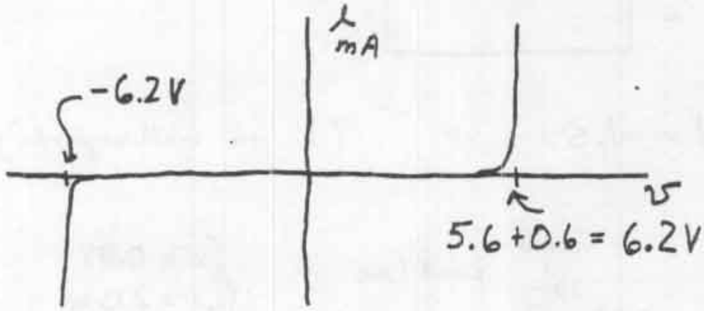
(a)



(b)



(c)



Problem 3.6

At 70° the reverse diode current is $i_R = v_o/R = 0.5/10^6 =$ 500 nA.

At 50° the current is 500 nA/4 = 125 nA and v_o = 0.125 V.

At 100° the current is (500 nA) × 2^3 = 4 μA and v_o = 4 V.

Problem 3.7

As the diode heats up, its forward voltage decreases by approximately 2 mV/°C. Thus the increase in temperature is ΔT = (0.65 V - 0.45 V)/(2 mV) = 100°. The final diode temperature is $T_{final} = T_{start} + \Delta T$ = 125°C.

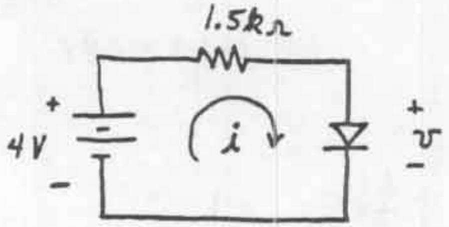
Problem 3.8

Assuming a forward drop of 0.6 V for each diode, five diodes must be placed in series to obtain a reference voltage of 3 V.

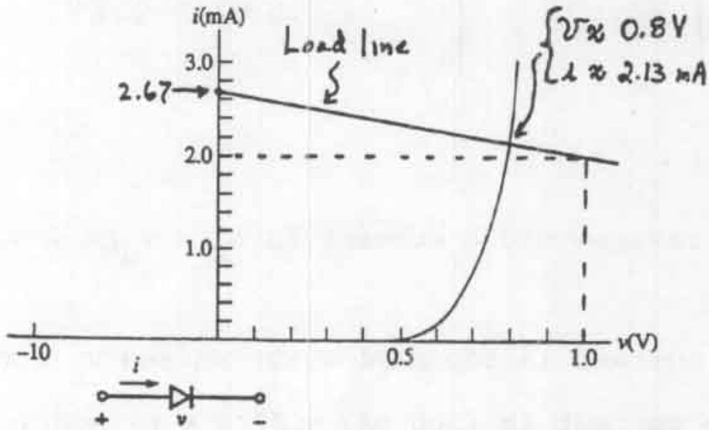
The voltage drops by approximately (2 mV/°C) × 5 diodes = 10 mV/°C. For a 10° increase in temperature the reference voltage decreases by 100 mV for a percentage change of 0.1/3 = 3.33%.

Problem 3.9

(a)

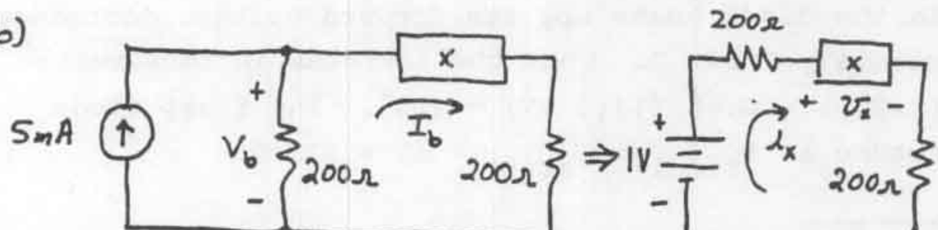


$$4 = 1.5i + v \qquad (i \text{ in milliamperes})$$

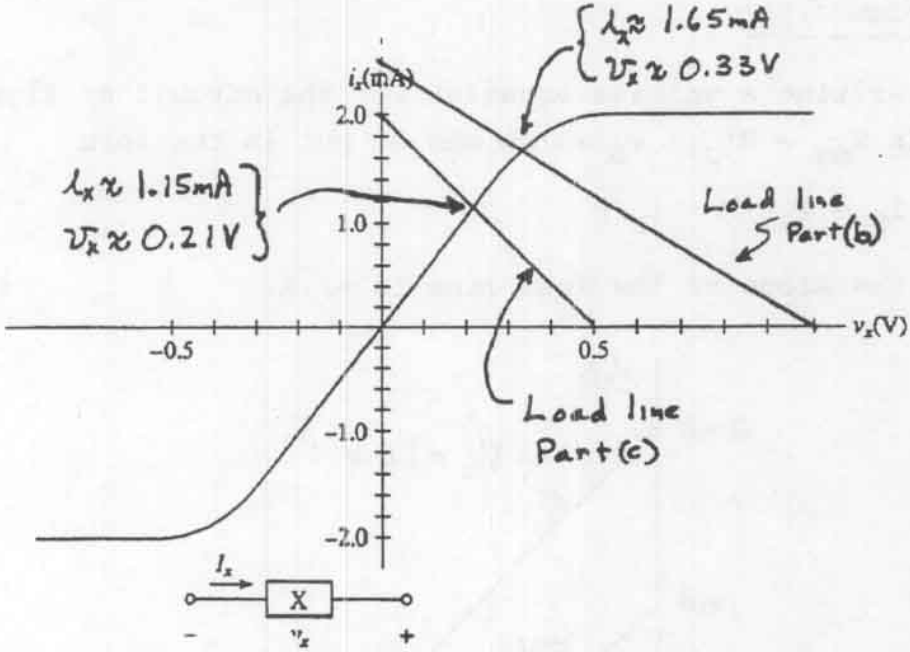


$$V_a = v \approx 0.8\text{V} \qquad I_a = i \approx 2.13\text{mA}$$

(b)

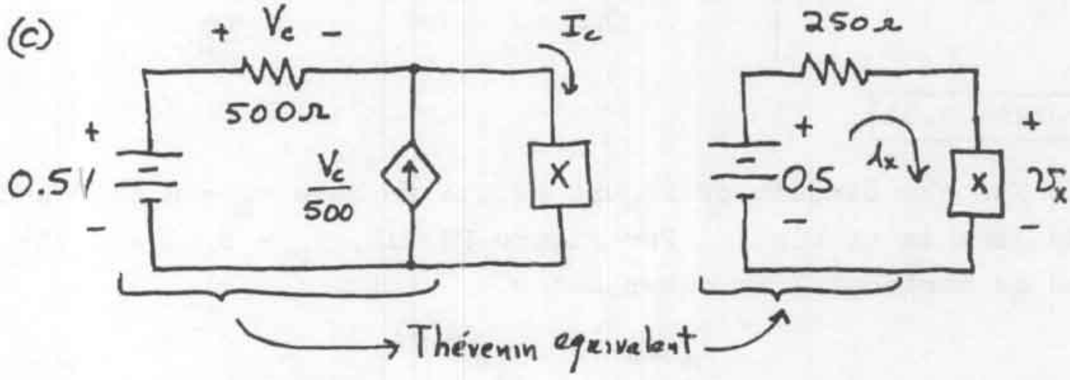


$$1\text{V} = 400 i_x + v_x \qquad (i_x \text{ in amperes})$$



$I_b = i_x \approx 1.65\,mA \qquad V_b = v_x + 200 i_x \approx 0.66\,V$

(c)



$0.5 = 250 i_x + v_x$ See Load line above.

$I_c = i_x \approx 1.15\,mA$

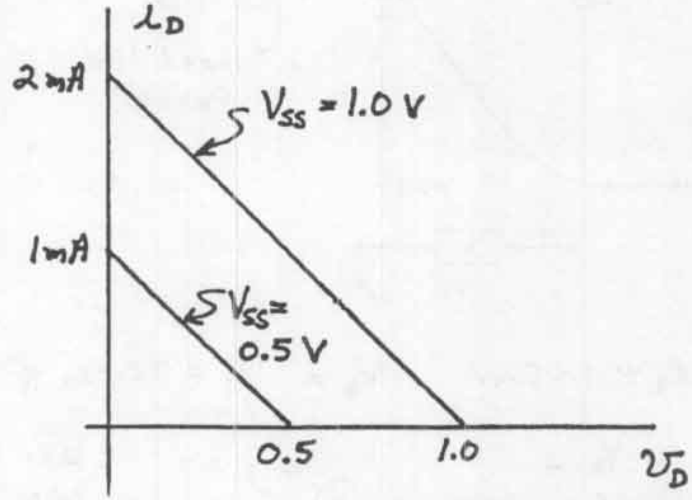
$V_c = 0.5 - v_x \approx 0.29$

Problem 3.10

Writing a voltage equation for the circuit of Figure 3.4, we obtain $V_{SS} = Ri_D + v_D$ which can be put in the form

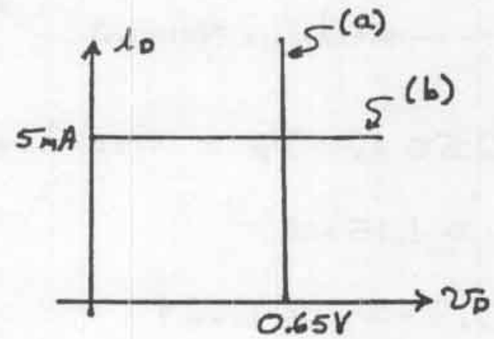
$i_D = V_{SS}/R - i_D/R$

Thus the slope of the load line is -1/R.



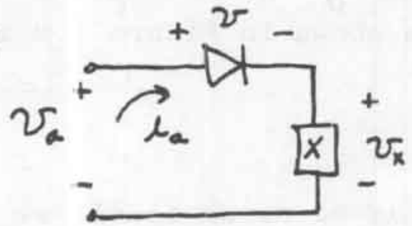
Problem 3.11

For the circuit of Figure P3.11a we have v_D = 0.65 V and the load line is vertical. For Figure P3.11b, i_D = 5 mA and the load line is horizontal as shown below.



Problem 3.12

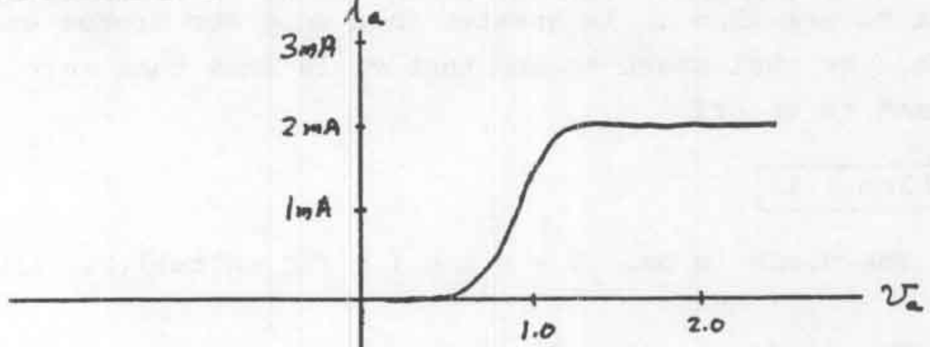
(a)



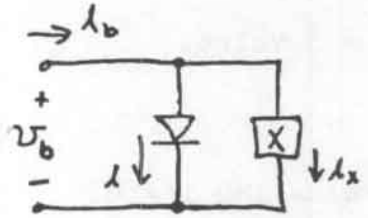
$$i_a = i = i_x$$

$$v_a = v + v_x$$

For each value of i_a add voltages.



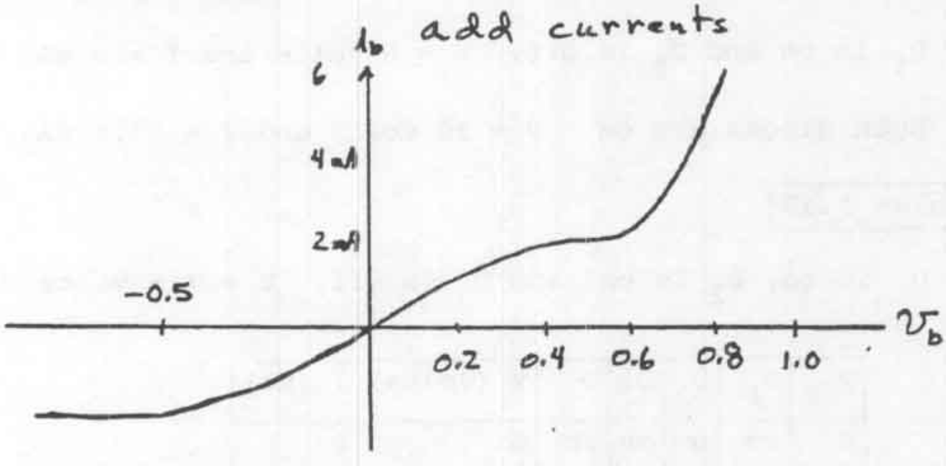
(b)



$$v_b = v = v_x$$

$$i_b = i + i_x$$

For each value of v_b add currents



Problem 3.13

The ideal diode model has $v_D = 0$ if $i_D \geq 0$, and $i_D = 0$ if $v_D \leq 0$. The volt-ampere characteristic is shown in Figure 3.8 in the book.

Problem 3.14

After solving a circuit using the ideal diode model, we must check to see that i_D is greater than zero for diodes assumed to be on. We must check to see that v_D is less than zero for diodes assumed to be off.

Problem 3.15

(a) The diode is on. $V = 0$ and $I = (10 \text{ volts})/(2.7 \text{ k}\Omega) = 3.70$ mA.

(b) The diode is off. $I = 0$ and $V = 10$ volts.

(c) The diode is on. $V = 0$ and $I = 0$.

(d) The diode is on. $I = 5$ mA and $V = 5$ volts.

Problem 3.16

(a) D_1 is on and D_2 is off. $V = 10$ volts and $I = 0$.

(b) D_1 is on and D_2 is off. $V = 6$ volts and $I = 6$ mA.

(c) Both diodes are on. $V = 30$ volts and $I = 33.6$ mA.

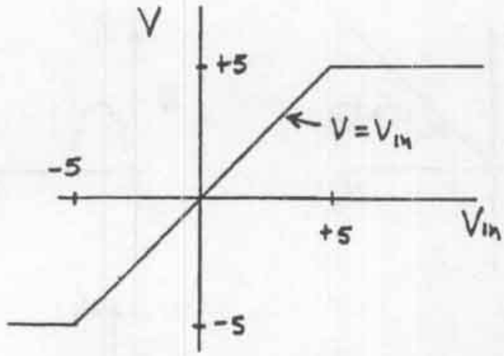
Problem 3.17

(a) D_1 is on, D_2 is on, and D_3 is off. $V = 7.5$ volts and $I = 0$.

(b)

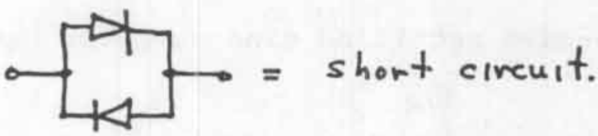
V_{in}	D_1	D_2	D_3	D_4	V (volts)	I (mA)
0	on	on	on	on	0	0
2	on	on	on	on	2	2
6	off	on	on	off	5	5
10	off	on	on	off	5	5

Plotting V versus V_{in}, we have

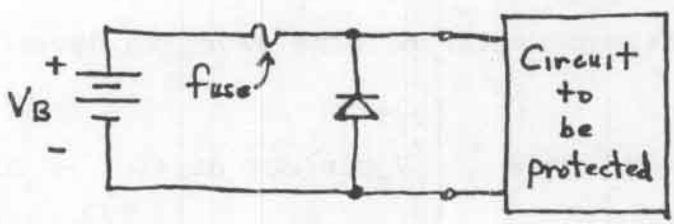


Problem 3.18

Assuming ideal diodes we have:



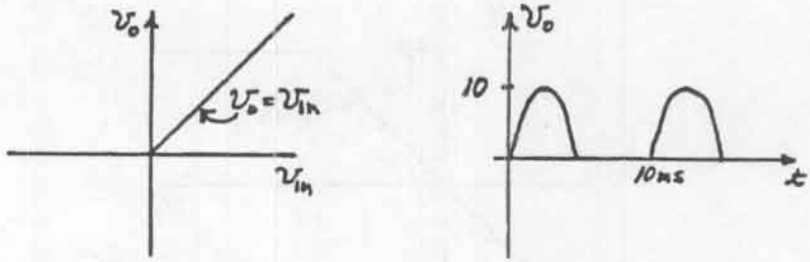
Problem 3.19



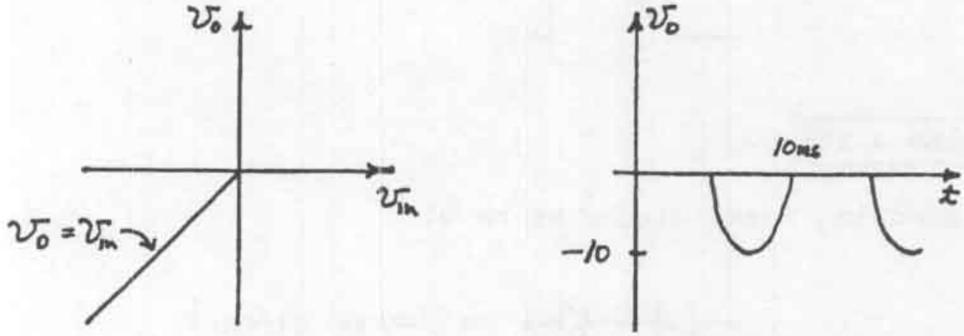
If the polarity of V_B is reversed, the diode is forward biased and draws a large current. Then the fuse blows protecting the circuit from a reverse polarity supply voltage.

Problem 3.20

(a)



(b)



Problem 3.21

(a) For a half-wave rectified sine wave, we have:

$$V_{avg} = \frac{1}{T}\int_0^T v(t)\ dt = \frac{1}{T}\int_0^{T/2} V_m \sin(\omega t)\ dt = \frac{V_m}{\omega T}\Big[-\cos(\omega t)\Big]_0^{T/2} = \frac{2V_m}{2\pi} = \frac{V_m}{\pi}$$

(We have used the fact that $\omega T = 2\pi$.)

(b) For a full-wave rectified sine wave, we have:

$$V_{avg} = \frac{1}{T}\int_0^T v(t)\ dt = \frac{1}{T}\left[\int_0^{T/2} V_m \sin(\omega t)\ dt + \int_{T/2}^{T} -V_m \sin(\omega t)\ dt\right]$$

Integrating evaluating and using the fact that $\omega T = 2\pi$, we obtain

$$V_{avg} = \frac{2V_m}{\pi}$$

Problem 3.22

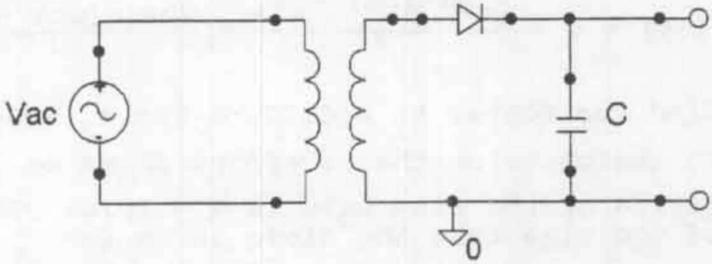
The current through the meter is a half-wave rectified sine wave with a peak amplitude of $(10\sqrt{2})/R$. As shown in Problem 3.21, the average of a half-wave rectified sine wave is its peak value divided by π. Thus we have

$$\frac{10\sqrt{2}}{R\pi} = 5 \text{ mA}$$

Solving we find $R = 900\ \Omega$.

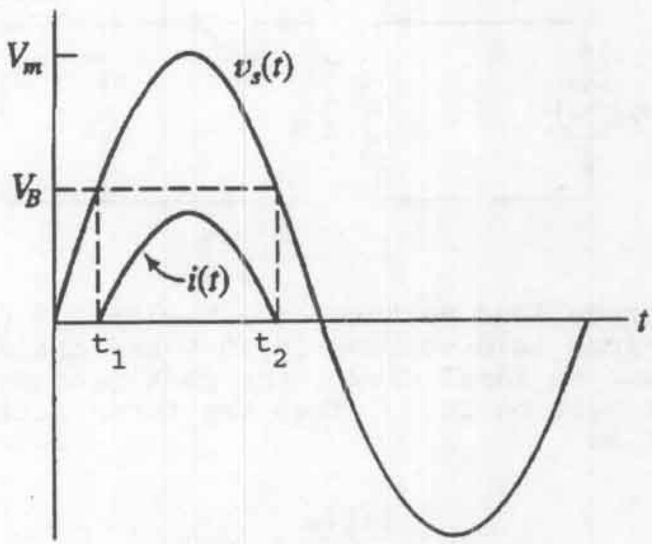
Problem 3.23

Half-wave circuit:



Full-wave circuits are shown in Figure 3.13 and 3.14 in the book except that capacitors need to be added in parallel with the loads.

Problem 3.24



Peak current flows at the instant for which $v_s(t)$ attains its maximum value. The maximum current is

$$I_{max} = \frac{V_m - V_B}{R} = \frac{20 - 14}{10} = 0.6 \text{ A}$$

As a function of time, the current is

$$i(t) = \frac{V_m \sin(\omega t) - V_B}{R}$$

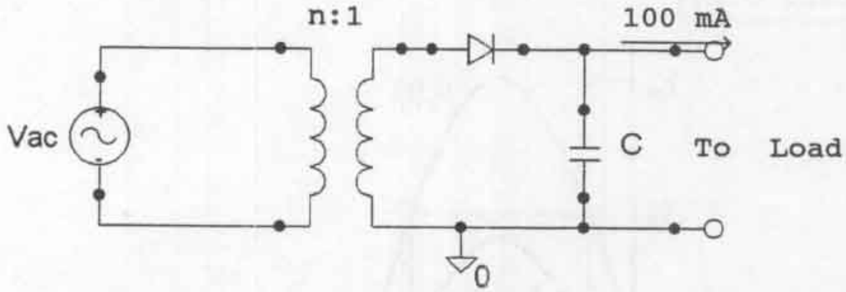
provided that this expression yields a positive result. Otherwise $i(t) = 0$. To determine the interval for which the diode is in the on state we must solve this equation:

$$i(t) = 0 = \frac{V_m \sin(\omega t) - V_B}{R} = \frac{20\sin(\omega t) - 14}{10}$$

Solving we find two roots: $t_1 = 0.775/\omega$ and $t_2 = 2.37/\omega$ radian. t_1 and t_2 are indicated on the waveforms shown on the preceding page. The period of the sine wave is $T = 2\pi/\omega$. Thus the percentage of the time that the diode is on is

$$\text{diode on} = \frac{2.37/\omega - 0.775/\omega}{2\pi/\omega} \times 100\% = 25.3\%$$

Problem 3.25



For an average load voltage of 9 V with 2-V peak-to-peak ripple, the maximum load voltage is 10 V and the minimum is 8 V. Because we assume an ideal diode, the peak secondary voltage of the transformer must be 10 V. Thus the turns ratio needed for the transformer is

$$n = \frac{110\sqrt{2}}{10} = 15.6$$

The capacitance is given by Equation 3.4 in the book.

$$C = \frac{I_L T}{V_r} = \frac{0.1(1/60)}{2} = 833\ \mu F$$

Problem 3.26

The circuit diagram is shown in Figure 3.14 in the book except for the filter capacitor which should be added in parallel with the load. For an average load voltage of 9 V with 2-V peak-to-peak ripple, the maximum load voltage is 10 V and the minimum is 8 V. Because we assume ideal diodes, the peak secondary voltage of the transformer must be 10 V. Thus the turns ratio needed for the transformer is

$$n = \frac{110\sqrt{2}}{10} = 15.6$$

The capacitance is given by Equation 3.6 in the book.

$$C = \frac{I_L T}{2V_r} = \frac{0.1(1/60)}{2(2)} = 417\ \mu F$$

Problem 3.27

The circuit diagram is shown in Figure 3.13 in the book except for the filter capacitor which should be added in parallel with the load. For an average load voltage of 9 V with 2-V peak-to-peak ripple, the maximum load voltage is $V_m = 10$ V and the minimum is 8 V. Because we assume ideal diodes, the peak voltage between the ends of the secondary winding of the transformer must be 20 V. Thus the turns ratio needed for the transformer is

$$n = \frac{110\sqrt{2}}{20} = 7.78$$

The capacitance is given by Equation 3.6 in the book.

$$C = \frac{I_L T}{2V_r} = \frac{0.1(1/60)}{2(2)} = 417\ \mu F$$

Problem 3.28

See the solution to Problem 3.25. For an average load voltage of 9 V with 2-V peak-to-peak ripple, the maximum load voltage is 10 V and the minimum is 8 V. Because we assume a diode having a forward drop of 0.8 V, the peak secondary voltage of the transformer must be 10.8 V. Thus the turns ratio needed for the transformer is

$$n = \frac{110\sqrt{2}}{10.8} = 14.4$$

The capacitance is given by Equation 3.4 in the book.

$$C = \frac{I_L T}{V_r} = \frac{0.1(1/60)}{2} = 833\ \mu F$$

Problem 3.29

The capacitance is given by Equation 3.6 in the book.

$$C = \frac{I_L T}{2V_r}$$

(a) For a source frequency of 400 Hz, we have

$$C = \frac{1(1/400)}{2(0.5)} = 2500\ \mu F$$

(b) For a source frequency of 60 Hz, we have

$$C = \frac{1(1/60)}{2(0.5)} = 16{,}700\ \mu F$$

Smaller capacitances are needed for higher frequencies. Furthermore the transformers are smaller and lighter when designed for higher frequencies. Thus power supplies designed for higher frequency operation can be smaller and lighter.

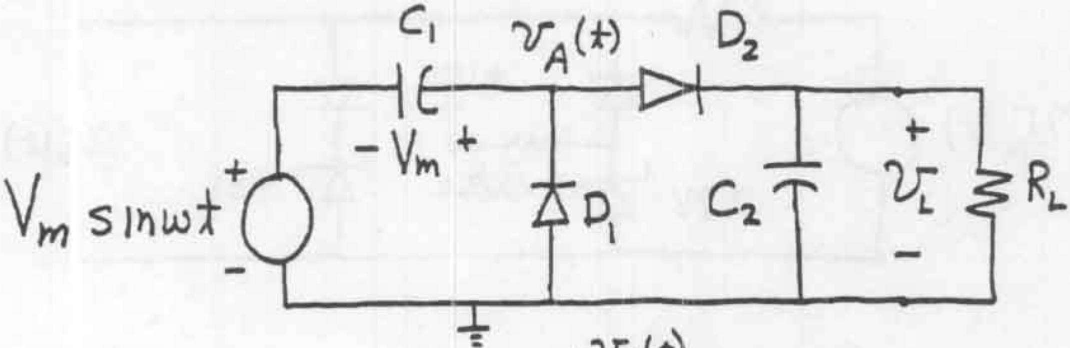
Problem 3.30

A clipper circuit removes a portion of an input signal. A typical circuit with waveforms is shown in Figure 3.15 in the book. (Many correct circuits exist for this problem.)

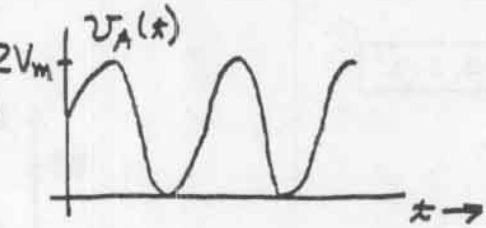
Problem 3.31

A clamp circuit adds a dc component to the input waveform such that the resulting output has a positive (or negative) peak of a specified value. Circuit examples are shown in Figures 3.19, 3.20 and 3.21 in the book.

Problem 3.32

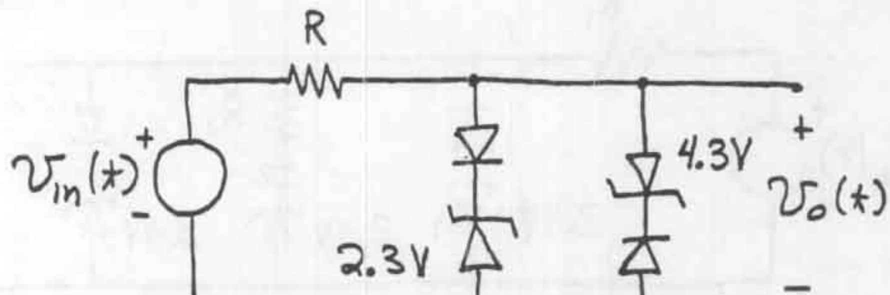


$$v_A(t) = V_m + V_m \sin(\omega t)$$



Notice that C_1 and D_1 form a clamp circuit. Furthermore, D_2 and C_2 form a peak rectifier so the load voltage is approximately equal to $2V_m$ which is why this circuit is called a voltage doubler.

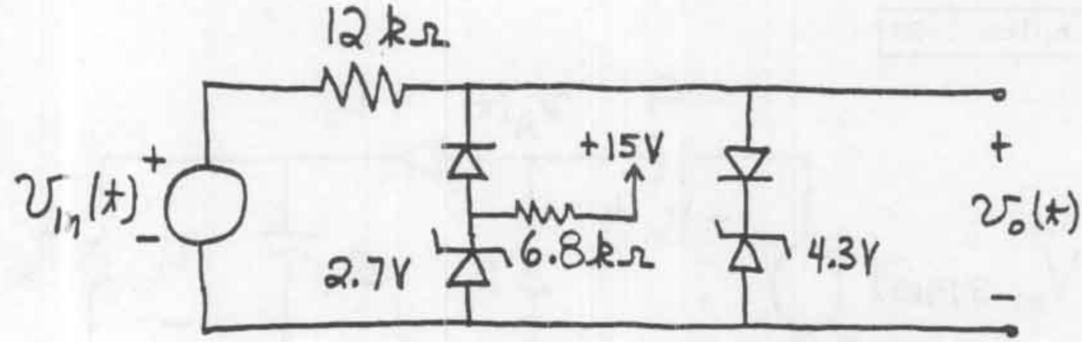
Problem 3.33



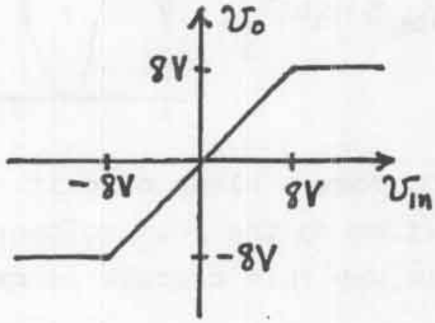
Suitable nominal resistor values are 4.7, 5.1, 5.6, 6.2, or 6.8 kΩ. Other correct answers exist for this problem.

Problem 3.34

One solution is shown on the next page. Other resistor values will work, but make sure that the 2.7 V Zener is in the breakdown region for $v_{in} = -10$ V.

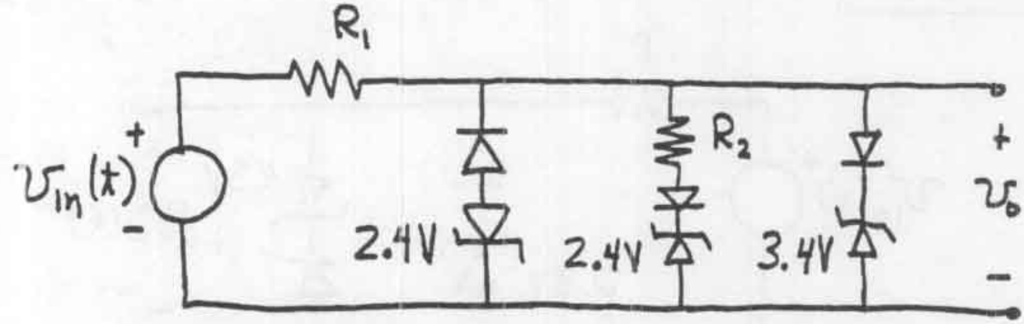


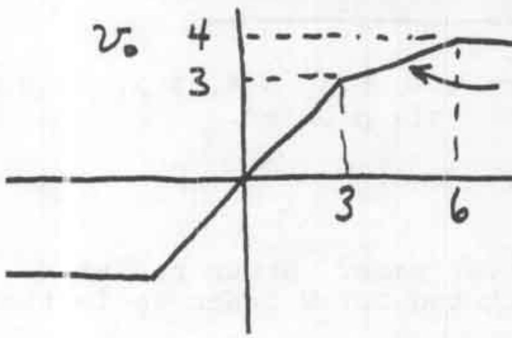
Problem 3.35



Problem 3.36

(a)



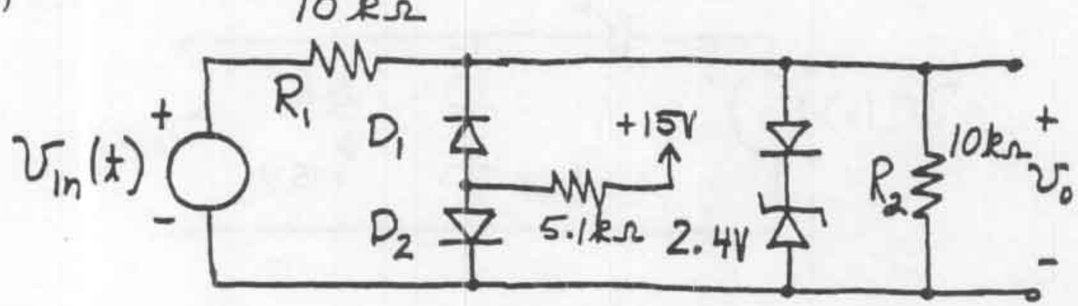


$$\text{Slope} = \frac{1}{3} = \frac{R_2}{R_1 + R_2}$$

Choose

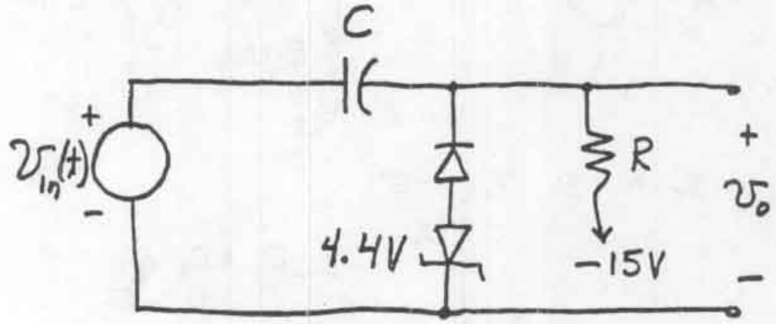
$$R_1 = 2R_2$$

(b)

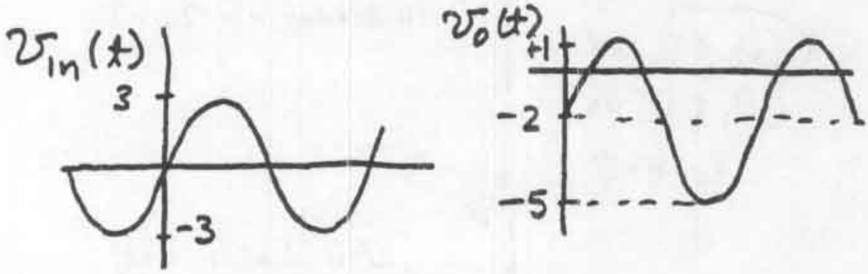


Other resistor values will work, but verify that D_2 remains forward biased for $v_{in} = -10$ V. To achieve the desired slope for the transfer characteristic, we must have $R_1 = R_2$.

Problem 3.37

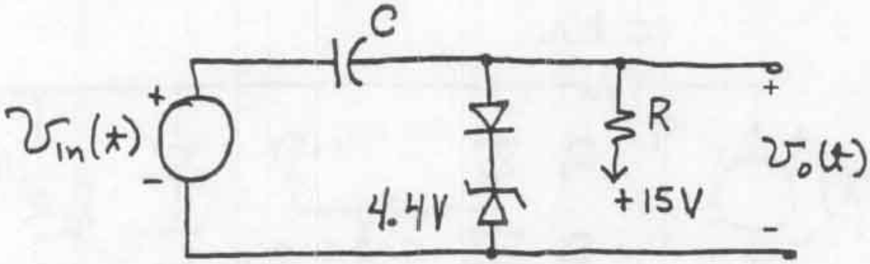


We must choose R and C so that RC >> T where T is the period of the input signal. Here are example waveforms:

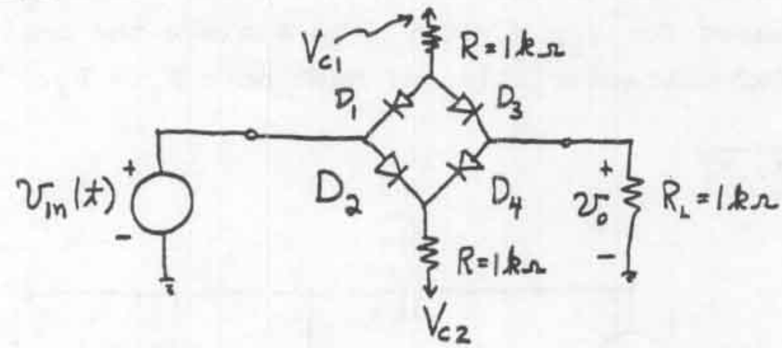


Problem 3.38

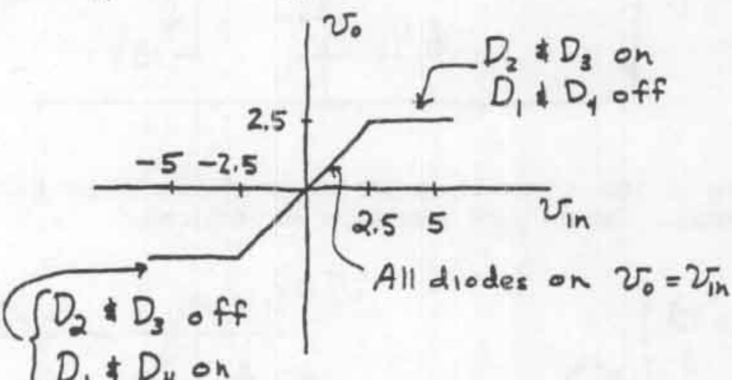
One solution is shown on the next page. Choose RC >> T where T is the period of the input signal.



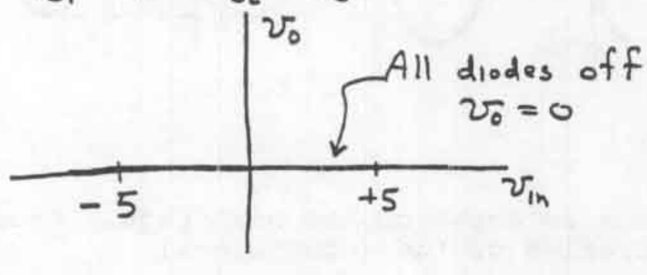
Problem 3.39



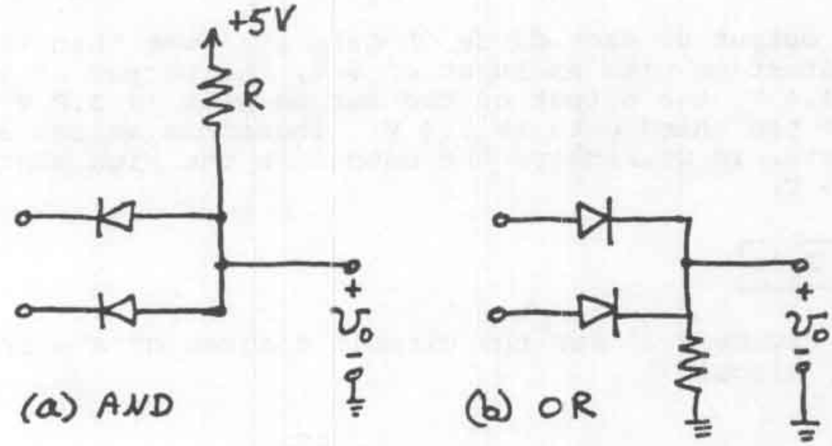
(a) $V_{C1} = +5 \quad V_{C2} = -5$



(b) $V_{C1} = -5 \quad V_{C2} = +5$



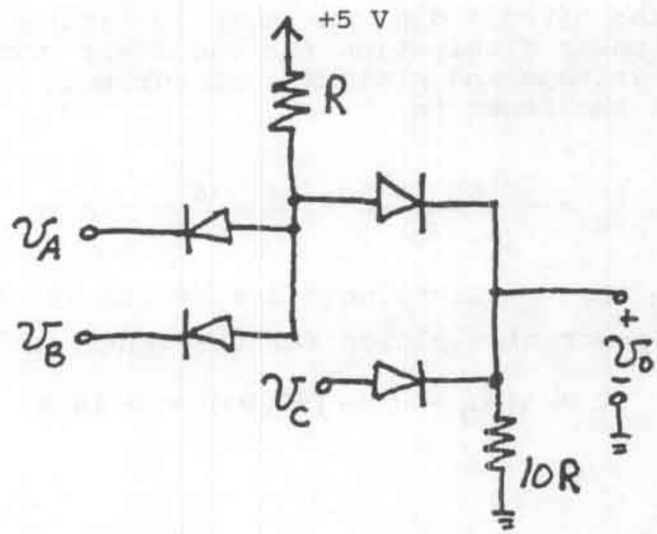
Problem 3.40



Problem 3.41

Two problems for diode logic are (1) an inverter is not possible and (2) the logic levels become closer together as signals propagate through cascaded gates.

Problem 3.42



Any value of R from about 100 Ω to 100 kΩ is suitable.

Problem 3.43

The output of each diode OR gate is lower than the input by 0.6 V. Starting with an input of 5 V, the output of the first gate is 4.4 V, the output of the second gate is 3.8 V and the output of the third gate is 3.2 V. Therefore we can cascade only two OR gates if we require the output in the high state to be at least 3.5 V.

Problem 3.44

See Figure 3.25 for the circuit diagram of a simple voltage regulator circuit.

$$\text{Source regulation} = \frac{\Delta V_{load}}{\Delta V_{SS}} \times 100\%$$

$$\text{Load regulation} = \frac{V_{no\text{-}load} - V_{full\text{-}load}}{V_{full\text{-}load}} \times 100\%$$

Problem 3.45

Refer to the circuit diagram shown in Figure 3.25 in the book. Highest power dissipation for the Zener occurs for the highest source voltage and minimum load current. Then the current through the Zener is

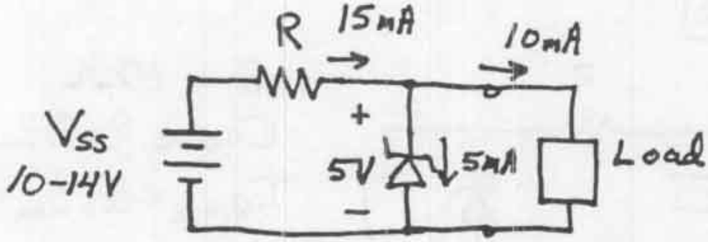
$$i_D = -\frac{V_{SS} + v_D}{R} = \frac{14 - 6}{100} = -80 \text{ mA}$$

(Notice that i_D and v_D assume negative values in this circuit.) The worst-case power dissipation for the Zener is:

$$P_D = v_D i_D = (-6)(-0.08) = 0.48 \text{ W}$$

Problem 3.46

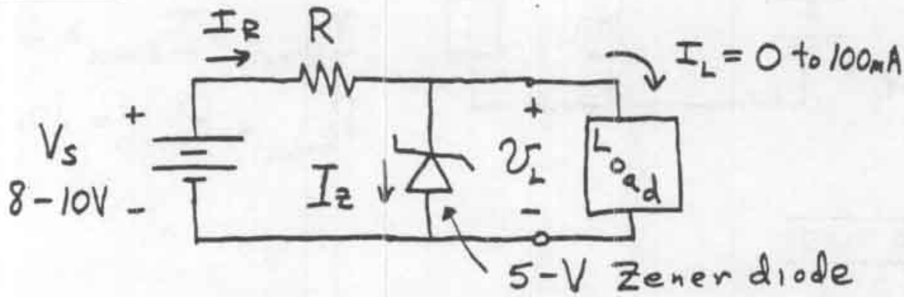
The circuit diagram is shown on the next page.



Minimum Zener diode current occurs with maximum load current and minimum V_{SS}. Thus we compute the required resistance.

$$R = \frac{V_{SS} - 5}{15\ \text{mA}} = \frac{10 - 5}{15\ \text{mA}} = 333\ \Omega$$

Problem 3.47



For all values of V_s and I_L we must have $I_z > 0$. Minimum I_z occurs for $V_s = 8$ V and $I_L = 100$ mA. Thus

$$I_{zmin} = \frac{8 - 5}{R} - 0.1 > 0 \quad \Rightarrow \quad R < 30\ \Omega$$

We select the standard nominal value R = 24 Ω to allow for resistor tolerance and to allow some design margin. Then we can compute the maximum power dissipation for each element as follows.

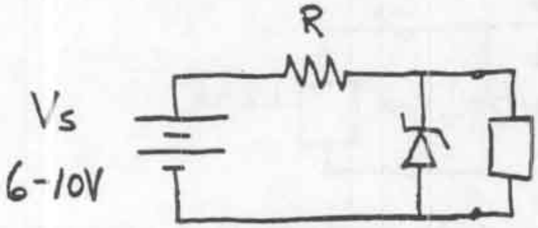
$$I_{Rmax} = \frac{V_{smax} - 5}{R} = 208\ \text{mA} = I_{zmax}$$

$$P_{Rmax} = RI_{Rmax}^2 = 1.04\ \text{W}$$

$$P_{zmax} = 5I_{zmax} = 1.04\ \text{W}$$

To allow some design margin, we should specify power dissipations of 2 W for the resistor and for the Zener.

Problem 3.48



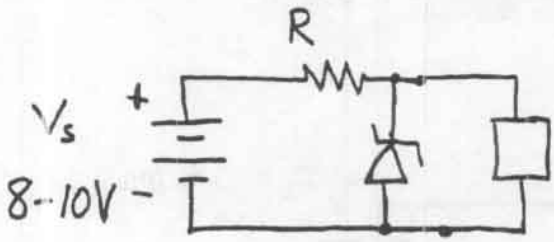
$R < 10\,\Omega$

Choose $R = 8.2\,\Omega$

$I_{R\,max} = I_{z\,max} = 610\text{ mA}$

$P_{R\,max} = P_{z\,max} = 3.05\text{ W}$

Problem 3.49



$R < 3.0\,\Omega$

Choose $R = 2.4\,\Omega$

$I_{R\,max} = I_{z\,max} = 2.08\text{A}$

$P_{R\,max} = P_{z\,max} = 10.4\text{W}$

Problem 3.50

Dynamic resistance is defined as

$$r_d = \left[\left(\frac{di_D}{dv_D}\right)_Q \right]^{-1}$$

For a vertical characteristic, we have

$$\left(\frac{di_D}{dv_D}\right)_Q = \infty \text{ and } r_d = 0.$$

Problem 3.51

Diode current is given by the Shockley equation:

$$i_D = I_s\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right]$$

Under forward bias the exponential is much greater than unity. Thus we can write

$$i_D = I_s \exp\left(\frac{v_D}{nV_T}\right)$$

$$I_s = i_D \exp\left(\frac{-v_D}{nV_T}\right)$$

(a) For $n = 1$: $I_s = 10^{-3} \exp\left(\frac{-0.6}{0.026}\right) = 95.0 \times 10^{-15}$ A

(b) For $n = 2$: $I_s = 10^{-3} \exp\left(\frac{-0.6}{2 \times 0.026}\right) = 9.75 \times 10^{-9}$ A

Problem 3.52

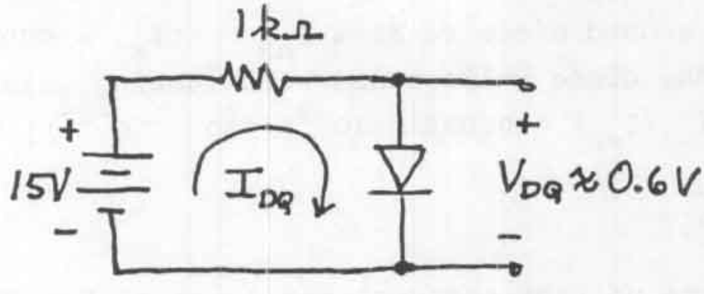
$$i_D = I_s\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right]$$

$$\exp\left(\frac{v_D}{nV_T}\right) = \frac{i_D + I_s}{I_s}$$

$$v_D = nV_T \ln\left(\frac{i_D + I_s}{I_s}\right)$$

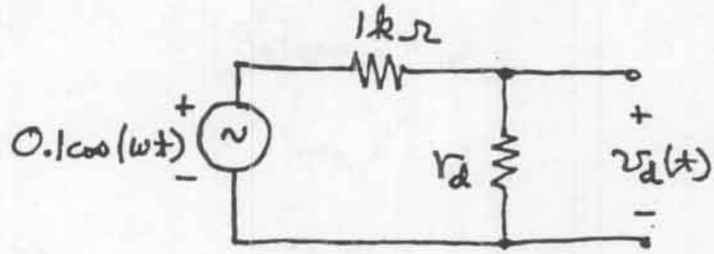
Problem 3.53

The large-signal (dc) equivalent circuit is:



The diode is forward biased with $V_{DQ} \cong 0.6$ V and $I_{DQ} \cong (15 - 0.6)/(1\ k\Omega) = 14.4$ mA.

The dynamic resistance of the diode is $r_d = nV_T/I_{CQ} = 1.81$ Ω. The small-signal (ac) equivalent circuit is:



The output voltage is

$$v_d(t) = 0.1\cos(\omega t)\frac{r_d}{1000 + r_d} = (181 \times 10^{-6})\cos(\omega t)$$

Finally the total output voltage is the sum of the dc and ac terms:

$$v_D(t) = 0.6 + (181 \times 10^{-6})\cos(\omega t)$$

Problem 3.54

$$i_D = I_s\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right] \cong I_s\exp\left(\frac{v_D}{nV_T}\right)$$

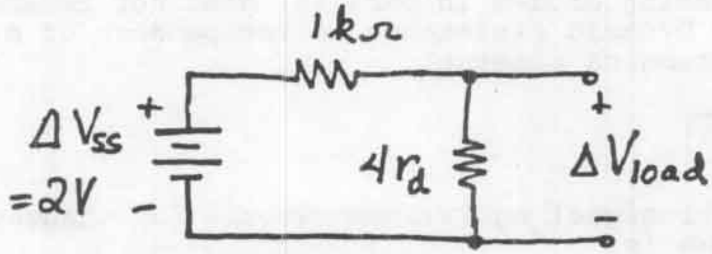
For the first diode we have

$$I_{s1} = i_{D1}\exp\left(\frac{-v_D}{nV_T}\right) = 10^{-3}\exp\left(\frac{-0.6}{0.026}\right) = 95.0 \times 10^{-15} \text{ A}$$

For the second diode we have $I_{s2} = 10I_{s1} = 950 \times 10^{-15}$ A. Solving for the diode voltage and substituting values, we have $v_{D2} = nV_T\ln(i_{D2}/I_{s2}) = 0.026\ln[10^{-3}/(950 \times 10^{-15})] = 0.540$ V.

Problem 3.55

(a) The source voltage changes from 10 to 12 V. We compute the Q-point for the middle of this range as $I_{DQ} = (11 - 2.4)/(1\ \text{k}\Omega) = 8.6$ mA. Then the dynamic resistance of each diode is $r_d = nV_T/I_{DQ} = (26\ \text{mV})/(8.6\ \text{mA}) = 3.02\ \Omega$. The small-signal equivalent circuit is



The change in the load voltage is

$$\Delta v_{load} = \Delta V_s \frac{4r_d}{1000 + 4r_d} = 2\,\frac{4(3.02)}{1000 + 4(3.02)} = 23.9\text{ mV}$$

$$\text{Source regulation} = \frac{\Delta V_{load}}{\Delta V_{SS}} \times 100\% = \frac{0.0239}{2} \times 100\% = 1.2\%$$

(b) For $V_{SS} = 12$ V, we have $I_{DQ} = 9.6$ mA and $r_d = (26\text{ mV})/(9.6\text{ mA}) = 2.71\ \Omega$. When the load is connected, it draws approximately $(2.4\text{ V})/(10\text{ k}\Omega) = 0.24$ mA. Thus the change in the diode current is $i_d = -0.24$ mA and the change in the load voltage is $\Delta V_{load} = 4r_d i_d = 2.6$ mV. The load regulation is

$$\text{Load regulation} = \frac{V_{no\text{-}load} - V_{full\text{-}load}}{V_{full\text{-}load}} \times 100\%$$

$$= \frac{\Delta V_{load}}{V_{full\text{-}load}} \times 100\ \%$$

$$= \frac{2.6\text{ mV}}{2.4\text{ V}} \times 100\% = 0.108\%$$

Problem 3.56

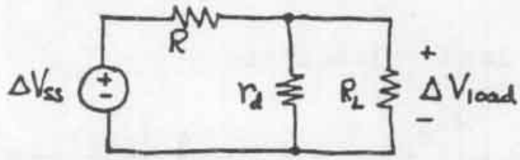
(a) $r_d = nV_T/I_{CQ} = (26\text{ mV})/(2\text{mA}) = 13\ \Omega$

(b) With two diodes in parallel, the dynamic resistance of each of them is $(26\text{ mV})/(1\text{ mA}) = 26\ \Omega$. However the dynamic resistance of the parallel combination is $13\ \Omega$.

Thus placing diodes in parallel does not reduce the dynamic resistance. Dynamic resistance is independent of diode area if the current remains constant.

Problem 3.57

The small-signal equivalent circuit for changes in the source voltage is:



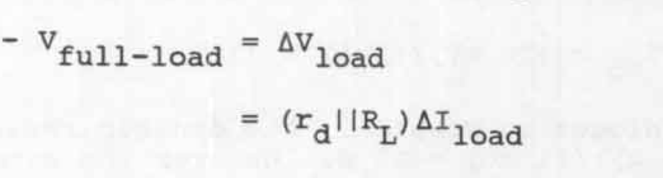
The change in the load voltage is given by

$$\Delta V_{load} = \Delta V_{SS} \frac{r_d || R_L}{R + r_d || R_L}$$

$$\text{Source regulation} = \frac{\Delta V_{load}}{\Delta V_{SS}} \times 100\%$$

$$= \frac{r_d || R_L}{R + r_d || R_L} \times 100\%$$

The small-signal equivalent circuit for changes in the load current is:



The change in load voltage due to the change in load current is

$$V_{no\text{-}load} - V_{full\text{-}load} = \Delta V_{load}$$

$$= (r_d || R_L) \Delta I_{load}$$

$$= (r_d || R_L) \frac{V_{full\text{-}load}}{R_L}$$

$$\text{Load regulation} = \frac{V_{no\text{-}load} - V_{full\text{-}load}}{V_{full\text{-}load}} \times 100\%$$

$$= \frac{(r_d || R_L)}{R_L} \times 100\%$$

$$= \frac{r_d}{r_d + R_L} \times 100\%$$

Problem 3.58

(a) $r_d = nV_T/I_{DQ} = 26\ \Omega$

(b) $\Delta v_D = \Delta i_D r_d = (0.1\text{ mA}) \times (26\ \Omega) = 2.6\text{ mV}$

(c) $i_D = I_s\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right]$

$$v_D = nV_T \ln\left(\frac{i_D}{I_s} - 1\right)$$

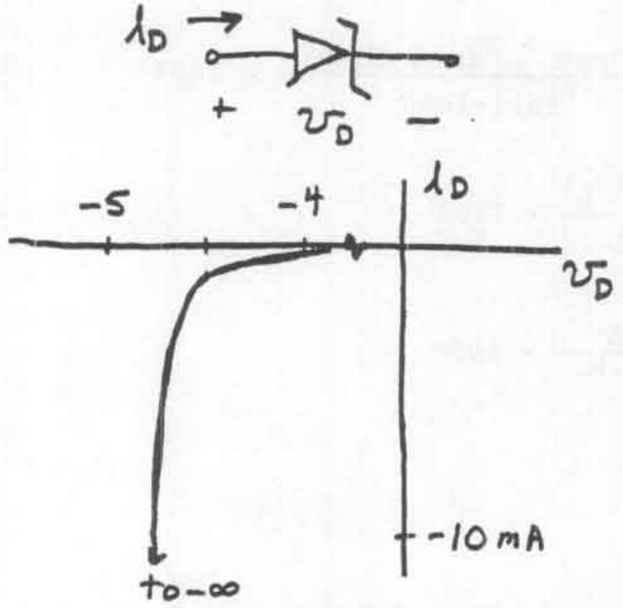
For $i_D = 1$ mA we find $v_D = 0.65854$ V and for $i_D = 1.1$ mA we find $v_D = 0.66102$ V for a difference of $\Delta v_D = 2.48$ mV which is 4.8% lower than the result using the dynamic resistance.

Problem 3.59

$$r_d = \left[\left(\frac{di_D}{dv_D}\right)_Q\right]^{-1} = 1.67 \times 10^6 \times \left(1 + \frac{V_{DQ}}{5}\right)^4$$

For $I_{DQ} = -1$ mA, $V_{DQ} = -4.5$ V and $r_d = 167\ \Omega$

For $I_{DQ} = -10$ mA, $V_{DQ} = -4.77$ V and $r_d = 7.48\ \Omega$



$$i_D = \frac{-10^{-6}}{(1 + v_D/5)^3}$$

v_D	i_D
0	$-1\,\mu A$
-3	$-15.6\,\mu A$
-4	$-125\,\mu A$
-4.5	-1 mA
-4.77	-10 mA
-5	$-\infty$

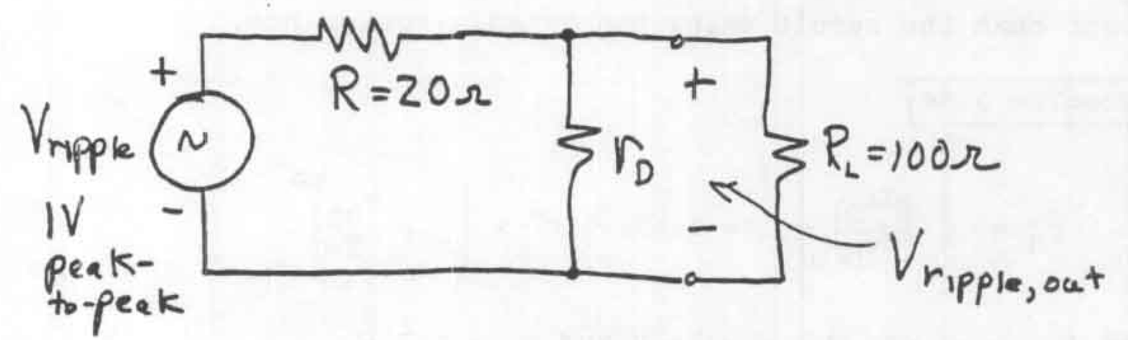
Problem 3.60

$I_L = V_L/R_L = 5/100 = 50$ mA

$I_{source} = (8 - 5)/20 = 150$ mA

$I_{QZenner} = I_{source} - I_L = 100$ mA

Small-signal equivalent circuit:



Let $R'_L = R_L || r_d$, then we can write:

$$V_{ripple,out} = 10 \text{ mV} = (1 \text{ V}) \times \frac{R'_L}{R'_L + R}$$

Solving we find $R'_L = 0.202\ \Omega$. Thus we have $R'_L = 0.202 = \frac{1}{1/r_d + 1/R_L}$ which yields $r_d = 0.202\ \Omega$.

Problem 3.61

See Figures 3.36 and 3.37 in the book.

Problem 3.62

In an intrinsic semiconductor, the free electron and hole concentrations are equal.

Problem 3.63

Free electrons and holes are generated by thermal energy that causes covalent bonds to break. The higher the temperature, the higher the rate of **generation**. When a free electron encounters a hole, **recombination** can occur in which the hole and free electron combine to form a filled covalent bond. As the concentration of holes and electrons builds up, recombination occurs more frequently. At a given temperature, an equilibrium exists for which the rate of recombination equals the rate of generation of charge carriers. As temperature increases, this equilibrium occurs for larger concentrations of charge carriers.

Problem 3.64

The conductivity of intrinsic silicon increases with temperature because the free-electron and hole concentrations increase with temperature.

Problem 3.65

See Figures 3.39 and 3.40 in the book.

Problem 3.66

$$p + N_D = n + N_A$$

Problem 3.67

The mass-action law states that $pn = p_i n_i$ in which p_i and n_i are the hole and free-electron concentrations in intrinsic silicon. Thus as we increase p (n) by adding acceptors (donors) the free-electron (hole) concentration decreases.

Problem 3.68

The average motion of the charge carriers due to an applied electric field is called drift. The average drift velocity is proportional to the electric field vector $\mathcal{E}$. We denote the drift velocity vector of electrons as $\mathbf{v}_n$ and the hole velocity vector as $\mathbf{v}_p$. Thus, we can write $\mathbf{v}_n = -\mu_n \mathcal{E}$ in which the constant of proportionality μ_n is called the mobility of the free electrons. Similarly, for holes we have $\mathbf{v}_p = \mu_p \mathcal{E}$ in which μ_p is the hole mobility.

Problem 3.69

Diffusion is caused by the random thermal motion of charge carriers. Diffusion causes a concentration of charge carriers to spread out with time.

Problem 3.70

The volume occupied by a single electon is

$$\text{vol} = \frac{1}{(5 \times 10^{22} \text{ atoms/cm}^3) \times (10^6 \text{ cm}^3/\text{m}^3)} = 2 \times 10^{-29} \text{ m}^3$$

We can get a crude estimate of atomic spacing by assuming that each atom is at the center of a cube.

$$\text{atomic spacing} \cong \sqrt[3]{\text{vol}} = 2.71 \times 10^{-10} \text{ m} = 2.71 \text{ Angstroms}$$

Problem 3.71

$$p \cong N_A = 10^{16} \text{ cm}^{-3}$$

$pn = n_i^2 = (1.45 \times 10^{10})^2 \quad \Rightarrow \quad n = 2.10 \times 10^4 \text{ cm}^{-3}$

Problem 3.72

(a) We have $n >> p$, thus $n + N_A = p + N_D \cong N_D$ and we have $n \cong N_D - N_A = 0.99 \times 10^{17}$ cm^{-3}. Then $p = n_i^2/n = 2.12 \times 10^3$ cm^{-3}.

(b) We have $N_A = N_D$, thus $n = p = n_i = 1.45 \times 10^{10}$ cm^{-3}.

Problem 3.73

See Figure 3.43 in the book.

Problem 3.74

Thermal energy creates minority carriers on each side of the junction. When these minority carriers enter the depletion region they are swept across to the opposite side. This results in current flow from the n-side to the p-side.

High-energy majority carriers can cross the junction in opposition to the barrier field. This diffusion current is equal and opposite to the minority carrier current.

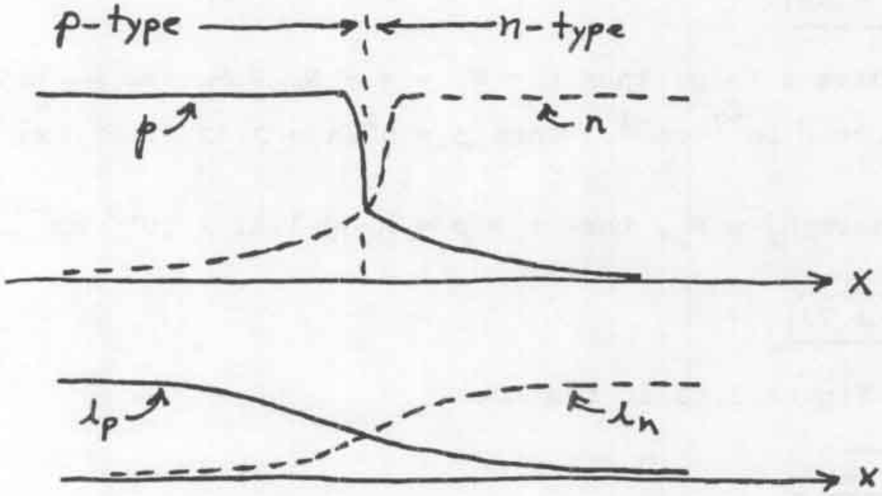
Problem 3.75

I_s is the minority carrier current. It increases with temperature because the concentration of minority carriers increases with temperature.

I_s is proportional to junction area, because the number of minority carriers that diffuse into the depletion region is proportional to junction area.

As the doping is increased on both sides of the junction the minority concentration decreases resulting in a decrease in I_s.

Problem 3.76



Problem 3.77

With the switch open, we have

$$i_{D1} = 1 \text{ mA} = I_s\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right] = i_D = I_s\left[\exp\left(\frac{0.600}{0.026}\right) - 1\right]$$

Solving, we find $I_s = 9.5 \times 10^{-14}$ A.

With the switch closed, the current splits equally between the two diodes, and we have

$$i_{D1} = 0.5 \text{ mA} = i_D = I_s\left[\exp\left(\frac{v_{D1}}{nV_T}\right) - 1\right]$$

Solving for v_{D1} we have

$$v_{D1} = nV_T \ln\left(\frac{i_{D1}}{I_s} + 1\right) = 582 \text{ mV.}$$

Repeating with n = 2, we find $I_s \cong 9.75 \times 10^{-9}$ A and v_{D1} = 564 mV.

Problem 3.78

Under forward bias with $v_D >> nV_T$ we have

$$i_{D1} \cong I_s \exp\left(\frac{v_{D1}}{nV_T}\right) \quad \text{and} \quad i_{D2} \cong I_s \exp\left(\frac{v_{D2}}{nV_T}\right)$$

Dividing the respective sides of these equations we obtain:

$$\frac{i_{D2}}{i_{D1}} = \frac{I_s \exp\left(\frac{v_{D2}}{nV_T}\right)}{I_s \exp\left(\frac{v_{D1}}{nV_T}\right)} = \exp\left(\frac{v_{D2} - v_{D1}}{nV_T}\right)$$

Solving for $\Delta v_D = v_{D2} - v_{D1}$ we have

$$\Delta v_D = nV_T \ln\left(\frac{i_{D2}}{i_{D1}}\right)$$

Computing the desired results we have:

n	i_{D2}/i_{D1}	Δv_D (mV)
1	2	18
1	10	60
2	2	36
2	10	120

Problem 3.79

(a) By symmetry, $I_A = I_B = 100$ mA.

(b) Solving the Shockley equation for I_s we have

$$I_s = \frac{i_D}{\exp(v_D/nV_T) - 1}$$

Substituting values for diode A at 300 K:

$$V_{TA} = \frac{kT}{q} = 25.86 \text{ mV}$$

$$I_{sA} = \frac{100 \text{ mA}}{\exp(0.7/0.026) - 1}$$

$$= 1.75 \times 10^{-13} \text{ A}$$

Similarly for diode B at 305 K we have

$$V_{TB} = 26.29 \text{ mV} \quad \text{and} \quad I_{sB} = 3.5 \times 10^{-13} \text{ A}$$

Now we must have

$$0.20 = I_A + I_B$$

$$0.20 = [1.75\exp(v/25.86) + 3.5\exp(v/26.29)] \times 10^{-13}$$

in which we have assumed that v is expressed in mV. We solve this equation by trial and err resulting in v = 696.6 mV. Then we can compute the currents as I_A = 87 mA and I_B = 113 mA.

Problem 3.80

First we compute I_s assuming that the series resistance is zero.

$$I_s = \frac{i_D}{\exp(v_D/nV_T) - 1}$$

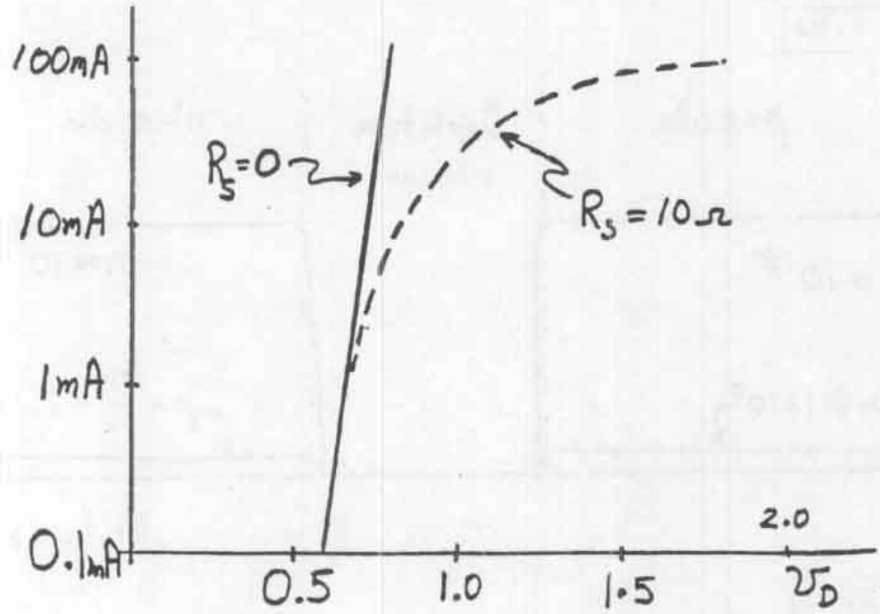
$$= \frac{10^{-3}}{\exp(650/26) - 1}$$

$$= 1.39 \times 10^{-14}$$

Then the diode voltage is given by

$$v_D = nV_T \ln\left(\frac{i_D}{I_s} + 1\right) + R_s i_D$$

The plots are shown on the next page.



Problem 3.81

For the first diode we have:

$$i_{D1} = I_{s1}\left[\exp\left(\frac{v_{D1}}{V_T}\right) - 1\right]$$

Substituting values and solving for I_{s1} yields

$$I_{s1} = 9.50 \times 10^{-14} \text{ A}$$

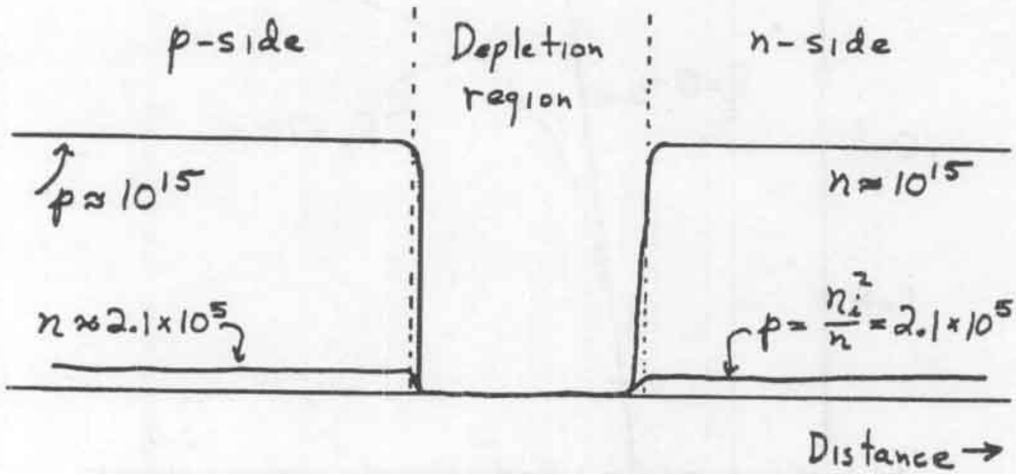
$$I_{s2} = I_{s1}/2 = 4.75 \times 10^{-14}$$

$$v_{D2} = V_T \ln\left(\frac{i_D}{I_{s2}} + 1\right)$$

$$= 0.026 \ln\left(\frac{10^{-3}}{4.75 \times 10^{-14}} + 1\right)$$

$$= 618 \text{ mV}$$

Problem 3.82



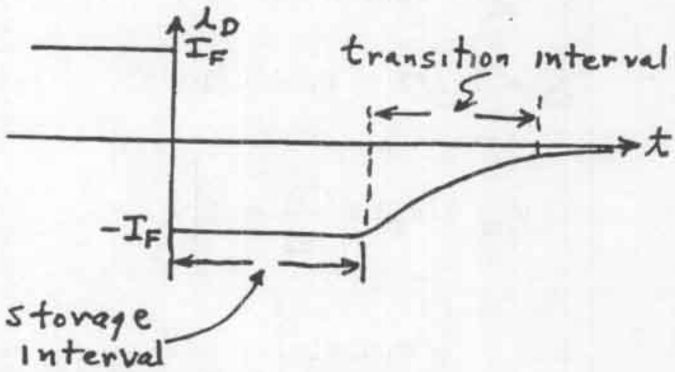
Problem 3.83

The two capacitances are the depletion capacitance which is most important under reverse bias and the diffusion capacitance which is most important under forward bias.

Problem 3.84

See Figure 3.50 in the book.

Problem 3.85



The reverse recovery time is the sum of the storage interval and the transition interval.

Problem 3.86

$$\varepsilon = \varepsilon_r \varepsilon_0 = 3.97 \times 8.85 \times 10^{-12} = 35.1 \times 10^{-12}$$

$$C = \frac{\varepsilon A}{d} \quad \Rightarrow \quad A = \frac{Cd}{\varepsilon} = \frac{30 \times 10^{-12} \times 10^{-7}}{35.1 \times 10^{-12}} = 8.55 \times 10^{-8}$$

$$L = \sqrt{A} = \sqrt{8.55 \times 10^{-8}} = 292\ \mu m$$

Problem 3.87

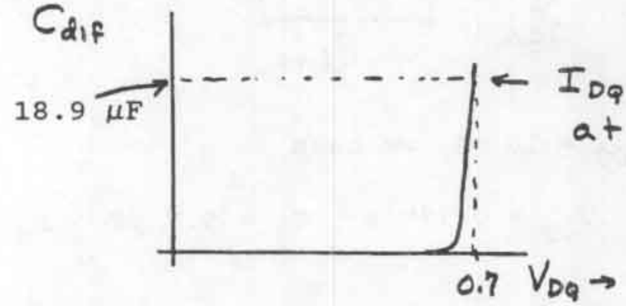
$$C_j = \frac{C_{j0}}{\left[1 - (V_{DQ}/\phi_0)\right]^m}$$

m	$V_{DQ} = -1$ V	$V_{DQ} = -10$ V
1/2	70.7 pF	30.2 pF
1/3	79.4 pF	45.0 pF

Problem 3.88

$$C_{dif} = \frac{\tau_T I_{DQ}}{V_T} \qquad I_{DQ} \cong I_s \exp(V_{DQ}/V_T)$$

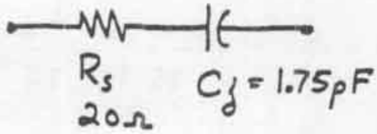
$$C_{dif} = 3.94 \times 10^{-17} \times \exp(V_{DQ}/0.026)$$



Problem 3.89

(a) Under reverse bias, C_{dif} is negligible. The depletion capacitance is given by:

$$C_j = \frac{C_{j0}}{\left[1 - (V_{DQ}/\phi_0)\right]^m} = \frac{5 \text{ pF}}{\left[1 - (-20/0.9)\right]^{0.333}} = 1.75 \text{ pF}$$

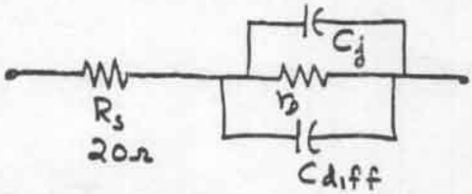


(b) $C_{dif} = \dfrac{\tau_T I_{DQ}}{V_T} = 231 \text{ pF}$

$$r_d = \frac{nV_T}{I_{DQ}} = 26\ \Omega$$

$$V_{DQ} = nV_T \ln(I_{DQ}/I_s) = 0.718 \text{ V}$$

$$C_j = \frac{C_{j0}}{\left[1 - (V_{DQ}/\phi_0)\right]^m} = \frac{5 \text{ pF}}{\left[1 - (0.718/0.9)\right]^{0.333}} = 8.51 \text{ pF}$$



(c) Similarly for $I_{DQ} = 10$ mA, we have

$C_{dif} = 2310$ pF $V_{DQ} = 0.778$ V $C_j = 9.7$ pF $r_d = 2.6\ \Omega$

Problem 3.90

(a) $i_D(0-) = (5 - 0.67)/(5 \text{ k}\Omega) = 0.866 \text{ mA}$

$i_D(0+) = -(5 + 0.62)/(5 \text{ k}\Omega) = -1.124 \text{ mA}$

$$R_s = \frac{v_D(0-) - v_D(0+)}{i_D(0-) - i_D(0+)} = \frac{(0.67 - 0.62)\ V}{(0.866 + 1.124)\ mA} = 25\ \Omega$$

(b) $$C_{j0} = \left(\frac{dQ}{dv_D}\right)_{V_{DQ} = 0} - 7\ pF$$

(We must subtract the input capacitance of the oscilloscope.)

$$C_{j0} = \frac{dQ/dt}{\left(dv_D/dt\right)_{V_{DQ}=0}} - 7\ pF$$

From Figure P3.90 we see that $V_{DQ} = 0$ at $t = 1\ \mu s$. Also $dQ/dt = i_D = -1$ mA when $V_{DQ} = 0$.

$$C_{j0} = \frac{-10^{-3}}{-30 \times 10^{6}} - 7\ pF$$

$$= 26.3\ pF$$

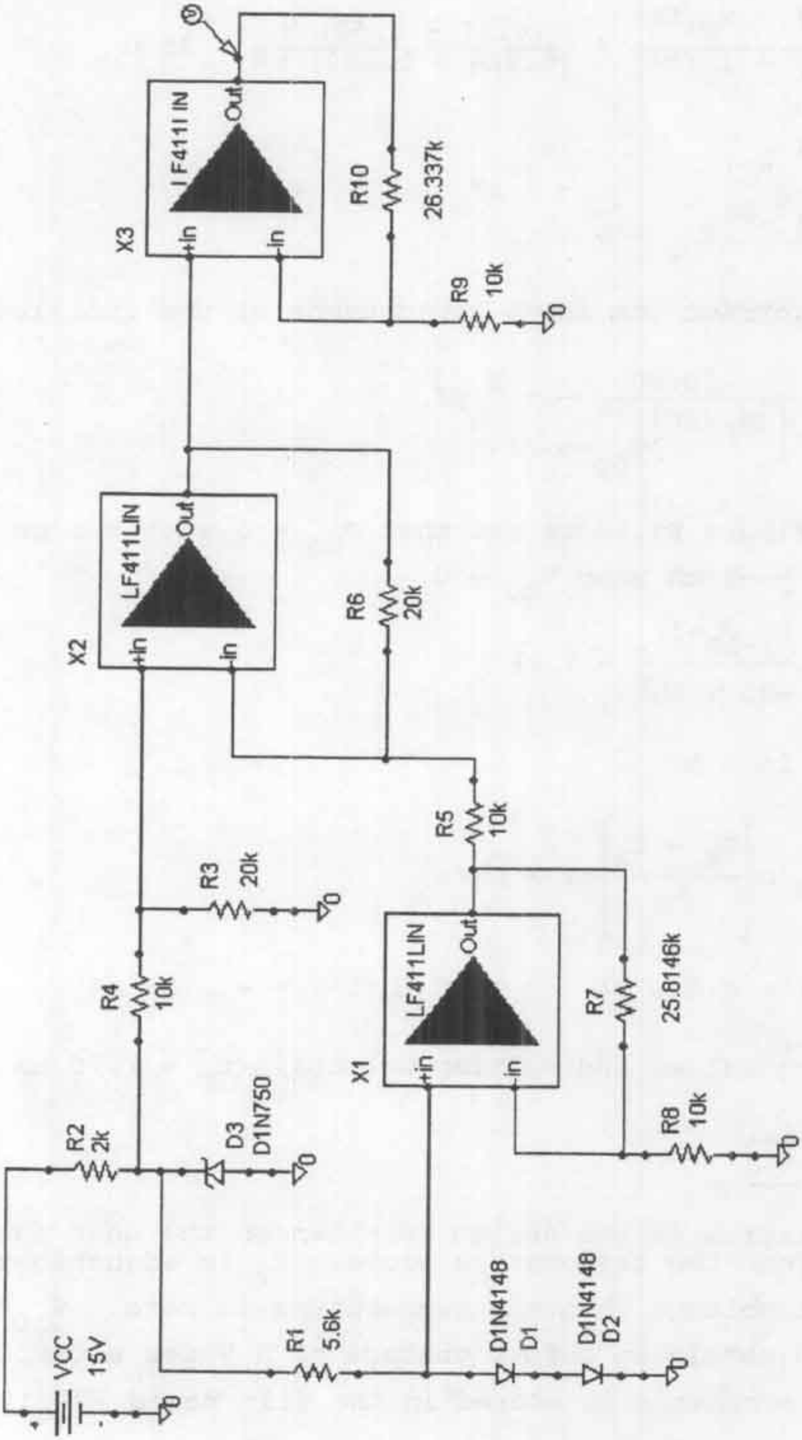
(c) $$t_s = \tau_T \ln\left(\frac{I_F - I_R}{I_R}\right) \cong 1\ \mu s$$

$I_F = i_D(0-) = 0.866$ mA $\quad$ $I_R = i_D(0+) = -1.124$ mA

Substituting values and solving we obtain $\tau_T = 1.75\ \mu s$.

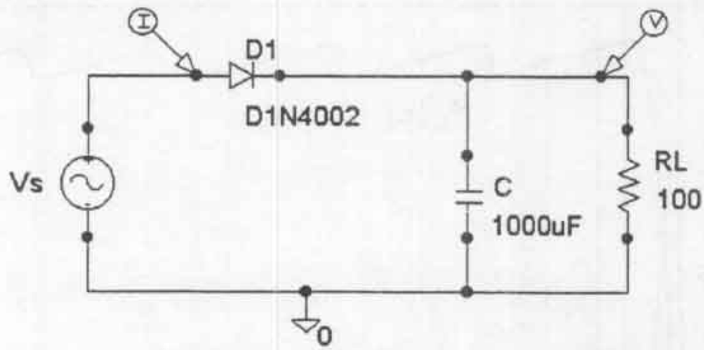
Problem 3.91

The diagram of one design is shown on the next page. Diodes D_1 and D_2 form the temperature probe. R_7 is adjusted to obtain zero output voltage when the temperature is zero. R_{10} is adjusted to obtain an output voltage of 5 V for a temperature of 50°C. The schematic is stored in the file named P3_91.

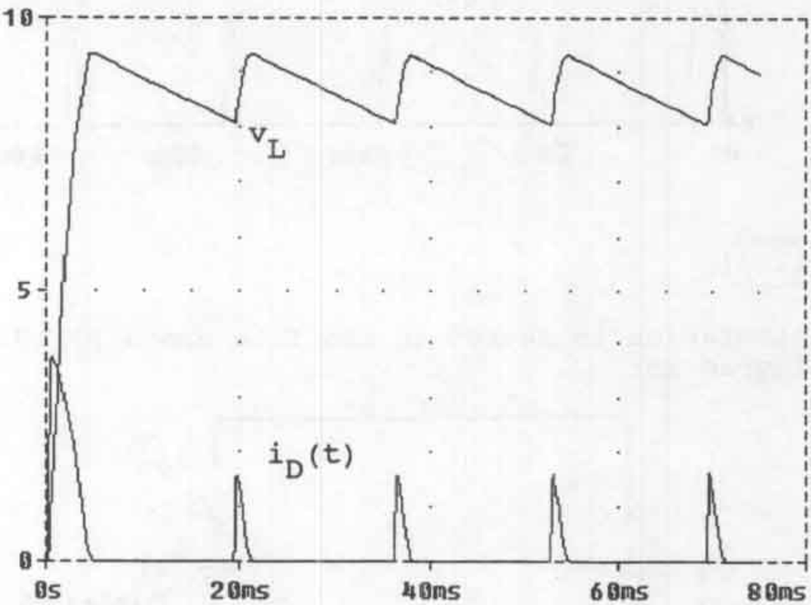

VCC
15V
R1
5.6k
D1N4148
D1
D1N4148
D2
R2
2k
D3
D1N750
R4
10k
R3
20k
X1
LF411LIN
R7
25.8146k
R8
10k
R5
10k
X2
LF411LIN
R6
20k
X3
R10
26.337k
R9
10k

Problem 3.92

The schematic is stored in the file named P3_92. The circuit diagram is:

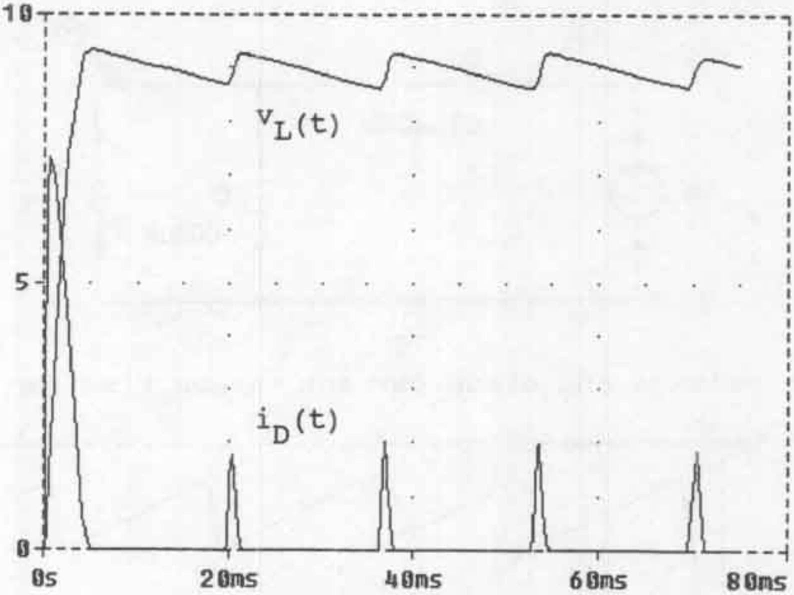


The output voltage and diode current versus time for C = 1000 μF:



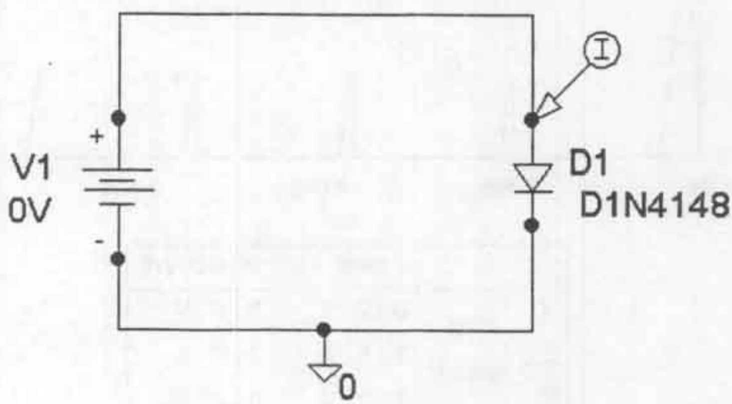
	1000 μF	2000 μF
$V_{L,avg}$	8.7 V	8.9 V
$I_{D,peak}$	1.5 A	2.0 A
$V_{r,p-p}$	1.2 V	0.6 V

The output voltage and diode current versus time for C = 2000 μF are shown below:

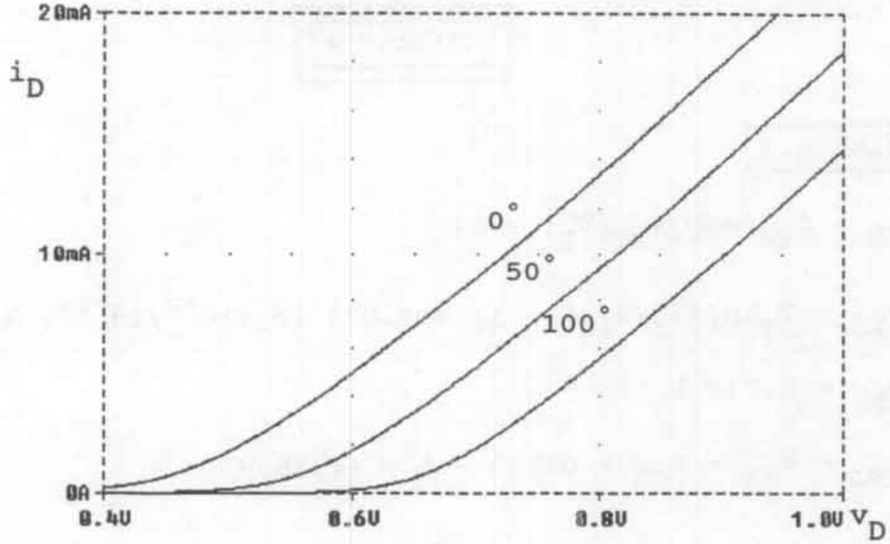


Problem 3.93

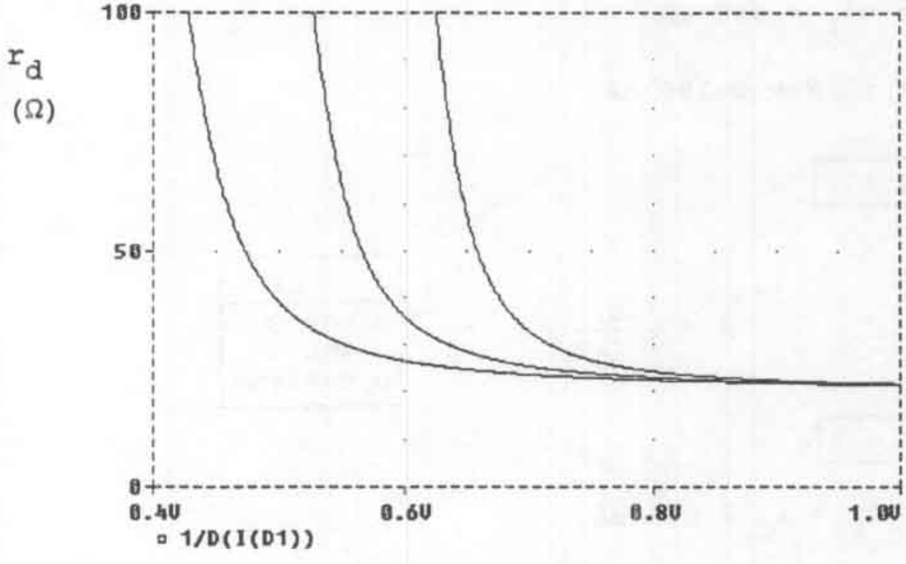
The simulation is stored in the file named P3_93. The circuit diagram is:



Plots of the diode characteristics are shown on the next page.



Plots of the dynamic resistance are:



Chapter 4

Exercise 4.1

$$i_E = I_{ES}[\exp(v_{BE}/V_T) - 1]$$

$$v_{BE} = V_T \ln[(i_E/I_{ES}) + 1] = 0.026 \ln[(10^{-2}/10^{-14}) + 1]$$

$$v_{BE} = 0.718 \text{ V}$$

$$v_{BC} = v_{BE} - v_{CE} = 0.718 - 5 = -4.28 \text{ V}$$

$$\alpha = i_C/i_E = \frac{i_C}{i_C + i_B} = \frac{\beta i_B}{\beta i_B + i_B} = \frac{\beta}{\beta + 1} = \frac{50}{50 + 1}$$

$$\alpha = 0.980$$

$$i_C = \alpha i_E = 9.8 \text{ mA}$$

$$i_B = i_C/\beta = 0.196 \text{ mA}$$

Exercise 4.2

$$\beta = \frac{\alpha}{1 - \alpha}$$

α	β
0.900	9
0.990	99
0.999	999

Exercise 4.3

$$i_B = i_E - i_C = 0.5 \text{ mA}$$

$$\alpha = i_C/i_E = 0.95$$

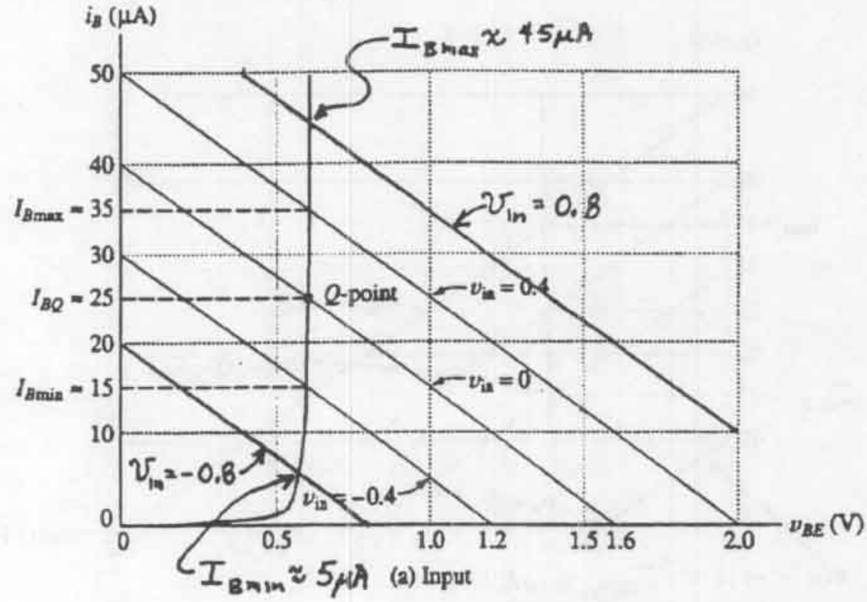
$$\beta = \alpha/(1 - \alpha) = 19$$

Exercise 4.4

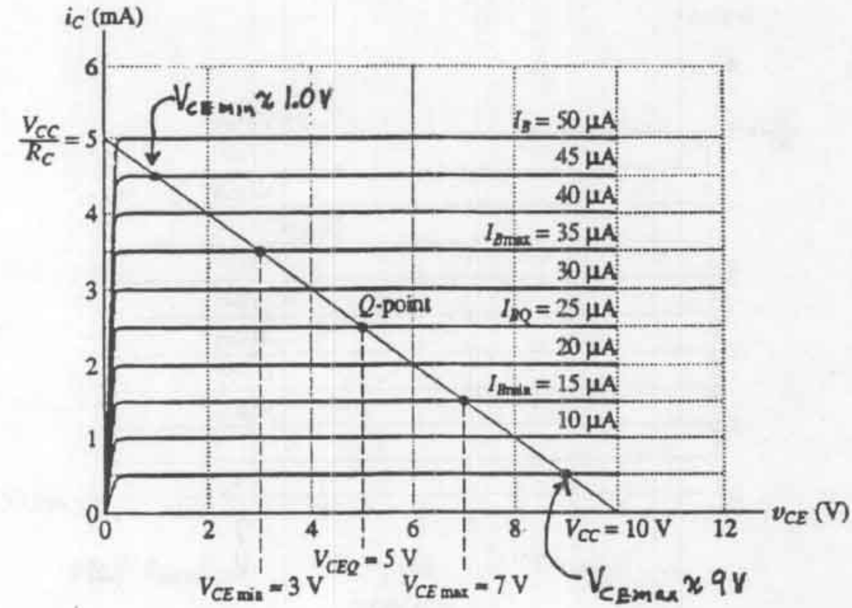
The output characteristics are identical to Figure 4.4b in the book except that the values on the i_C axis must be doubled.

Exercise 4.5

The load lines for v_{in} = -0.8 V and 0.8 V are shown below.



(a) Input

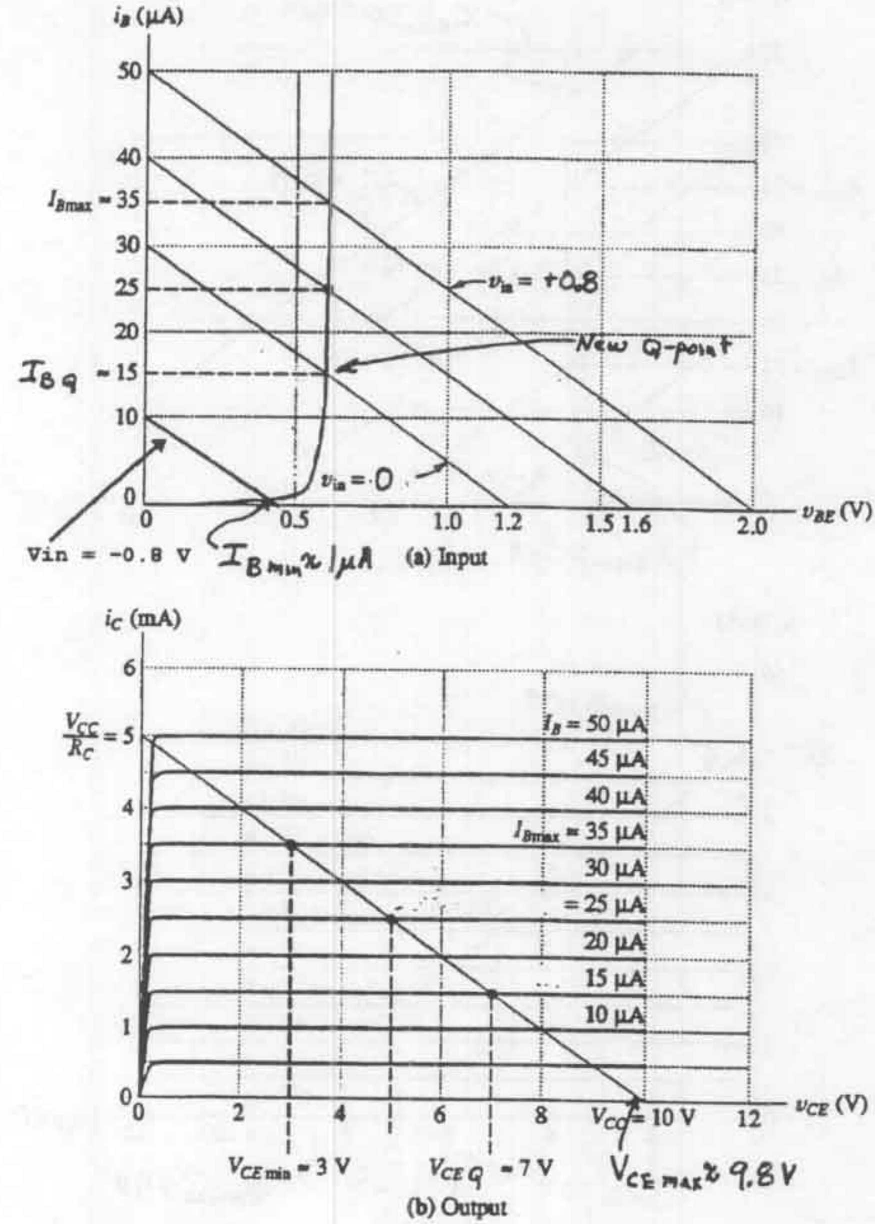


(b) Output

The results are $V_{CEmax} \cong 9.0$ V, $V_{CEQ} \cong 5.0$ V, $V_{CEmin} \cong 1.0$ V.

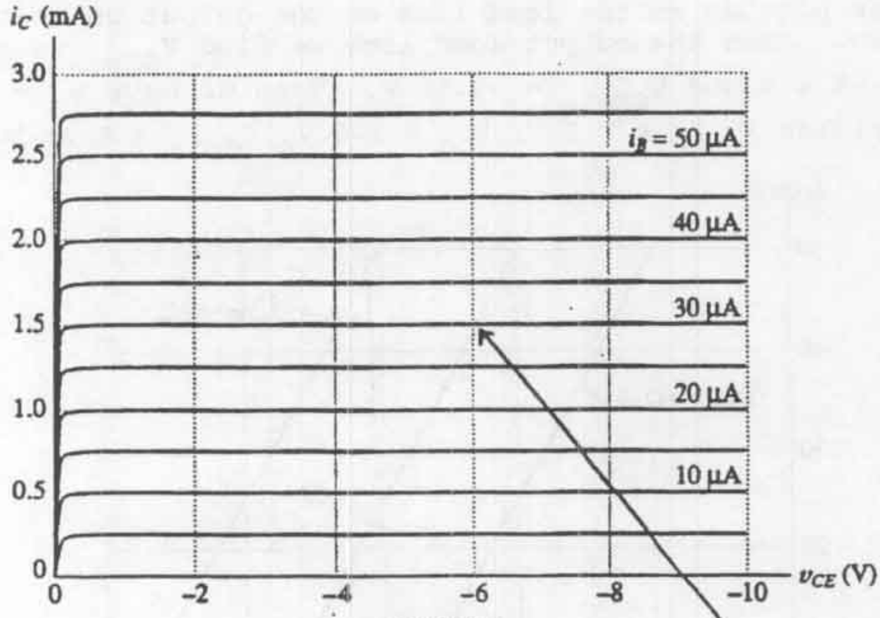
Exercise 4.6

The load lines are shown below.



From the load lines we find $V_{CEmax} \cong 9.8$ V, $V_{CEQ} \cong 7.0$ V, and $V_{CEmin} \cong 3.0$ V.

Exercise 4.7



(b) Output

Pick a point in the active region such as the one indicated by the arrow. Then $\beta = i_C/i_B = (1.5\ \text{mA})/(30\ \mu\text{A}) = 50$. $\alpha = \beta/(\beta + 1) = 0.98$. Slightly different answers will result from different points in the active region depending on the transistor.

Exercise 4.8

The equation for the input circuit is

$$v_{in}(t) + R_B i_B - v_{BE} - 9 + 8.2 = 0$$

Substituting values and rearranging we have

$$v_{BE} - 8000 i_B = -0.8 + 0.2\sin(2000\pi t)$$

The corresponding load line is plotted on the next page. From the load line we determine that $I_{Bmax} \cong 48\ \mu\text{A}$, $I_{BQ} \cong 24\ \mu\text{A}$ and $I_{Bmin} \cong 5\ \mu\text{A}$.

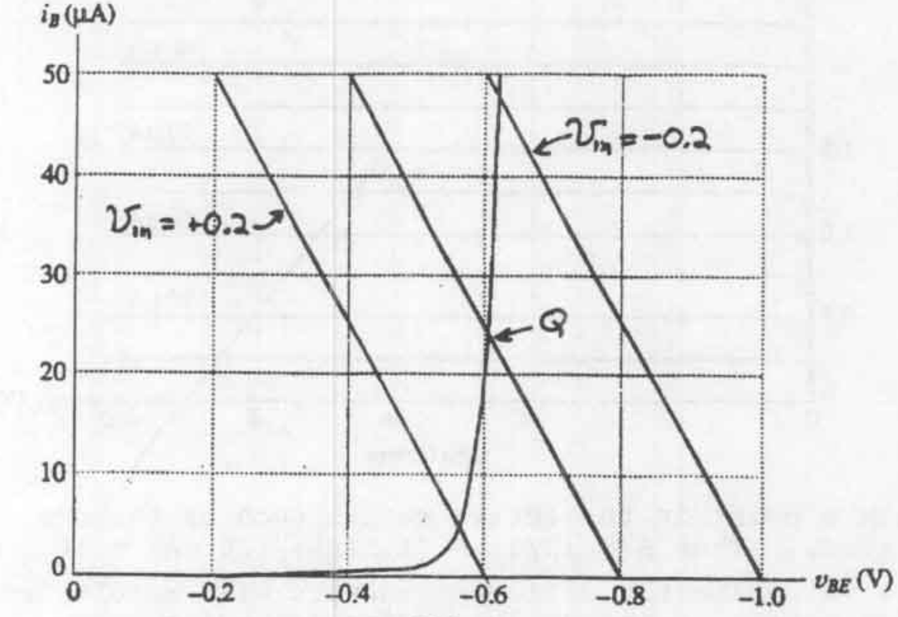
The equation for the output circuit is

$$v_{CE} - R_C i_C + 9 = 0$$

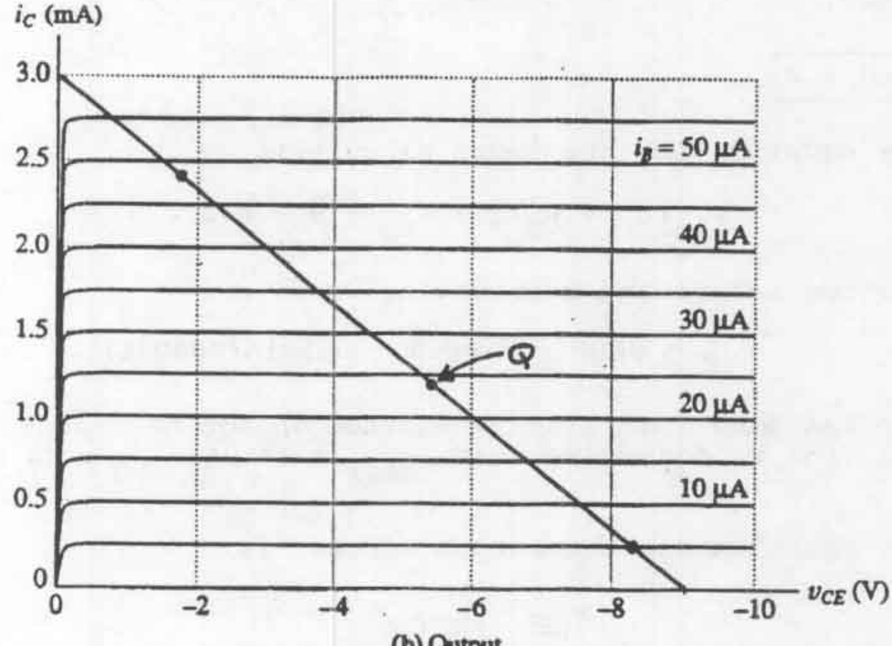
Substituting values and rearranging we have

$$v_{CE} - 3000 i_C = -9$$

which is plotted as the load line on the output characteristics as shown. From the output load line we find $V_{CEmax} = -1.8$ V, $V_{CEQ} = -5.4$ V and $V_{CEmin} = -8.25$ V. Then we have $v_o = v_{CE} + 9$, which yields $V_{Omax} \cong 7.2$ V, $V_{OQ} \cong 3.6$ V, $V_{Omin} \cong 0.75$ V.



(a) Input



(b) Output

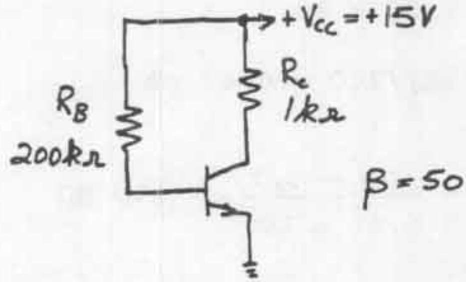
Exercise 4.9

(a) $V_{BE} = -0.2$ V and $V_{CE} = 5$ V, because we have $v_{BE} < 0.5$, the transistor is in cutoff.

(b) $I_B = 50\ \mu A$ and $I_C = 2$ mA, because we have $I_C < \beta I_B$ the transistor is in saturation.

(c) $V_{CE} = 5$ V and $I_B = 50\ \mu A$, because we have $V_{CE} > 0.2$ and $I_B > 0$, the transistor is in the active region.

Exercise 4.10



(a) Let us assume operation in the active region. Then we have $I_B = (V_{CC} - 0.7)/R_B = 71.5\ \mu A$, $I_C = \beta I_B = 3.575$ mA, and $V_{CE} = V_{CC} - R_C I_C = 11.4$ V. Because we found $V_{CE} > 0.2$ V, the active-region assumption is valid and the results are correct.

(b) Again let us assume operation in the active region. Then we have $I_B = (V_{CC} - 0.7)/R_B = 71.5\ \mu A$, $I_C = \beta I_B = 17.9$ mA, and $V_{CE} = V_{CC} - R_C I_C = -2.9$ V. Because we found $V_{CE} < 0.2$ V, the active-region assumption is invalid, and the results are not correct.

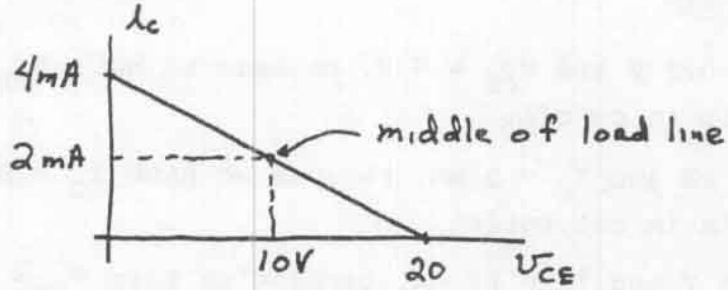
Therefore let us assume operation in saturation. Then we have $I_B = (V_{CC} - 0.7)/R_B = 71.5\ \mu A$, $I_C = (V_{CC} - 0.2)/R_C = 14.8$ mA. Because we have $\beta I_B > I_C$ the saturation-region assumption is valid.

Exercise 4.11

The load-line equation is

$$V_{CC} = R_C I_C + V_{CE} \quad \text{or} \quad 20 = 5000 I_C + V_{CE}$$

A plot of the load line is:



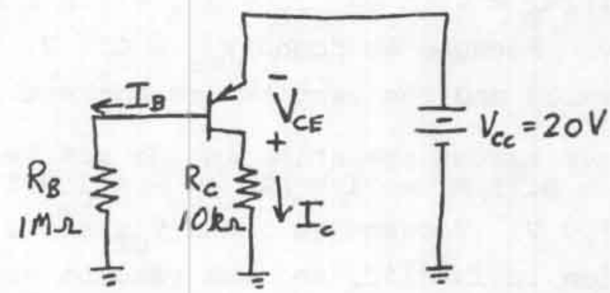
(a) $I_B = I_C/\beta = (2\ mA)/100 = 20\ \mu A$

$$R_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20 - 0.7}{20 \times 10^{-6}} = 965\ k\Omega$$

(b) $I_B = I_C/\beta = (2\ mA)/300 = 6.67\ \mu A$

$$R_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20 - 0.7}{6.67 \times 10^{-6}} = 2.9\ M\Omega$$

Exercise 4.12



(a) $I_B = \dfrac{V_{CC} + V_{BE}}{R_B} = \dfrac{20 - 0.7}{1\ M\Omega} = 19.3\ \mu A$

We assume operation in the active region. Then we have

$$I_C = \beta I_B = 0.965\ mA$$
$$V_{CE} = -20 + R_C I_C = -10.35\ V$$

Because $V_{CE} < -0.2$ V, the transistor is in fact operating in the active region and the problem is solved.

(b) As in part (a) we have $I_B = 19.3\ \mu A$. We start by assuming operation in the active region resulting in

$$I_C = \beta I_B = 2.90 \text{ mA}$$

$$V_{CE} = -20 + R_C I_C = 9 \text{ V}$$

Because $V_{CE} > -0.2$ V, the active region assumption is not valid. Therefore assume operation in saturation, in which case we have

$$I_B = \frac{V_{CC} + V_{BE}}{R_B} = \frac{20 - 0.7}{1\ M\Omega} = 19.3\ \mu A$$

$$V_{CE} = -\ 0.2 \text{ V}$$

$$I_C = \frac{V_{CC} - 0.2}{R_C}\ 1.98 \text{ mA}$$

Then because $\beta I_B > I_C$ the transistor is operating in saturation, and the problem is solved.

Exercise 4.13

$$R_1 = 100\ k\Omega \qquad R_2 = 50\ k\Omega$$

$$R_B = \frac{1}{1/R_1 + 1/R_2} = 33.3\ k\Omega$$

$$V_B = V_{CC}\frac{R_2}{R_1 + R_2} = 5 \text{ V}$$

$$I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{5 - 0.7}{33.3k + (\beta+1)1k}$$

$$I_C = \beta I_B$$

$$I_E = I_C + I_B$$

$$V_{CE} = V_{CC} - R_C I_C - R_E I_E$$

β	I_B (μA)	I_C (mA)	I_E (mA)	V_{CE} (V)
100	32.0	3.20	3.23	8.57
300	12.9	3.86	3.87	7.27

In Example 4.7 the ratio of the collector currents is 4.24/4.12 = 1.029. For the higher resistor values in this exercise the ratio is 3.86/3.20 = 1.21. In general higher resistance values in the four-resistor bias circuit lead to greater changes in the bias point with changes in β. The SPICE simulation is stored in the file named Exer4_13.

Exercise 4.14

For the four-resistor bias circuit we have:

$$R_B = \frac{1}{1/R_1 + 1/R_2}$$

$$V_B = V_{CC}\frac{R_2}{R_1 + R_2}$$

$$I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1)R_E} \qquad I_C = \beta I_B$$

$$V_{CE} = V_{CC} - R_C I_C - R_E I_E$$

(a) An increase in R_C has no effect on I_C (provided that operation remains in the active region).
(b) An increase in R_E decreases I_B and I_C.
(c) An increase in R_1 decreases V_B I_B and I_C.
(d) An increase in R_2 increases V_B I_B and I_C.
(e) An increase in β increases I_C.

Exercise 4.15

(a) An increase in R_C reduces V_{CE}.
(b) An increase in R_1 increases V_{CE}.
(c) An increase in R_2 decreases V_{CE}.
(d) An increase in β decreases V_{CE}.

Exercise 4.16

Because $V_{BE} \cong 0.7$ V for Q_1 and Q_2 and because the bases are grounded, the voltage at the top node of the 2-mA current source is -0.7 V.

Exercise 4.17

Assuming that the area of Q_2 is twice that of Q_1, we have $I_{E2} = 2I_{E1}$. Also we must have $I_{E1} + I_{E2} = 2$ mA. These facts yield $I_{E1} = 0.667$ mA and $I_{E2} = 1.333$ mA.

Then we have $I_{C2} = \alpha I_{E2} = 0.99(1.333) = 1.320$ mA. $I_1 = I_{C2} - I_{B3} = 1.32 - (1 - 0.99)5 = 1.27$ mA. Finally $V_o = 0.7 - 5000I_1 + 15 = 9.35$ V.

Exercise 4.18

$$\alpha = \beta/(\beta + 1) = 0.990$$

$$I_{C1} = \alpha I_{E1} = 0.99 \text{ mA}$$

$$5000(I_{C1} - I_{B2}) = 0.7 + 2000I_{E2}$$

$$5000(0.99 \times 10^{-3} - I_{B2}) = 0.7 + 2000(\beta + 1)I_{B2}$$

$$I_{B2} = 20.53\ \mu\text{A} \qquad I_{C2} = \beta I_{B2} = 2.053 \text{ mA}$$

$$V_o = 6000I_{C2} - 15$$
$$= -2.68 \text{ V}$$

Exercise 4.19

$$g_m = I_{CQ}/V_T \qquad r_\pi = \frac{\beta V_T}{I_{CQ}}$$

I_{CQ} (mA)	g_m (mS)	r_π (Ω)
1	38.5	2600
10	385	260

Exercise 4.20

We analyzed the bias circuit in Example 4.7. For $\beta = 300$ we determined that $I_{CQ} = 4.24$ mA.

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = 1839\ \Omega$$

$$R'_L = \frac{1}{1/R_L + 1/R_C} = 667\ \Omega$$

$$R_B = R_1 || R_2 = 3.33\ k\Omega$$

(a)

$$A_v = \frac{v_o}{v_{in}} = -\frac{\beta R'_L}{r_\pi} = -109$$

$$A_{vo} = \frac{v_o}{v_{in}} = -\frac{\beta R_C}{r_\pi} = -163$$

$$Z_{it} = r_\pi = 1839$$

$$Z_{in} = \frac{1}{1/R_B + 1/Z_{it}} = 1185\ \Omega$$

$$A_i = \frac{i_o}{i_{in}} = A_v \frac{Z_{in}}{R_L} = -64.6$$

$$G = A_i A_v = 7039$$

$$Z_o = R_C = 1\ k\Omega$$

(b)

$$v_{in} = v_s \frac{Z_{in}}{Z_{in} + R_s} = 0.703 v_s$$

$$v_o = A_v v_{in} = -76.6 v_s$$

$$v_o(t) = -76.6 \sin(\omega t)\ mV$$

Exercise 4.21

$$R_B = R_1 || R_2 = 50\ \text{k}\Omega$$

$$V_B = V_{CC} \frac{R_1}{R_1 + R_2} = 10\ \text{V}$$

$$V_B = R_B I_{BQ} + V_{BEQ} + R_E(1 + \beta) I_{BQ}$$

Substituting values, we find $I_{BQ} = 14.26\ \mu\text{A}$. Then we have

$$I_{CQ} = \beta I_{BQ} = 4.28\ \text{mA}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = 1823\ \Omega$$

$$R'_L = \frac{1}{1/R_L + 1/R_E} = 667\ \Omega$$

$$A_v = \frac{(1 + \beta)R'_L}{r_\pi + (1 + \beta)R'_L} = 0.991$$

$$Z_{it} = \frac{v_{in}}{i_b} = r_\pi + (1 + \beta)R'_L = 202.5\ \text{k}\Omega$$

$$Z_i = \frac{1}{1/R_B + 1/Z_{it}} = 40.1\ \text{k}\Omega$$

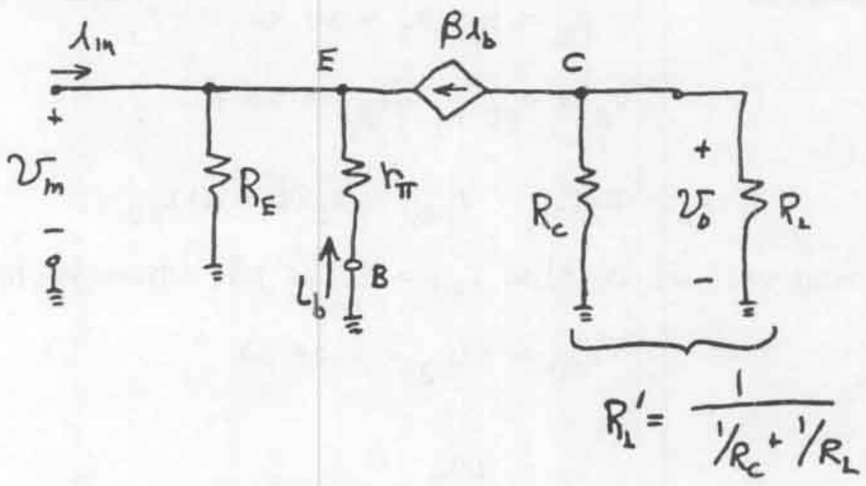
$$R'_s = \frac{1}{1/R_s + 1/R_1 + 1/R_2} = 8.33\ \text{k}\Omega$$

$$Z_o = \frac{v_x}{i_x} = \frac{1}{\frac{1 + \beta}{R'_s + r_\pi} + \frac{1}{R_E}} = 33.2\ \Omega$$

$$A_i = A_v \frac{Z_i}{R_L} = 39.7$$

$$G = A_v A_i = 39.4$$

Exercise 4.22



From the equivalent circuit we can write: $v_{in} = -r_\pi i_b$ and $v_o = -\beta i_b R_L'$. Dividing the respective sides of these equations we obtain:

$$A_v = \frac{\beta R_L'}{r_\pi}$$

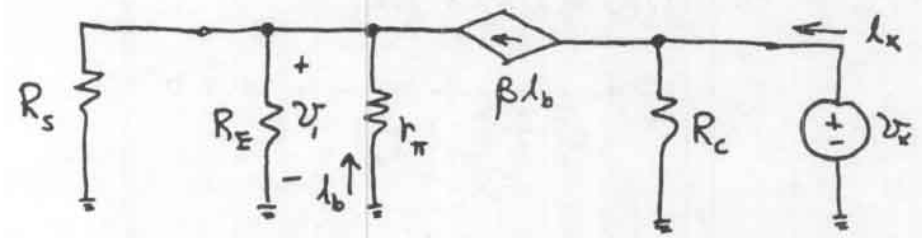
Writing a current equation at the input terminal we have:

$$i_{in} = v_{in}/R_E - (\beta + 1) i_b$$

Then we substitute $i_b = -v_{in}/r_\pi$ and rearrange to obtain:

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{1/R_E + (\beta + 1)/r_\pi}$$

The equivalent circuit for determining the output impedance is:



From the circuit we can write:

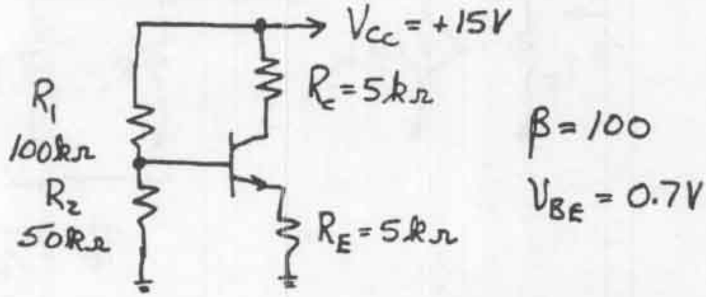
$$v_1/R_s + v_1/R_E = (\beta + 1) i_b \quad \text{and} \quad v_1 = -r_\pi i_b$$

Using the second equation to substitute into the first, we obtain $i_b = 0$. Thus the controlled source βi_b is an open circuit, and we have

$$R_o = v_x/i_x = R_C$$

Exercise 4.23

The dc circuit is:



$R_B = R_1 || R_2 = 33.3\ k\Omega$ $\quad V_B = V_{CC}R_2/(R_1 + R_2) = 5\ V$

$$I_{BQ} = \frac{V_B - V_{BEQ}}{R_B + (\beta + 1)R_E} = 7.99\ \mu A \qquad I_{CQ} = \beta I_{BQ} = 0.799\ mA$$

$r_\pi = \beta V_T/I_{CQ} = 3254\ \Omega$ $\quad R_L' = R_C || R_L = 833\ \Omega$

$A_v = \beta R_L'/r_\pi = 25.6$ $\quad R_i = R_E || [r_\pi/(\beta + 1)] = 32.0\ \Omega$

$R_o = R_C = 5\ k\Omega$ $\quad A_i = A_v R_i/R_L = 0.819$ $\quad G = A_v A_i = 21.0$

Exercise 4.24

From the equivalent circuit shown in Figure 4.40 in the book we can write:

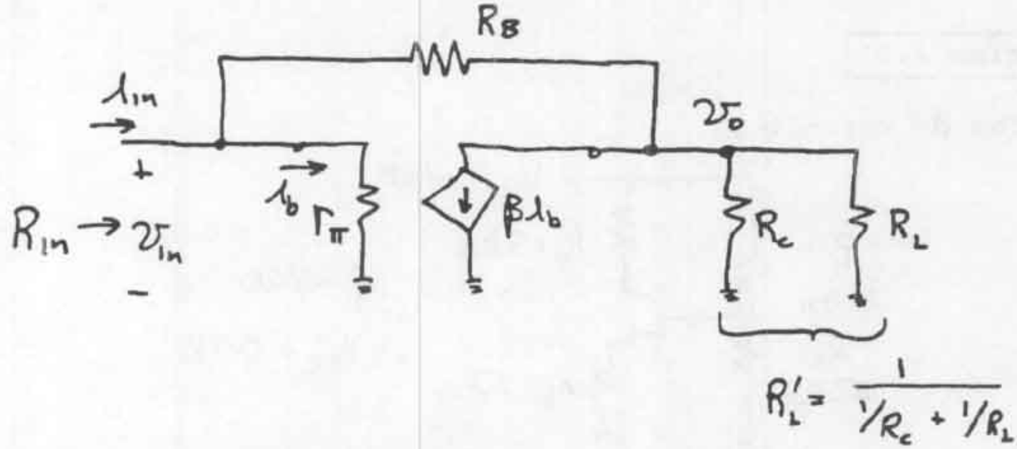
$$\frac{v_o}{R_L'} + \frac{v_o - v_{in}}{R_B} + \beta i_b = 0$$

Then using $i_b = v_{in}/r_\pi$ to substitute for i_b and rearranging the resulting equation we obtain:

$$A_v = \frac{v_o}{v_{in}} = \frac{R_L'(r_\pi - \beta R_B)}{r_\pi(R_L' + R_B)}$$

Exercise 4.25

To determine the input resistance, we use this equivalent circuit:



From the circuit we can write:

$$i_{in} = \frac{v_{in}}{r_\pi} + \frac{v_{in} - v_o}{R_B} \quad (1)$$

$$\frac{v_o}{R_L'} + \frac{v_o - v_{in}}{R_B} + \beta\frac{v_{in}}{r_\pi} = 0 \quad (2)$$

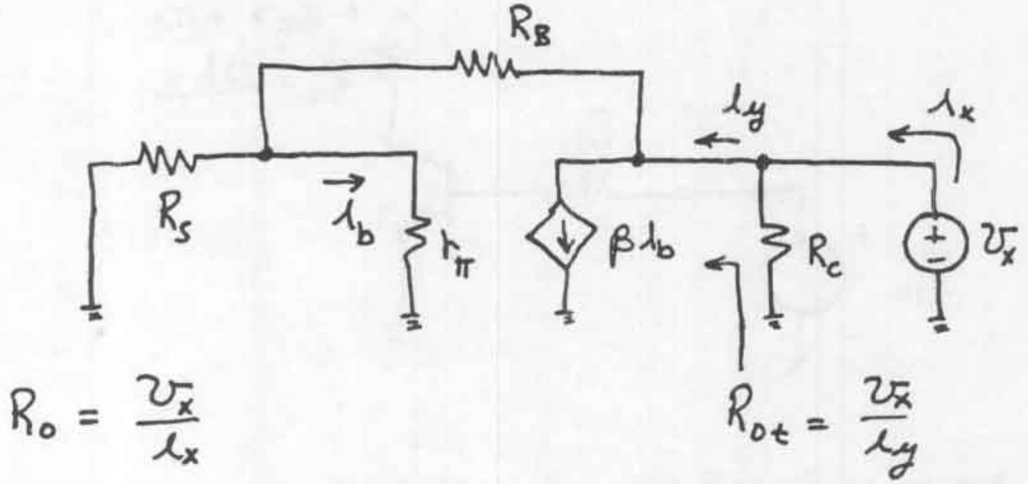
Now we solve Equation (2) for v_o, use the resulting expression to substitute for v_o in Equation (1), and rearrange the resulting equation to obtain:

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{(R_B + R_L')r_\pi}{r_\pi + R_B + (\beta + 1)R_L'}$$

To determine the output resistance, we use the equivalent circuit shown on the next page, from which we can write:

$$i_y = \frac{v_x}{R_B + R_s r_\pi/(R_s + r_\pi)} + \beta i_b \quad (3)$$

$$i_b = \frac{v_x}{R_B + R_s r_\pi/(R_s + r_\pi)} \times \frac{R_s}{R_s + r_\pi} \tag{4}$$



Now we use Equation(4) to substitute for i_b in Equation (3) and rearrange to obtain:

$$R_{ot} = \frac{R_B R_s + R_B r_\pi + R_s r_\pi}{(\beta + 1)R_s + r_\pi}$$

Finally, we have

$$R_o = R_C || R_{ot}$$

Exercise 4.26

$V_o = V_{CC} = 3$ V for $V_{in} < 0.7$ V

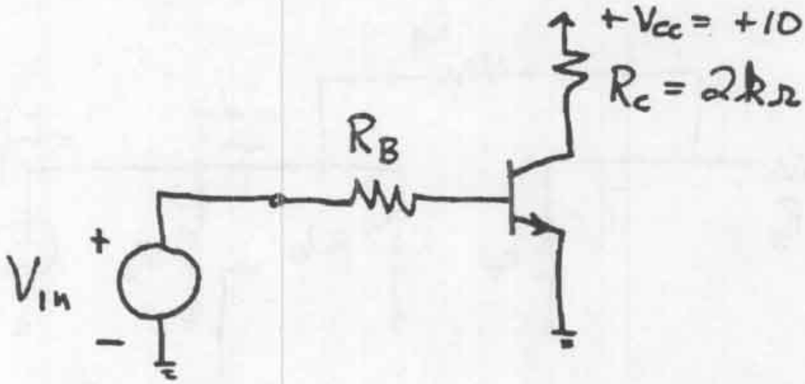
$V_o = V_{CC} - R_C\beta[(V_{in} - 0.7)/R_B]$

$= 3 - 0.4\beta(V_{in} - 0.7)$ for $V_{in} > 0.7$ and $V_o > 0.2$

$V_o = 0.2$ otherwise

The plots are shown in Figure 4.44 in the book.

Exercise 4.27



For the BJT to be in saturation, we must have:

$$\beta I_B > I_C$$

$$\beta(V_{in} - 0.7)/R_B > (V_{CC} - 0.2)/R_C$$

Substituting values and rearranging, we find

$$R_B < 8.16\ \text{k}\Omega$$

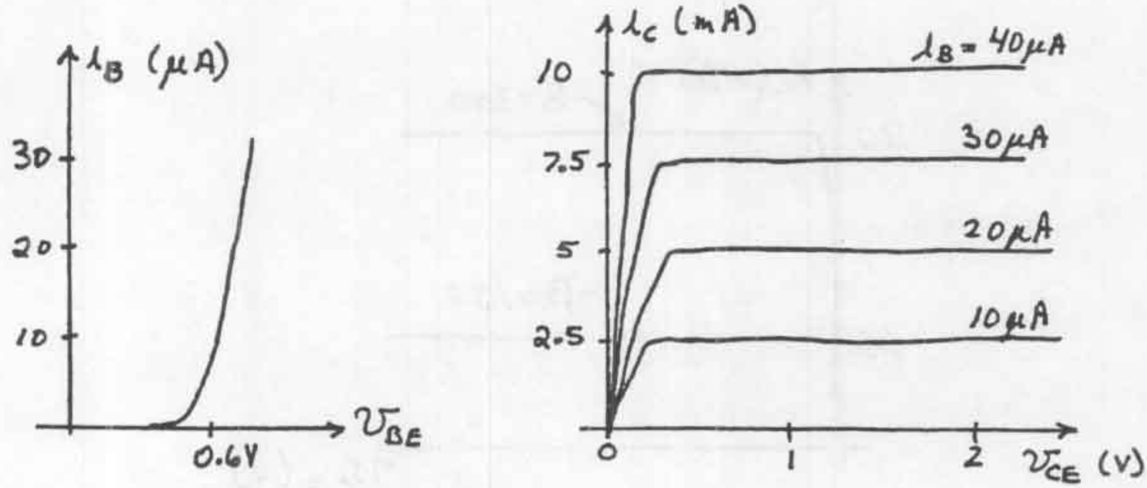
Problem 4.1

See Figure 4.1b in the book.

Problem 4.2

To forward bias a pn junction, the p-side of the junction should be connected to the positive voltage. In the active region, forward bias is applied to the emitter--base junction, and reverse bias is applied to the collector--base junction.

Problem 4.3

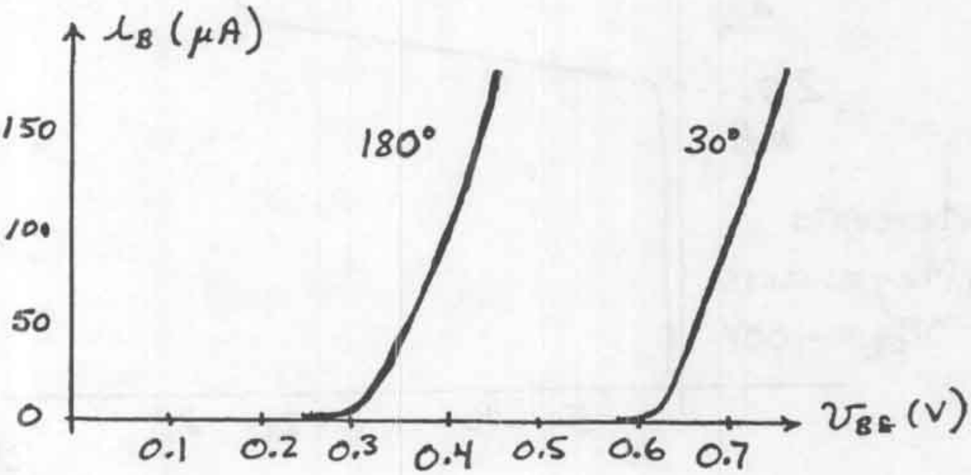


Problem 4.4

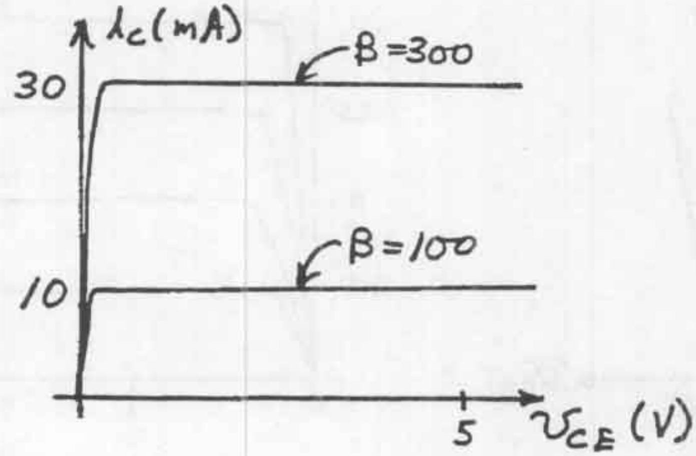
At 180°C the base-to-emitter voltage is

$$v_{BE} = 0.7 - 0.002(180 - 30) = 0.4 \text{ V}$$

Sketches of the input characteristics are shown below.



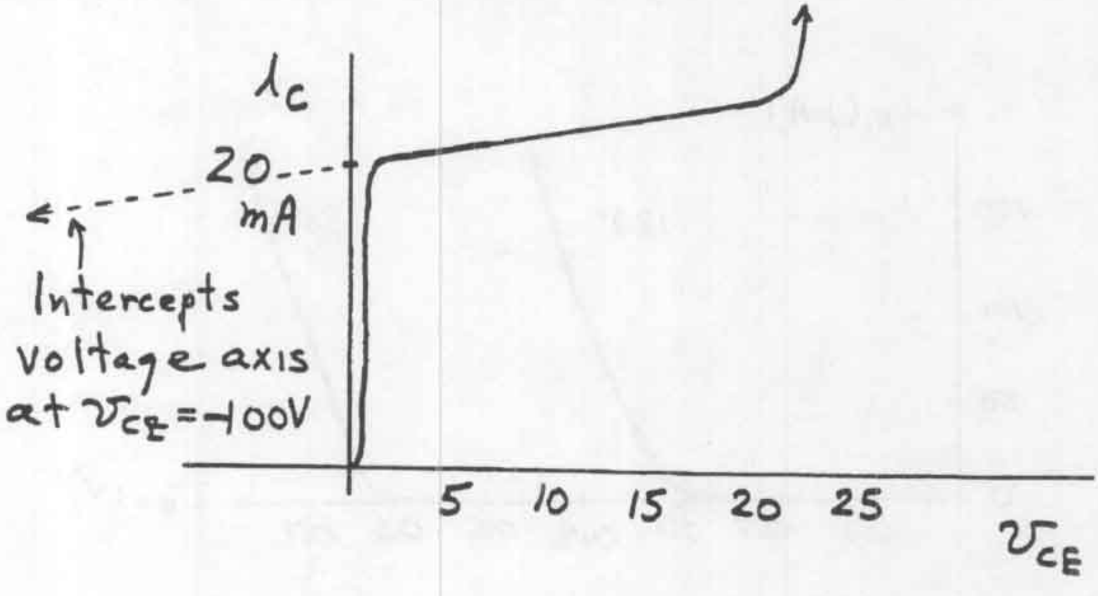
Problem 4.5



Problem 4.6

See Figure 4.5b in the book. V_A is the Early voltage and V_B is the breakdown voltage.

Problem 4.7



Problem 4.8

$$\beta = i_C/i_B = (9 \text{ mA})/(0.3 \text{ mA}) = 30$$

$$\alpha = \beta/(\beta + 1) = 30/31 = 0.9677$$

$$i_E = i_C + i_B = 9.3 \text{ mA}$$

Problem 4.9

$$\alpha = \beta/(\beta + 1) = 50/51 = 0.9804$$

Problem 4.10

Equation 4.1 in the book states

$$i_E = I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right]$$

Solving for v_{BE} we obtain

$$v_{BE} = V_T \ln(i_E/I_{ES} + 1) = 0.026\ln(10^{-2}/10^{-13} + 1) = 0.6585 \text{ V}$$

$$v_{BC} = v_{BE} - v_{CE} = 10 - 0.6585 = -9.34 \text{ V}$$

$$i_B = i_E/(\beta + 1) = 99.01\ \mu\text{A}$$

$$i_C = i_E - i_B = 9.901 \text{ mA}$$

$$\alpha = \beta/(\beta + 1) = 0.9901$$

Problem 4.11

$$I_{B2} + I_{C1} + I_{B1} = 1 \text{ mA}$$

Because the transistors are identical and have equal V_{BE}, we conclude that $I_{B2} = I_{B1}$ and $I_{C2} = I_{C1}$. Furthermore $I_{C1} = \beta I_{B1}$.

$$I_{B1} + 100I_{B1} + I_{B1} = 1 \text{ mA} \quad \Rightarrow \quad I_{B1} = 9.804\ \mu\text{A}$$

$$I_{C1} = I_{C2} = \beta I_{B1} = 0.9804 \text{ mA}$$

$$I_{E1} = (\beta + 1)I_{B1} = 0.9902 \text{ mA}$$

Solving Equation 4.1 for V_{BE} we have

$$V_{BE} = V_T \ln(I_E/I_{ES} + 1)$$

$$= 0.026\ln[(0.9902 \times 10^{-3})/10^{-14} + 1]$$

$$= 0.6583 \text{ V}$$

Problem 4.12

$$V_{BE1} = V_{BE2}$$

$$V_T \ln(I_{E1}/I_{ES1} + 1) = V_T \ln(I_{E2}/I_{ES2} + 1)$$

$$I_{E1}/I_{E2} = I_{ES1}/I_{ES2} = 0.1$$

Therefore we can write

$$I_{B1}/I_{B2} = I_{C1}/I_{C2} = 0.1$$

$$I_{B2} + I_{C1} + I_{B1} = 1 \text{ mA}$$

$$10I_{B1} + 100I_{B1} + I_{B1} = 1 \text{ mA}$$

$$I_{B1} = 9.009 \ \mu\text{A}$$

$$I_{C1} = \beta I_{B1} = 0.9009 \text{ mA}$$

$$I_{C2} = 10I_{C1} = 9.009 \text{ mA}$$

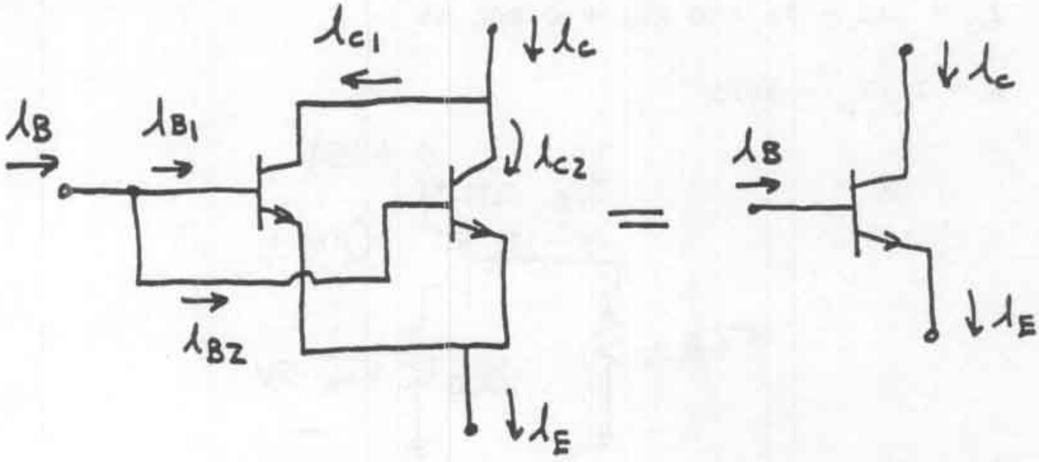
$$I_{E1} = (\beta + 1)I_{B1} = 0.9099 \text{ mA}$$

$$V_{BE2} = V_{BE1} = V_T \ln(I_{E1}/I_{ES1} + 1)$$

$$= 0.026\ln(0.9099 \times 10^{-3}/10^{-14} + 1)$$

$$= 0.6561 \text{ V}$$

Problem 4.13



Because the transistors are identical and v_{BE} is the same for both transistors, we conclude that $i_{C1} = i_{C2}$ and $i_{B1} = i_{B2}$. Thus we have

$$\beta_{eq} = \frac{i_C}{i_B} = \frac{i_{C1} + i_{C2}}{i_{B1} + i_{B2}} = \frac{2i_{C1}}{2i_{B1}} = \beta_1 = 100$$

$$i_E = i_{E1} + i_{E2}$$

$$i_E = I_{ES1}\exp(v_{BE}/V_T - 1) + I_{ES2}\exp(v_{BE}/V_T - 1)$$

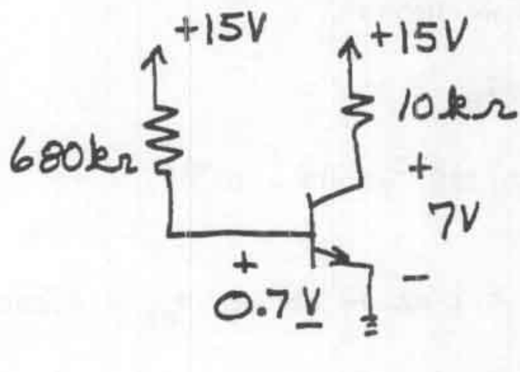
$$i_E = (I_{ES1} + I_{ES2})\exp(v_{BE}/V_T - 1) = I_{ESeq}\exp(v_{BE}/V_T - 1)$$

Thus we conclude that

$$I_{ESeq} = I_{ES1} + I_{ES2} = 2 \times 10^{-13}\text{ A}$$

Problem 4.14

(a)

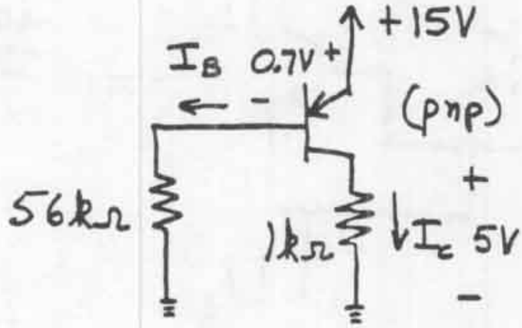


$I_B = (15 - 0.7)/(680\ k\Omega) = 21.0\ \mu A$

$I_C = (15 - 7)/(10\ k\Omega) = 0.800\ mA$

$\beta = I_C/I_B = 38.1$

(b)



$I_B = (15 - 0.7)/(56\ k\Omega) = 0.255\ mA$

$I_C = 5/(1\ k\Omega) = 5\ mA$

$\beta = I_C/I_B = 19.6$

Problem 4.15

Solving Equation 4.1 for I_{ES} we have

$$I_{ES} = \frac{I_E}{\left[\exp\left(\frac{V_{BE}}{V_T}\right) - 1\right]} = \frac{10 \times 10^{-3}}{\left[\exp\left(\frac{0.700}{0.026}\right) - 1\right]} = 2.03 \times 10^{-14}\ A$$

Then for $I_E = 1$ mA we have:

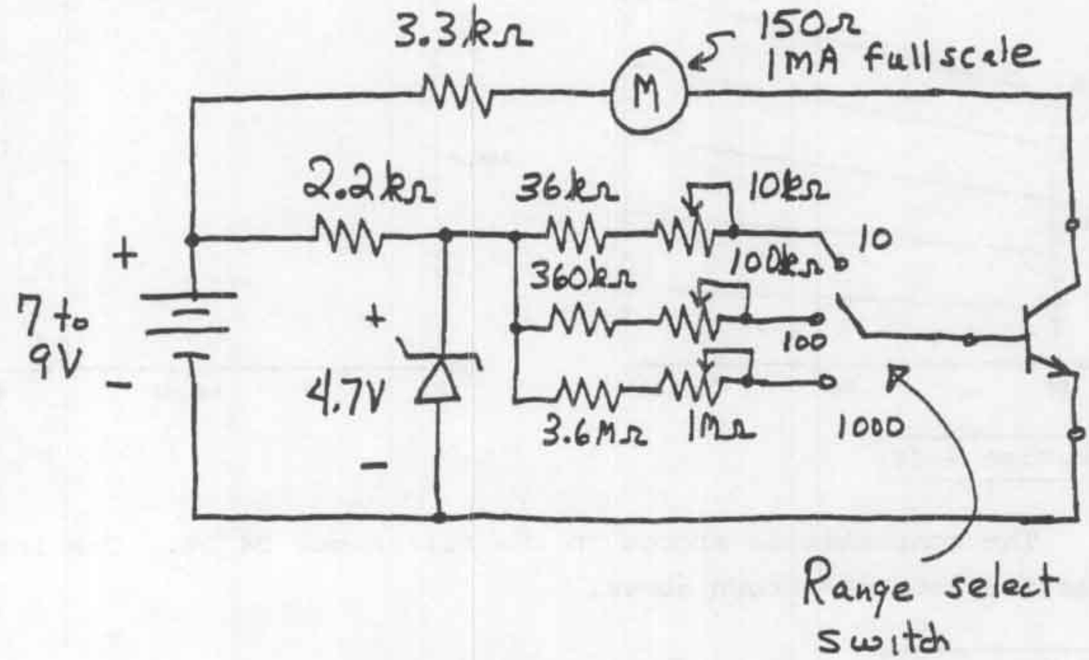
$$V_{BE} = V_T \ln(I_E/I_{ES} + 1)$$

$$= 0.026 \ln[(10^{-3}/2.03 \times 10^{-14}) + 1]$$

$$= 0.640\ V$$

Similarly for $I_E = 0.1$ mA we obtain $V_{BE} = 0.580$ V.

Problem 4.16



$$\beta = \frac{\text{meter reading}}{1\ \text{mA}} \times \beta_{\text{full-scale}}$$

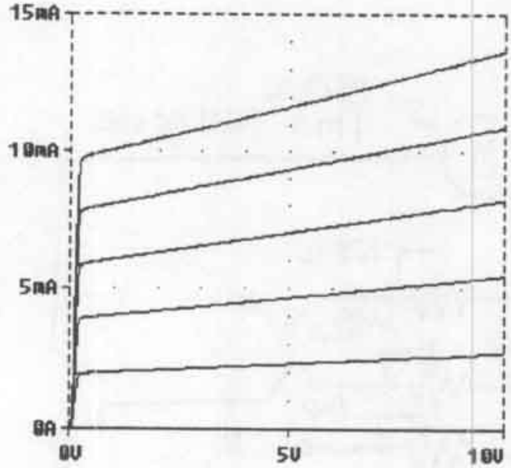
Adjust the potentiometers for $I_B = 1\ \mu A$ with the 1000 scale, $I_B = 10\ \mu A$ with the 100 scale, and $I_B = 100\ \mu A$ with the 10 scale.

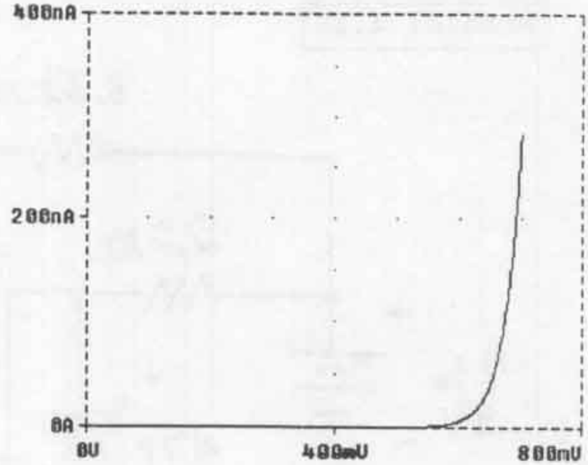
All fixed resistors are ±5% tolerance. The 3.3-kΩ resistor limits current if the test terminals are accidentally shorted together.

The 2.2 kΩ resistor and Zener diode form a voltage regulator that ensures that the base current is nearly independent of battery voltage.

Problem 4.17

The schematic is stored in the file named P4_17. The output characteristics are shown on the next page.





Problem 4.18

The schematic is stored in the file named P4_18. The input characteristic is shown above.

Problem 4.19

Distortion occurs in BJT amplifiers mainly because of the curvature of the input characteristic. Nonuniform spacing and curvature of the output characteristics also contributes to distortion. If the BJT is driven into cutoff or saturation, clipping (which is a severe form of distortion) occurs.

Problem 4.20

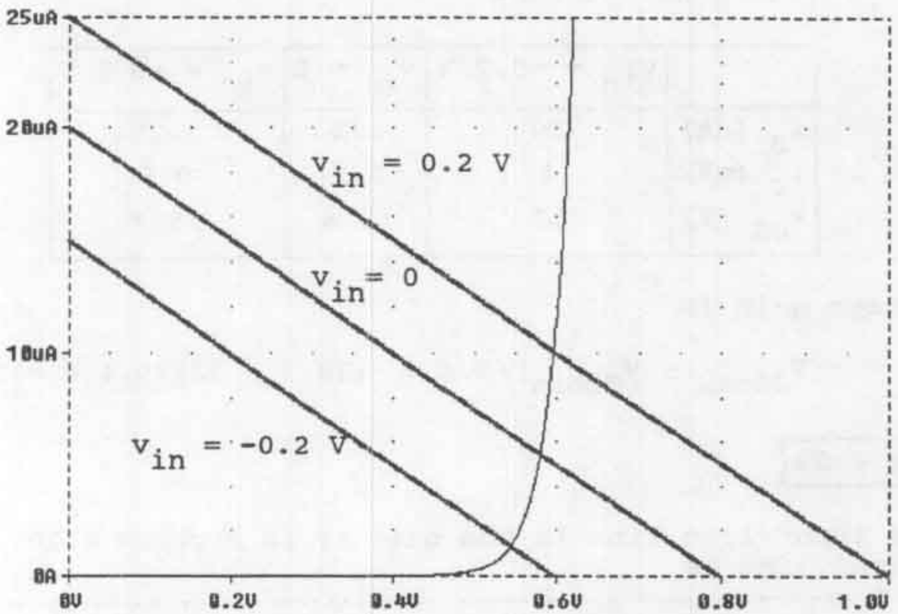
The equation for the input load line is

$$V_{BB} + v_{in}(t) = R_B i_B(t) + v_{BE}(t)$$

Substituting values we have:

$$0.8 + 0.2\sin(2000\pi t) = 40 \times 10^3 i_B + v_{BE}$$

Load lines are shown on the input characteristic:

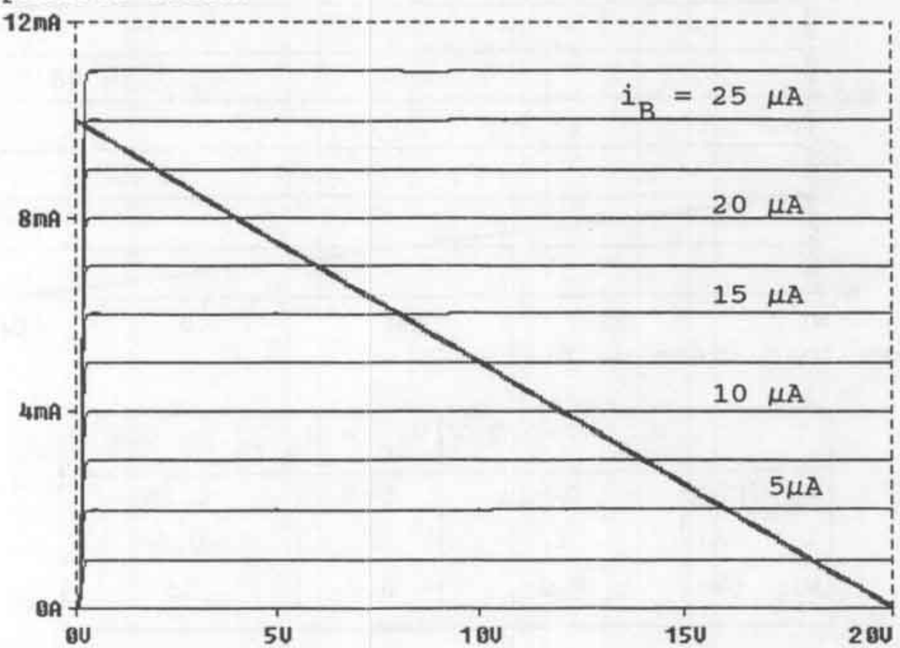


The equation for the output load line is

$$V_{CC} = R_C i_C + v_{CE}$$

$$20 = 2000 i_C + v_{CE}$$

This is plotted below:



From these load lines we find:

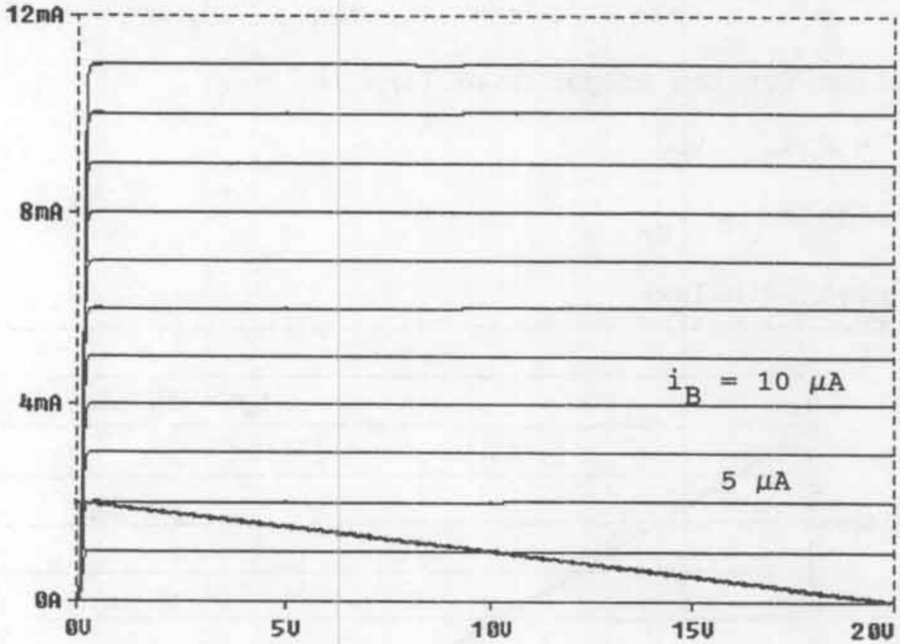
	v_{in} = +0.2 V	v_{in} = 0	v_{in} = -0.2 V
i_B (μA)	10	5.5	1.25
i_C (mA)	4	2.2	0.5
v_{CE} (V)	12	15.6	18.9

The voltage gain is

$$A_v = -(V_{CEmax} - V_{CEmin})/0.4 \cong -(18.9 - 12)/0.4 = -17.25$$

Problem 4.21

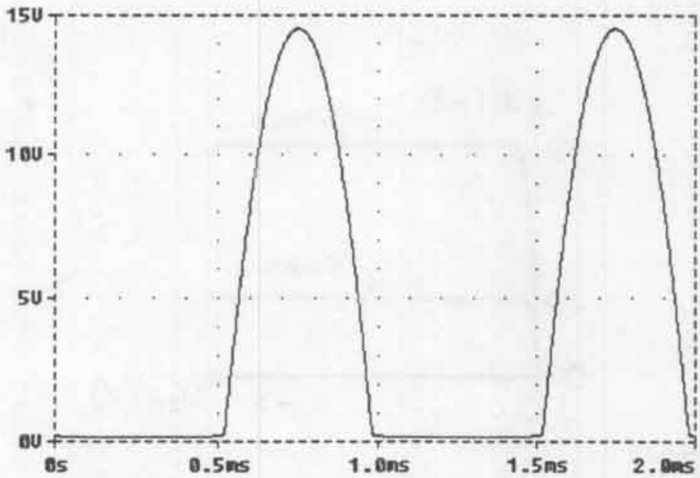
The input load line is the same as in Problem 4.20. The output load line is



From these load lines we find:

	v_{in} = +0.2 V	v_{in} = 0	v_{in} = -0.2 V
i_B (μA)	10	5.5	1.25
i_C (mA)	2	2	0.5
v_{CE} (V)	0.2	0.2	15

Because $V_{CEmin} = V_{CEQ}$ the waveform is severely distorted. The circuit schematic is stored in the file named P4_21. A plot of $v_{CE}(t)$ is:

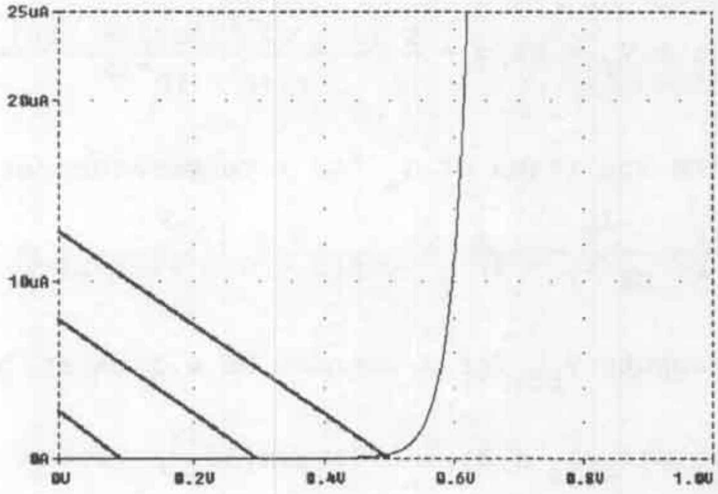


Problem 4.22

The equation for the input load line is

$$0.3 + v_{in}(t) = 40 \times 10^3 i_B + v_{BE}$$

Plotting load lines for $v_{in} = -0.2$, 0 and +0.2 V results in

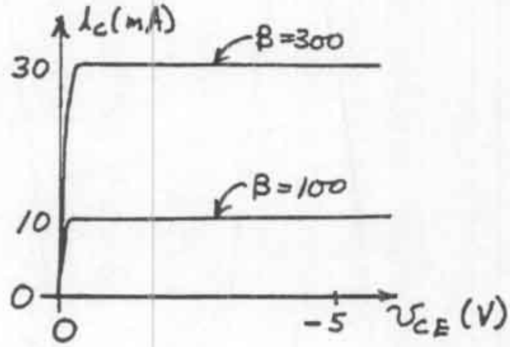


We have $I_{Bmax} \cong I_{BQ} \cong I_{Bmin}$, so there is virtually no signal at the output. Furthermore, $V_{CEmin} \cong V_{CEQ} \cong V_{CEmax} \cong 20$ V.

Problem 4.23

See Figure 4.16 in the book.

Problem 4.24



Problem 4.25

Assuming that current is constant at 2 mA we have

$$V_{BET2} = V_{BET1} + (2\text{ mV})(T_2 - T_1)$$
$$= -0.7 + 0.002(180 - 30)$$
$$= -0.4\text{ V}$$

At 180° we have $V_T = kT/q = \dfrac{1.38 \times 10^{-23}(273 + 180)}{1.60 \times 10^{-19}} = 39.1$ mV.

Now we compute the value of I_s for a temperature of 180°.

$$I_s = \frac{I_C}{\exp(V_{BE}/V_T - 1)} = \frac{2 \times 10^{-3}}{\exp(0.4/0.0391 - 1)} = 71.6\text{ nA}$$

Finally we compute V_{BE} for a current of 0.1 mA at 180°C.

$$V_{BE} = V_T \ln(I_C/I_s + 1) = 0.0391\ln[10^{-4}/(71.6 \times 10^{-9} + 1)]$$
$$= 0.283\text{ V}$$

Problem 4.26

See Figure 4.19 in the book.

Problem 4.27

See Figure 4.19 in the book.

Problem 4.28

(a) Active.
(b) Cutoff.
(c) Cutoff.
(d) Saturation.

Problem 4.29

(a) Cutoff.
(b) Saturation.
(c) Active.

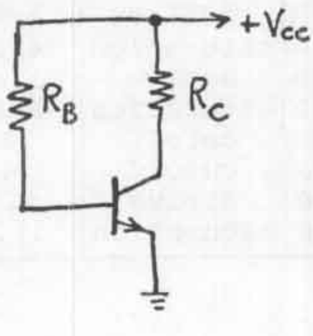
Problem 4.30

Step 1: Assume an operating region for the BJT.

Step 2: Solve the circuit to find I_C, I_B and V_{CE}.

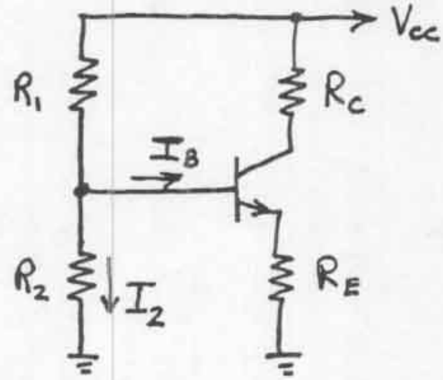
Step 3: Check to see if the values found in step 2 are consistent with the assumed operating state. If so the solution is complete, otherwise return to step 1.

Problem 4.31



The main problem with this fixed-base bias circuit is that I_B is constant with changes in β. Typically β varies by three to one between units of the same type. Thus some transistors may be biased near cutoff and others in saturation.

Problem 4.32



Design so that $V_B = V_{CC}R_2/(R_1 + R_2)$ is much greater than changes in V_{BE} from unit to unit and with temperature. Select component values so I_2 is much greater than I_B. A commonly used design rule is to pick I_2 ten to twenty times the nominal value of I_B. Another common design rule is to choose components so that V_{CE} and the voltages across R_C and R_E are each approximately one-third of V_{CC}.

Problem 4.33

Circuit	β	Region	I_C (mA)	V_{CE} (V)
(a)	100	active	1.93	10.9
(a)	300	saturation	4.21	0.2
(b)	100	active	1.47	5.00
(b)	300	saturation	2.18	0.2
(c)	100	cutoff	0	15
(c)	300	cutoff	0	15
(d)	100	active	6.5	8.5
(d)	300	saturation	14.8	0.2

Problem 4.34

Circuit	β	Region	I (mA)	V (V)
(a)	100	active	2.38	5.25
(a)	300	saturation	4.45	9.80
(b)	100	cutoff	0	10
(b)	300	cutoff	0	10
(c)	100	active	4.26	-10.74
(c)	300	active	4.29	-10.71
(d)	100	Q_1 active Q_2 active	10	10
(d)	300	Q_1 active Q_2 saturation	14.8	14.8

Problem 4.35

From the circuit we can write:

$$5 = R_B I_B + R_E I_E + 0.7$$

Using $I_E = I_C(\beta + 1)/\beta$ and $I_B = I_C/\beta$ to substitute and rearranging:

$$4.3 = R_B I_C/\beta + R_E I_C(\beta + 1)/\beta$$

Now we want $I_C = 4$ mA when $\beta = 100$ and $I_C = 5$ mA when $\beta = 300$. Thus we have the following two equations.

$$4.3 = 0.04R_B + 4.04R_E$$

$$4.3 = 0.01667R_B + 5.017R_E$$

Solving we find $R_B = 31.5$ kΩ and $R_E = 753$ Ω.

Problem 4.36

For the four-resistor bias circuit we have:

$$R_B = R_1 || R_2$$

$$V_B = V_{CC} \frac{R_2}{R_1 + R_2}$$

$$I_C = \beta I_B = \beta \frac{V_B - V_{BE}}{R_B + (\beta + 1)R_E}$$

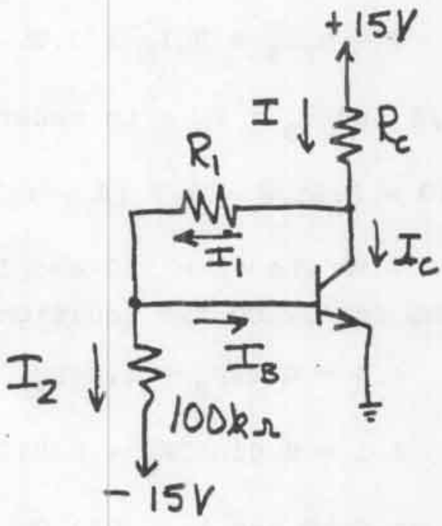
Maximum I_C occurs for $\beta = 200$, $R_E = 0.95R_{Enom} = 4.465$ kΩ, $R_1 = 0.95R_{1nom} = 95$ kΩ, and $R_2 = 1.05R_{2nom} = 49.35$ kΩ. With these values, we determine that $I_{Cmax} = 0.952$ mA.

Minimum I_C occurs for $\beta = 50$, $R_E = 1.05R_{Enom} = 4.935$ kΩ, $R_1 = 1.05R_{1nom} = 105$ kΩ, and $R_2 = 0.95R_{2nom} = 44.65$ kΩ. With these values, we determine that $I_{Cmin} = 0.667$ mA.

Problem 4.37

$V_{BE} = 0.7$ V

$\beta = 100$



$I_2 = \dfrac{15 + 0.7}{100\ \text{k}\Omega} = 157\ \mu A$

$I_B = I_C/\beta = (2\ \text{mA})/100 = 20\ \mu A$

$I_1 = I_2 + I_B = 177\ \mu A$

$R_1 = (V_{CE} - V_{BE})/I_1 = 24.3$ kΩ

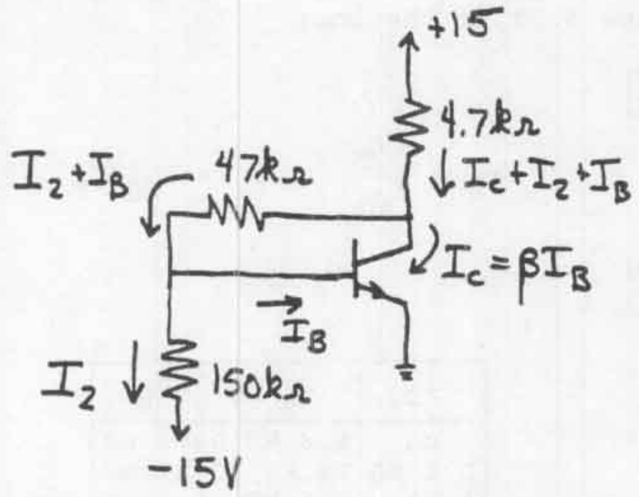
$I = I_C + I_1 = 2.177$ mA

$R_C = (V_{CC} - V_{CE})/I = 4.59$ kΩ

The closest nominal values are $R_1 = 24$ kΩ and $R_C = 4.7$ kΩ.

Problem 4.38

$V_{BE} = 0.7$ V
$\beta = 200$



$$I_2 = (15 + 0.7)/(150\ k\Omega) = 104\ \mu A$$

$$15 = (4.7\ k\Omega)(I_C + I_2 + I_B) + (47\ k\Omega)(I_2 + I_B) + 0.7$$

Substituting $I_C = \beta I_B$ and solving we find $I_B = 8.96\ \mu A$. Then we have $I_C = \beta I_B = 1.79$ mA. Finally we have

$$V_{CE} = V_{CC} - R_C(I_C + I_2 + I_B) = 6.04\ V$$

Problem 4.39

Many answers exist for this problem. Here is one of them:

We use $\beta = 100$ (which is the average value) in the design calculations. We design so $V_{CE} = 20/3 = 6.67$ V, $R_E I_E = 6.67$ V and $R_C I_C = 6.67$ V. Then we have $R_C = 6.67/I_C = 1.333$ kΩ and $R_E = 6.67/I_E \cong 6.67/I_C = 1.333$ kΩ. We select the closest nominal values of 1.3 kΩ.

We have $V_2 = V_{BE} + I_E R_E = 0.7 + 6.67 = 7.37$ V. $I_B = I_C/\beta = 50\ \mu A$. We design so that $I_2 = 20 I_B = 1$ mA. Then we have $R_2 = V_2/I_2 = 7.37$ kΩ and $R_1 = (V_{CC} - V_2)/(I_2 + I_B) = 12.03$ kΩ. Finally we select the nominal values $R_2 = 7.5$ kΩ and $R_1 = 12$ kΩ.

Problem 4.40

See Figure 4.33 in the book.

Problem 4.41

$$r_\pi = \frac{\beta V_T}{I_{CQ}} \qquad g_m = I_{CQ}/V_T$$

Problem 4.42

I_{CQ}	r_π	g_m
1 μA	2.6 MΩ	38.5 μS
0.1 mA	26 kΩ	3.85 mS
1 mA	2.6 kΩ	38.5 mS

Problem 4.43

Coupling capacitors are often used in discrete amplifiers so the source and load do not have dc currents flowing through them and so the bias points in the amplifier are independent of the source and the load. We must not use coupling capacitors if it is necessary to amplify dc signals because the coupling capacitors act as open circuits for dc.

Problem 4.44

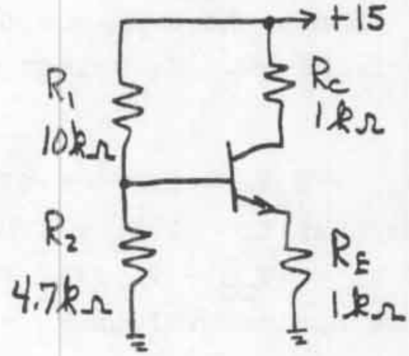
See Figure 4.34(a) in the book.

Problem 4.45

Dc circuit:

$\beta = 100$

$V_{BEQ} = 0.7$ V



$V_B = V_{CC}R_2/(R_1 + R_2) = 4.80$ V $\quad R_B = R_1||R_2 = 3.20$ kΩ

$$I_{BQ} = \frac{V_B - V_{BEQ}}{R_B + (\beta + 1)R_E} = 0.0393 \text{ mA} \qquad I_{CQ} = \beta I_B = 3.93 \text{ mA}$$

$r_\pi = \beta V_T/I_{CQ} = 662\ \Omega \qquad R_L' = R_L||R_C = 500\ \Omega$

$A_v = -\beta R_L'/r_\pi = -75.5 \qquad A_{vo} = -\beta R_L/r_\pi = -151$

$Z_{in} = R_1||R_2||r_\pi = 548\ \Omega \qquad A_i = A_v Z_{in}/R_L = -41.4$

$G = A_v A_i = 3124 \qquad Z_o = R_C = 1$ kΩ

Problem 4.46

	High-impedance amplifier	Low-impedance amplifier (Problem 4.45)
I_{CQ}	39.3 μA	3.93 mA
r_π	66.2 kΩ	662 Ω
A_v	-75.5	-75.5
A_{vo}	-151	-151
Z_{in}	54.8 kΩ	548 Ω
A_i	-41.4	-41.4
G	3124	3124
Z_o	100 kΩ	1 kΩ

Problem 4.47

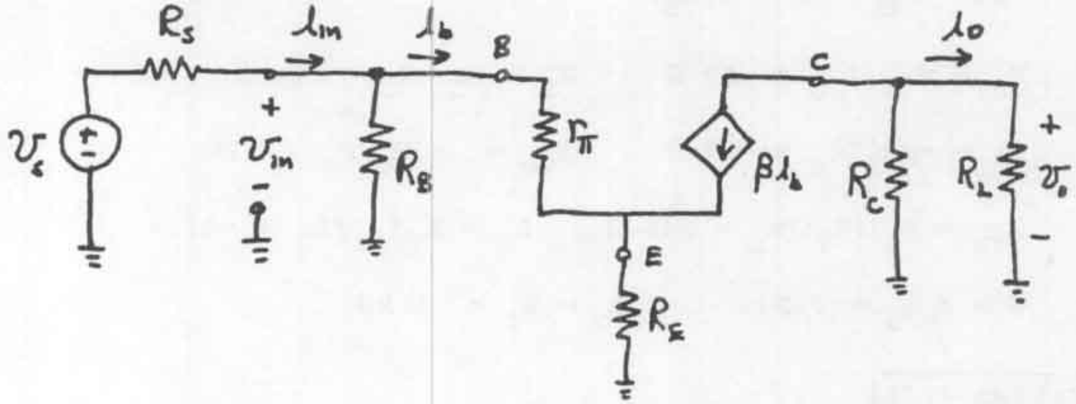
See Figure 4.36a in the book.

Problem 4.48

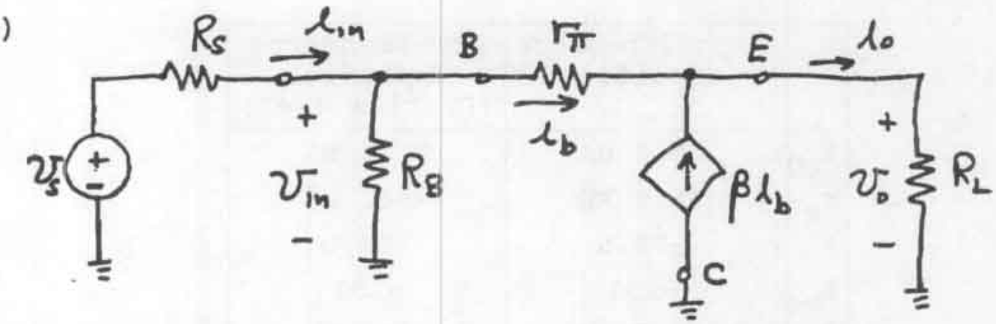
In a small-signal midband analysis of an amplifier we replace coupling capacitors and dc voltage sources by short circuits. We replace dc current sources and large inductances by open circuits.

Problem 4.49

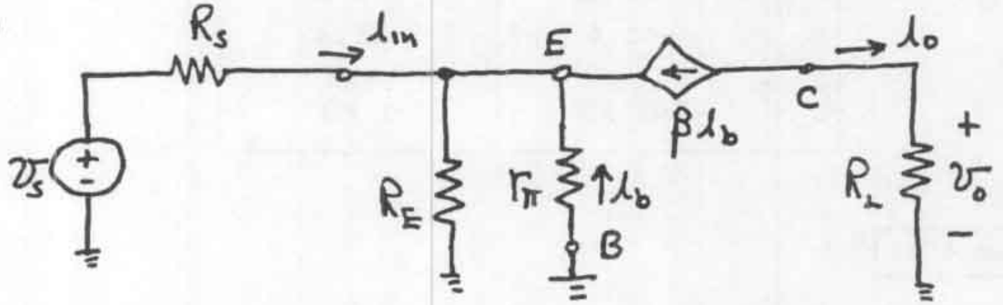
(a)



(b)



(c)



Problem 4.50

To determine the output resistance of an amplifier:

1. Replace the load with a test voltage (or current) source.

2. Write circuit equations involving the current i_x and voltage v_x of the test source.

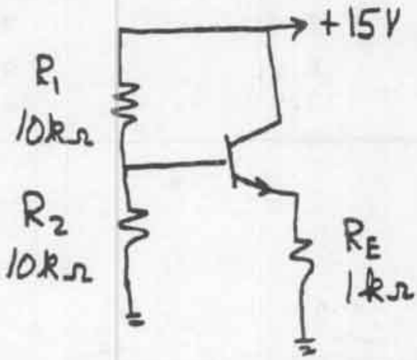
3. Eliminate current and voltage variables until one equation remains that relates i_x and v_x.

4. The output impedance is $Z_o = v_x/i_x$.

Problem 4.51

Dc circuit:

$V_{BEQ} = 0.7$ V
$\beta = 100$



$$V_B = V_{CC}R_2/(R_1 + R_2) = 7.5 \text{ V} \qquad R_B = R_1 || R_2 = 5 \text{ k}\Omega$$

$$I_{BQ} = \frac{V_B - V_{BEQ}}{R_B + (\beta + 1)R_E} = 64.1\ \mu\text{A} \qquad I_{CQ} = \beta I_B = 6.41 \text{ mA}$$

$$r_\pi = \beta V_T/I_{CQ} = 405\ \Omega \qquad R_L' = R_L || R_E = 333\ \Omega$$

$$A_v = \frac{R_L'(\beta + 1)}{r_\pi + R_L'(\beta + 1)} = 0.988 \qquad A_{vo} = \frac{R_E(\beta + 1)}{r_\pi + R_E(\beta + 1)} = 0.996$$

$$Z_{in} = R_B || [r_\pi + R_L'(\beta + 1)] = 4.36 \text{ k}\Omega$$

$$A_i = A_v Z_{in}/R_L = 8.61 \qquad G = A_v A_i = 8.51$$

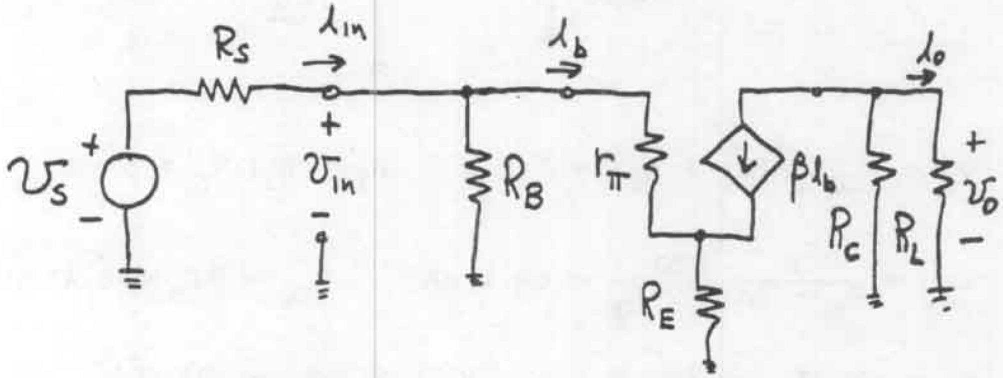
$$R_s' = R_B || R_s = 833\ \Omega$$

$$Z_o = R_E || [(R_s' + r_\pi)/(\beta + 1)] = 12.1\ \Omega$$

Problem 4.52

	High-impedance emitter follower	Low-impedance emitter follower (Problem 4.51)
I_{CQ}	64.1 μA	6.41 mA
r_π	40.5 kΩ	405 Ω
A_v	0.988	0.988
A_{vo}	0.996	0.996
Z_{in}	436 kΩ	4.36 kΩ
A_i	8.61	8.61
G	8.51	8.51
Z_o	1210 Ω	12.1 Ω

Problem 4.53



$$A_v = \frac{v_o}{v_{in}} = \frac{-\beta R_L'}{r_\pi + (\beta + 1)R_E} \qquad \text{where } R_L' = R_C || R_L$$

$$Z_{in} = R_B || [r_\pi + (\beta + 1)R_E]$$

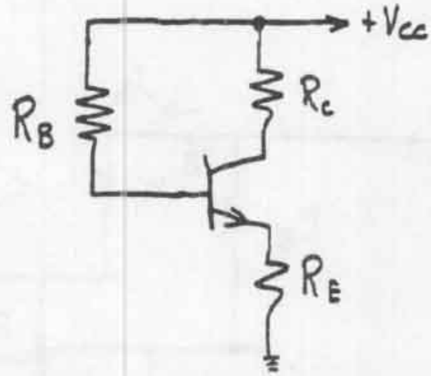
Problem 4.54

The dc equivalent circuit is shown on the next page. We have:

$$I_{BQ} = \frac{V_{CC} - V_{BEQ}}{R_B + (\beta + 1)R_E} \qquad I_{CQ} = \beta I_{BQ} \qquad r_\pi = \frac{\beta V_T}{I_{CQ}}$$

Dc circuit:

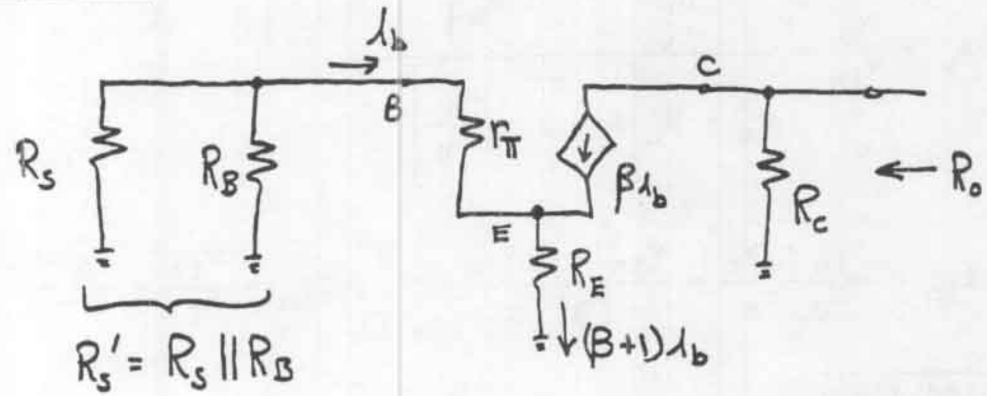
$V_{EQ} = 0.7$ V
$\beta = 100$



	$R_E = 0$	$R_E = 100\ \Omega$
I_{CQ}	5.30 mA	5.12 mA
r_π	491 Ω	509 Ω
A_v	-102	-4.76
Z_{in}	490 Ω	10.1 kΩ

Notice the dramatic effect of the 100-Ω emitter resistance on voltage gain and input impedance.

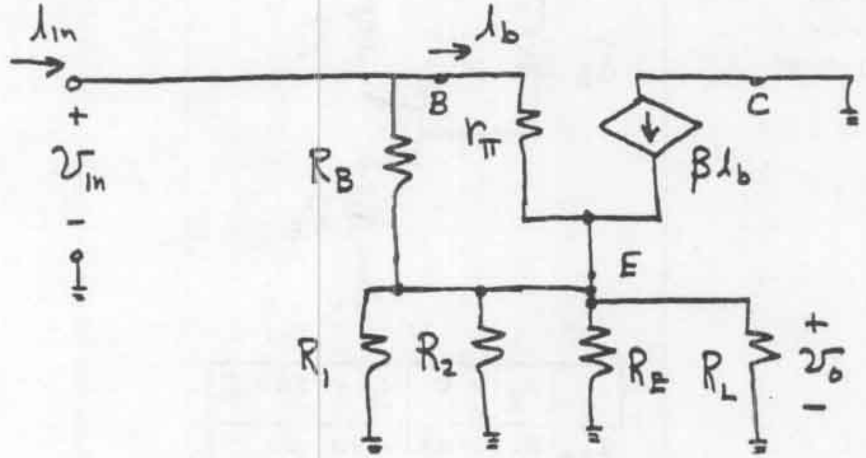
Problem 4.55



$$R'_S i_b + r_\pi i_b + (\beta + 1) R_E i_b = 0 \quad \Rightarrow \quad i_b = 0$$

Therefore we conclude that the βi_b acts as an open circuit and we have $R_o = R_C$.

Problem 4.56



Let $R_L' = R_1||R_2||R_E||R_L$

$$v_o = R_L'\left(i_b + \beta i_b + \frac{r_\pi i_b}{R_B}\right) \qquad v_{in} = r_\pi i_b + v_o$$

$$A_v = \frac{v_o}{v_{in}} = \frac{R_L'\left(1 + \beta + \frac{r_\pi}{R_B}\right)}{r_\pi + R_L'\left(1 + \beta + \frac{r_\pi}{R_B}\right)}$$

$$i_{in} = \frac{v_{in} - v_o}{R_B||r_\pi} = \frac{v_{in} - A_v v_{in}}{R_B||r_\pi} \qquad Z_{in} = \frac{v_{in}}{i_{in}} = \frac{R_B||r_\pi}{1 - A_v}$$

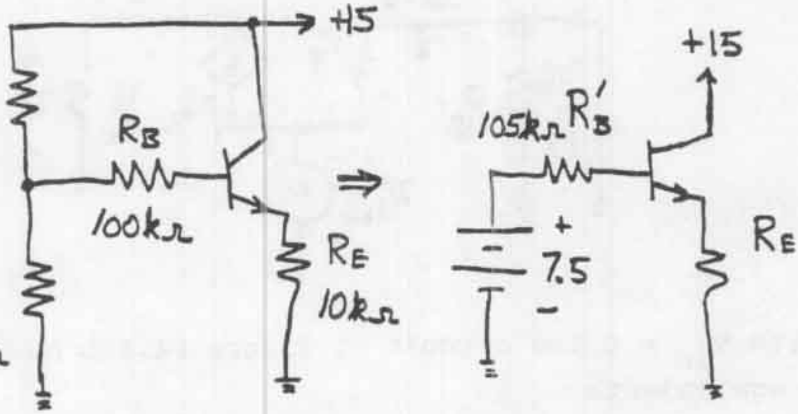
Problem 4.57

See the next page for the dc equivalent circuit from which we have:

$$I_{BQ} = (7.5 - V_{BEQ})/[R_B' + (\beta + 1)R_E] = 3.21\ \mu A$$

$$I_{CQ} = \beta I_{BQ} = 0.643\ \text{mA} \qquad r_\pi = \beta V_T/I_{CQ} = 8.09\ \text{k}\Omega$$

$\beta = 200$
$V_{BEQ} = 0.7$ V



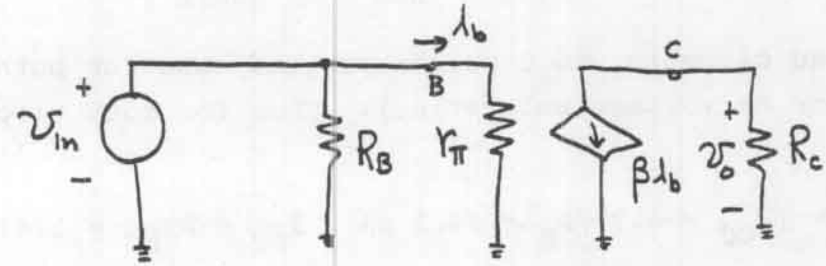
Then using the formulas from Problem 4.56, we have:

$$R'_L = R_1||R_2||R_E||R_L = 1.95\ k\Omega$$

$$A_v = 0.9798 \qquad Z_{in} = 370\ k\Omega$$

Problem 4.58

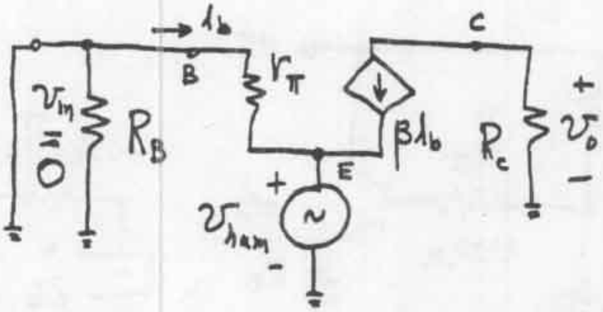
With $v_{hum} = 0$, both circuits have the same small-signal equivalent:



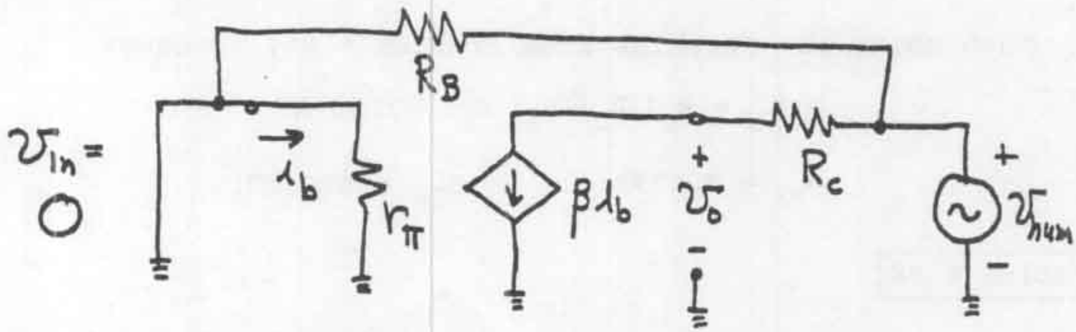
From this equivalent circuit we find:

$$A_v = v_o/v_{in} = -\beta R_C/r_\pi$$

With $v_{in} = 0$ the circuit of Figure P4.58a has the small-signal equivalent shown on the next page, from which we find that $A_{hum,a} = v_o/v_{hum} = \beta R_C/r_\pi$.



With $v_{in} = 0$ the circuit of Figure P4.58b has the small-signal equivalent:



Notice that $i_b = 0$, thus $\beta i_b = 0$, and there is zero voltage across R_C. Consequently $v_o = v_{hum}$ and $A_{hum,b} = 1$.

The dc circuits and Q-points are the same for both circuits (except for dc voltage polarities). Thus for both circuits we have:

$I_{BQ} = (V_{CC} - 0.7)/R_B = 14.3\ \mu A \quad I_{CQ} = \beta I_{BQ} = 1.43\ mA$

$r_\pi = \beta V_T/I_{CQ} = 1820\ \Omega$

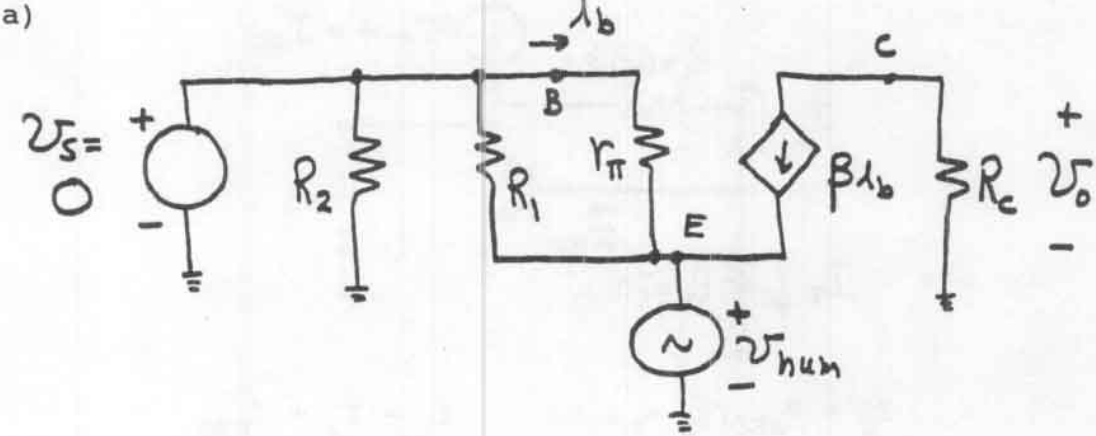
Calculating the gains of the two circuits we have:

	Circuit (a)	Circuit (b)
A_v	-258	-258
A_{hum}	258	1

Circuit (b) is preferable because it is much less sensitive to power-supply hum.

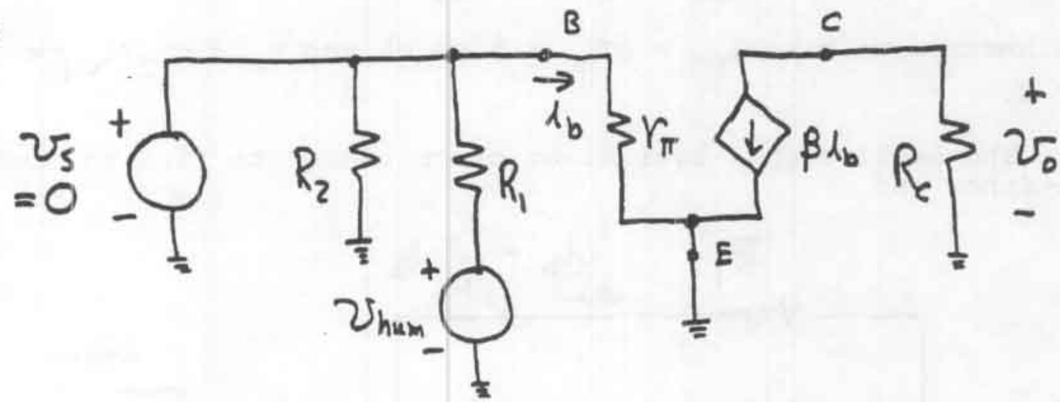
Problem 4.59

(a)



$$A_{hum} = \frac{v_o}{v_{hum}} = \frac{-\beta i_b R_C}{-r_\pi i_b} = \frac{\beta R_C}{r_\pi}$$

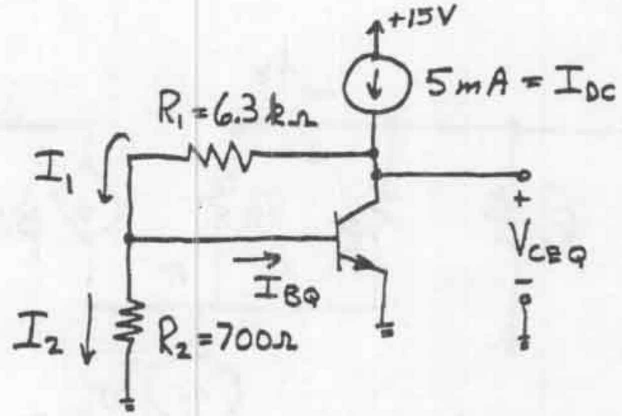
(b)



Because $v_s = 0$ we have $i_b = 0$ and $v_o = 0$. Thus $A_{hum} = 0$.

Because of lower sensitivity to power-supply hum, the circuit of Figure P4.59b is preferable to that of Figure P4.59a. In other words, the emitter bypass capacitor should be connected from emitter to ground.

Problem 4.60



$$I_2 = V_{BEQ}/R_2 = 1 \text{ mA} \qquad I_1 = I_2 + I_{BEQ}$$

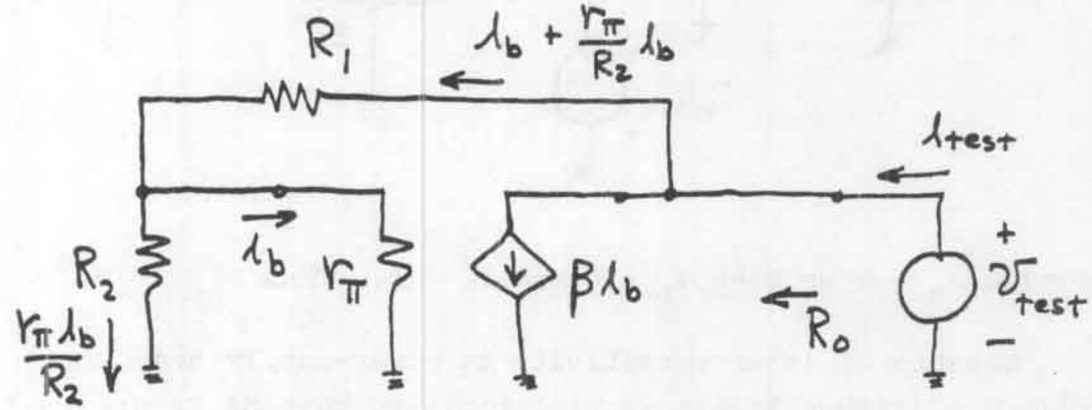
$$5 \text{ mA} = I_1 + I_{CQ} = I_2 + (\beta + 1)I_{BQ}$$

Using the first two equations to substitute for I_1 and I_2 and solving, we find $I_{BQ} = 39.6\ \mu A$. Then we have

$$V_{CEQ} = R_1 I_1 + V_{BEQ} = 7.25 \text{ V}$$

Furthermore we have $I_{CQ} = \beta I_{BQ} = 3.96$ mA and $r_\pi = \beta V_T/I_{CQ} = 657\ \Omega$.

The small signal equivalent circuit used to find the output impedance is:



$$v_{test} = R_1(i_b + r_\pi i_b/R_2) + r_\pi i_b$$

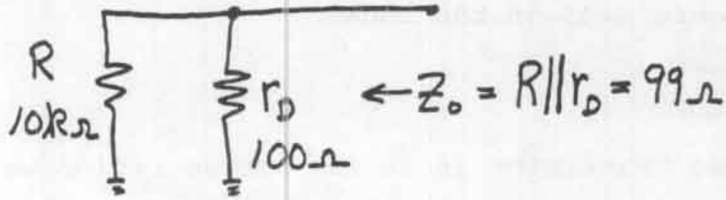
$$i_{test} = \beta i_b + i_b + r_\pi i_b/R_2$$

$$R_o = \frac{v_{test}}{i_{test}} = \frac{r_\pi + R_1(1 + r_\pi/R_2)}{1 + \beta + r_\pi/R_2} = 126\ \Omega$$

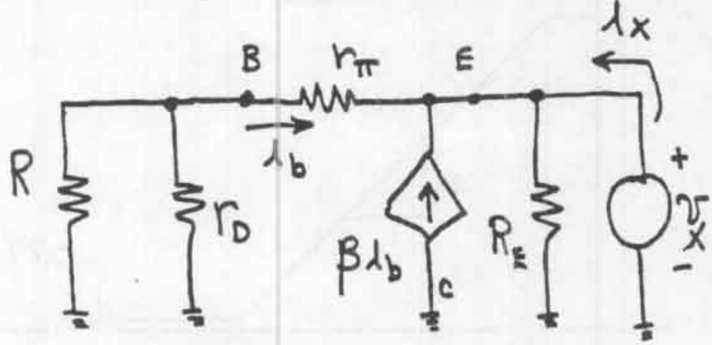
This circuit is sometimes used as a voltage reference (similar to a Zener diode regulator).

Problem 4.61

(a) For this circuit we have $V_o = 5.1$ V. The small-signal equivalent circuit is:



(b) For this circuit we have $V_o = 5.6 - V_{BEQ} = 4.9$ V. Furthermore, we have $I_{CQ} \cong I_{EQ} = V_o/R_E = 4.9$ mA and $r_\pi = \beta V_T/I_{CQ} = 1060\ \Omega$. The small-signal equivalent circuit is:



Let $r'_D = r_D || R = 99.0\ \Omega$, then we have:

$$i_b = -v_x/(r_\pi + r'_D)$$

$$i_x = -(\beta + 1)i_b + v_x/R_E$$

Using the first equation to substitute into the second and solving we find:

$$Z_o = \frac{v_x}{i_x} = \frac{1}{1/R_E + (\beta + 1)/(r_\pi + r'_D)} = 5.74\ \Omega$$

Circuit (b) is a better voltage reference because Z_o is much smaller.

Problem 4.62

See Figure 4.41 in the book. The transistor operates in saturation if the input is high and in cutoff if the input is low.

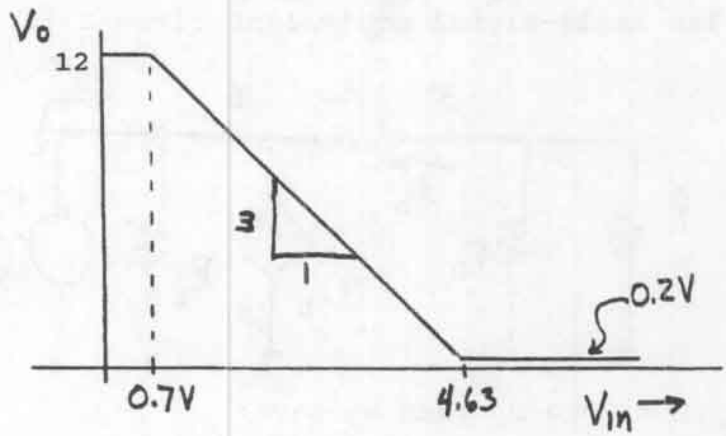
Problem 4.63

See Figure 4.45 in the book.

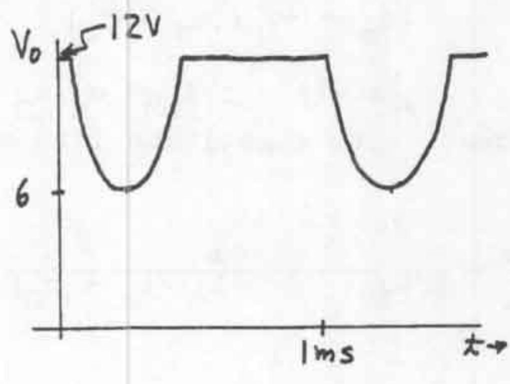
Problem 4.64

When the transistor is in the active region we have:

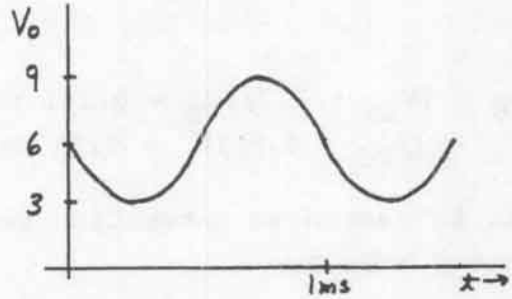
$$V_o = V_{CC} - R_C\beta\frac{V_{in} - 0.7}{R_B} = 14.1 - 3V_{in}$$



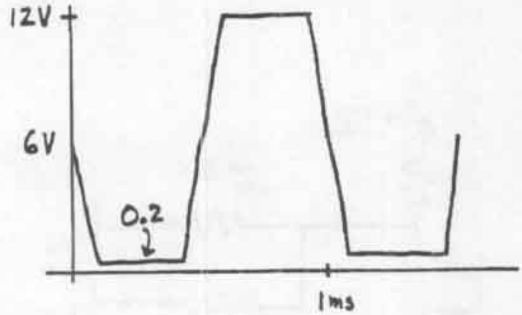
(a)



(b)

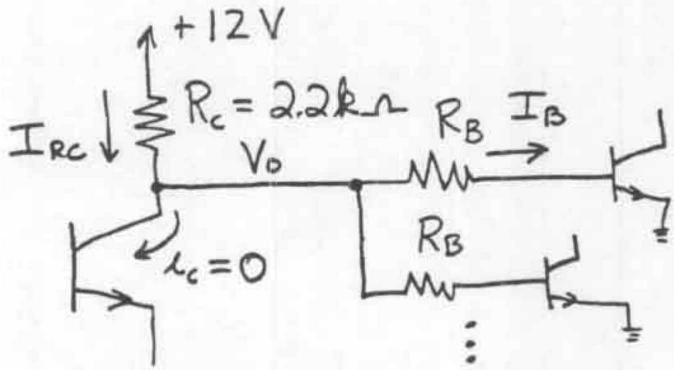


(c)



(d) In part (b) the circuit acts as a linear amplifier.

Problem 4.65



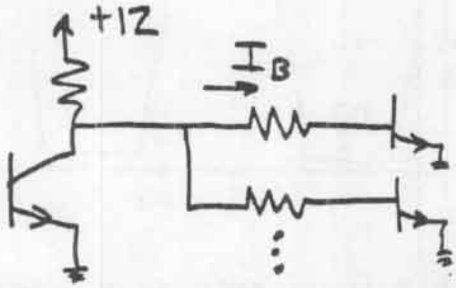
For V_o = 6 V we have I_{RC} = (12 - 6)/R_C = 2.73 mA and I_B (6 - 0.7)/(22 kΩ) = 0.241 mA. Thus the maximum fanout is the largest integer that does not exceed I_{RC}/I_B = 11.33. Thus the maximum fanout is 11.

Problem 4.66

$$I_B = (V_{in} - 0.7)/R_B = 0.241 \text{ mA}$$
$$I_C = (V_{CC} - 0.2)/R_C = 5.37 \text{ mA}$$

For the circuit to remain in saturation we must have $\beta I_B > I_C$ which implies that $\beta > 22.3$.

Problem 4.67



For $V_o = 0.5$ V, we have $I_B = 0$. Therefore there is no limit on fanout imposed by the conditions of this problem.

Chapter 5

Exercise 5.1

(a) $v_{GS} = 1$ V and $v_{DS} = 5$ V: Because we have $v_{GS} < V_{to}$ the FET is in cutoff.

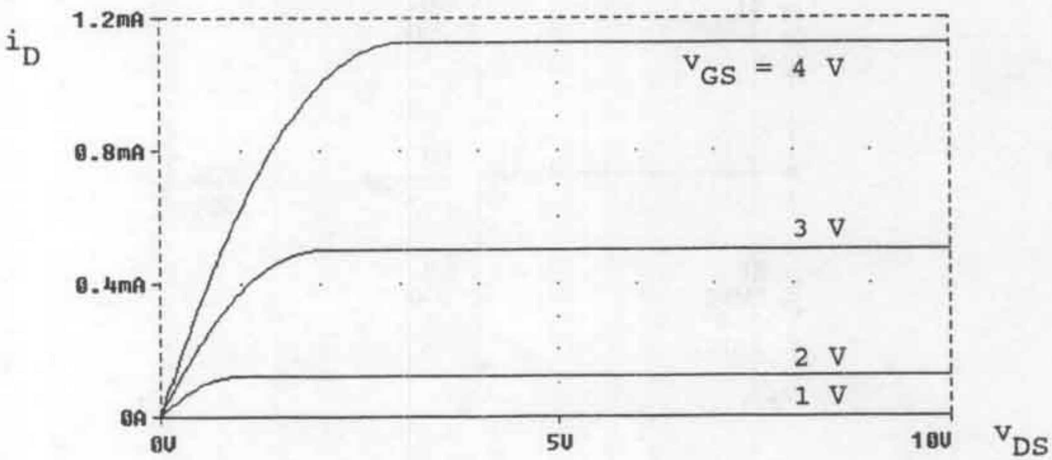
(b) $v_{GS} = 3$ V and $v_{DS} = 0.5$ V: Because $v_{GS} > V_{to}$ and $v_{GD} = v_{GS} - v_{DS} = 2.5 > V_{to}$ the FET is in the triode region.

(c) $v_{GS} = 3$ V and $v_{DS} = 6$ V: Because $v_{GS} > V_{to}$ and $v_{GD} = v_{GS} - v_{DS} = -3$ V $< V_{to}$ the FET is in the saturation region.

(d) $v_{GS} = 5$ V and $v_{DS} = 6$ V: Because $v_{GS} > V_{to}$ and $v_{GD} = v_{GS} - v_{DS} = 1$ V which is less than V_{to} the FET is in the saturation region.

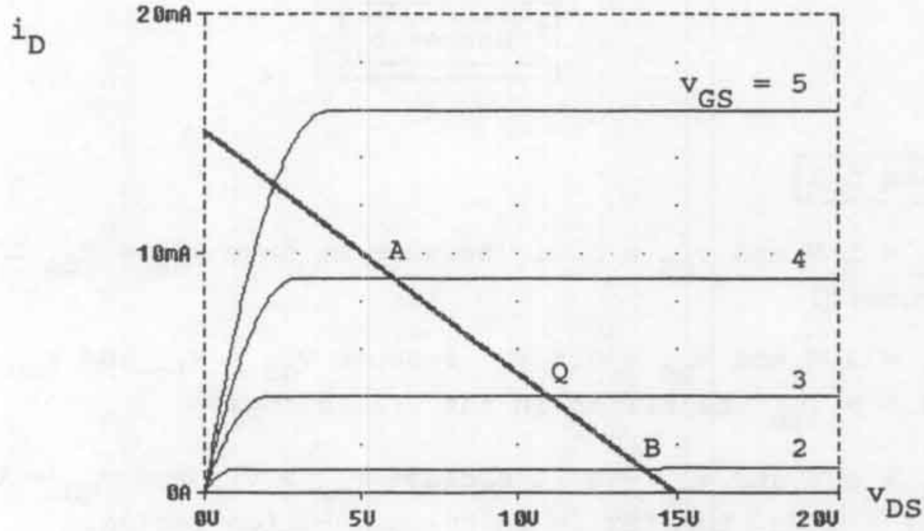
Exercise 5.2

The simulation is stored in the file named Exer5_2. The plots are:



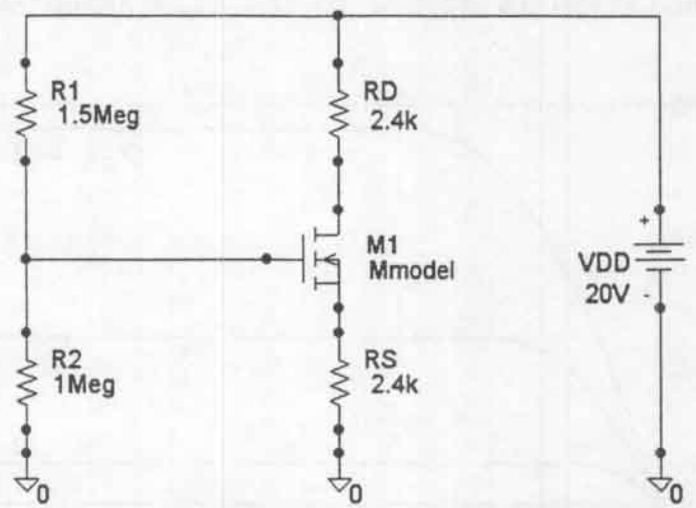
Exercise 5.3

The characteristics and the load line are shown on the next page. The simulation is stored in the file named Exer5_3.



For v_{in} = +1 we have v_{GS} = 4 and the instantaneous operating point is A. Similarly for v_{in} = −1 we have v_{GS} = 2 V and the instantaneous operating point is at B. We find $V_{DSQ} \cong 11$ V, $V_{DSmin} \cong 6$ V, $V_{DSmax} \cong 14$ V.

Exercise 5.4



The analysis is similar to Example 5.3 in the book.

$$K = \left(\frac{W}{L}\right)\frac{KP}{2} = 1 \text{ mA/V}^2$$

$$V_G = V_{DD} \frac{R_2}{R_1 + R_2} = 20 \frac{1}{(1.5 + 1)} = 8 \text{ V}$$

$$V_{GSQ}^2 + \left(\frac{1}{R_S K} - 2V_{to}\right)V_{GSQ} + (V_{to})^2 - \frac{V_G}{R_S K} = 0$$

After values are substituted, we have

$$V_{GSQ}^2 - 3.583V_{GSQ} + 0.6667 = 0$$

Solving we find $V_{GSQ} = 3.39$ V. (The second root is extraneous and should be discarded.) Then we have

$$I_{DQ} = K(V_{GSQ} - V_{to})^2 = 1.92 \text{ mA}$$

$$V_{DSQ} = V_{DD} - (R_D + R_S)I_{DQ} = 10.8 \text{ V}$$

Exercise 5.5

We should choose $R_D = 0$ for a source follower. Many values will work for the other resistors. A reasonable set of values is $R_S = 3.9$ kΩ , $R_1 = 1$ MΩ, and $R_2 = 2$ MΩ. These values yield $I_{DQ} =$ 1.98 mA and $V_{DSQ} = 7.26$ V. Use SPICE to check that your design provides a Q-point close to the desired value.

Exercise 5.6

From Figure 5.24 at an operating point defined by $V_{GSQ} = 2.5$ V and $V_{DSQ} = 6$ V, we have

$$g_m = \frac{\Delta i_D}{\Delta v_{GS}} = \frac{(4.4 - 1.1) \text{ mA}}{1 \text{ V}} = 3.3 \text{ mS}$$

$$1/r_d = \frac{\Delta i_D}{\Delta v_{DS}} \cong \frac{(2.9 - 2.3) \text{ mA}}{(14 - 2) \text{ V}} = 0.05 \times 10^{-3}$$

Taking the reciprocal, we find $r_d = 20$ kΩ

Exercise 5.7

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q\text{-point}}$$

$$= \left.\frac{\partial}{\partial v_{GS}} K(v_{GS} - V_{to})^2\right|_{Q\text{-point}}$$

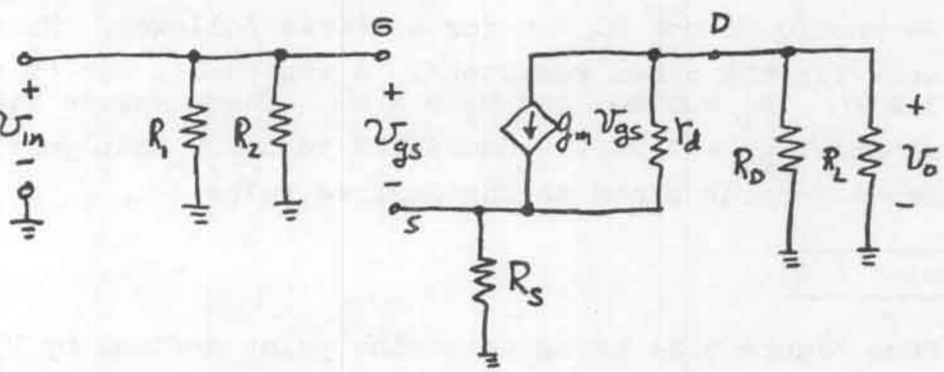
$$= 2K(V_{GSQ} - V_{to})$$

Exercise 5.8

$$R'_L = \frac{1}{1/r_d + 1/R_D + 1/R_L} = R_D = 4.7\ k\Omega$$

$$A_v = -g_m R'_L = -(1.77\ mS) \times (4.7\ k\Omega) = -8.32$$

Exercise 5.9



For simplicity we treat r_d as an open circuit. Let $R'_L = R_D || R_L$.

$$v_{in} = v_{gs} + R_s g_m v_{gs}$$

$$v_o = -R'_L g_m v_{gs}$$

$$A_v = \frac{v_o}{v_{in}} = \frac{-R'_L g_m}{1 + R'_L g_m}$$

Exercise 5.10

$$R_L' = R_D || R_L = 3.197 \text{ k}\Omega$$

$$A_v = \frac{v_o}{v_{in}} = \frac{-R_L' g_m}{1 + R_L' g_m} = \frac{-(3.197 \text{ k}\Omega)(1.77 \text{ mS})}{1 + (3.197 \text{ k}\Omega)(1.77 \text{ mS})} = -0.849$$

Exercise 5.11

The equivalent circuit is shown in Figure 5.35 in the book.

$$v_{in} = 0$$

$$v_{gs} = -v_x$$

$$i_x = \frac{v_x}{R_S} + \frac{v_x}{r_d} - g_m v_{gs} = \frac{v_x}{R_S} + \frac{v_x}{r_d} + g_m v_x$$

$$R_o = \frac{v_x}{i_x} = \frac{1}{g_m + \frac{1}{R_S} + \frac{1}{r_d}}$$

Exercise 5.12

Refer to the small-signal equivalent circuit shown in Figure 5.37 in the book. Let $R_L' = R_D || R_L$.

$$v_{in} = -v_{gs}$$

$$v_o = -R_L' g_m v_{gs}$$

$$A_v = v_o/v_{in} = R_L' g_m$$

$$i_{in} = v_{in}/R_s - g_m v_{gs} = v_{in}/R_s + g_m v_{in}$$

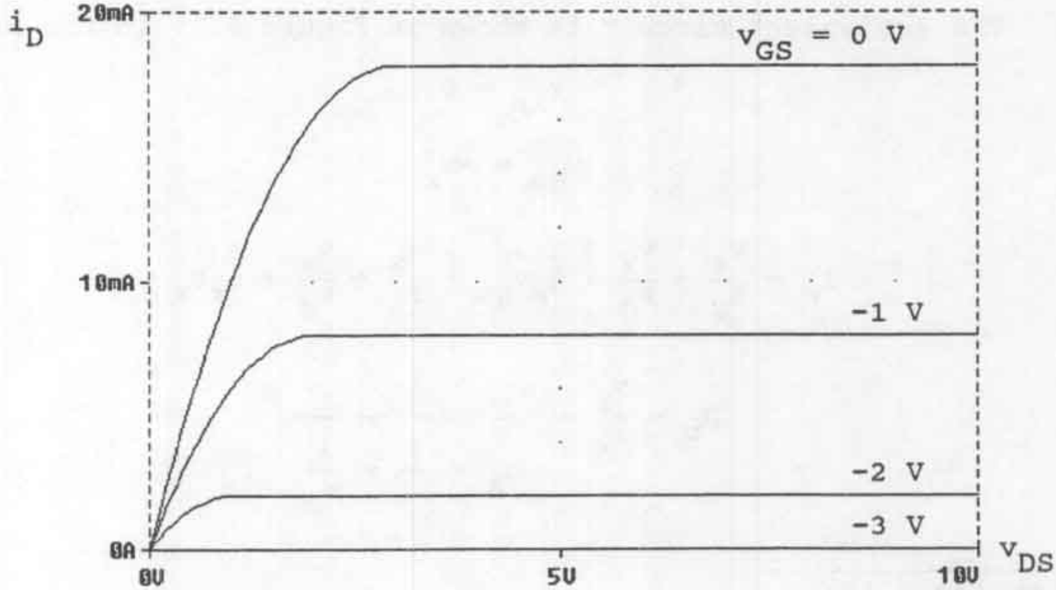
$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{g_m + 1/R_s}$$

If we set $v(t) = 0$, then we have $v_{gs} = 0$. Removing the load and looking back into the amplifier we see the resistance R_D. Thus we have

$$R_o = R_D$$

Exercise 5.13

The characteristics are:



Exercise 5.14

See Figure 5.45 in the book.

Exercise 5.15

(a) $v_{GS} = -5$ V and $v_{DS} = 5$ V: Because $v_{GS} < V_{to}$ the device is in cutoff.

b) $v_{GS} = -2$ V and $v_{DS} = 1$ V: Because $v_{GS} > V_{to}$ and $v_{GD} = v_{GS} - v_{DS} = -3 > V_{to}$ the device is operating in the linear (triode) region.

(c) $v_{GS} = -1$ V and $v_{DS} = 5$ V: Because $v_{GS} > V_{to}$ and $v_{GD} = v_{GS} - v_{DS} = -6 < V_{to}$ the device is operating in the saturation region.

(d) $v_{GS} = 0$ V and $v_{DS} = 2$ V: Because $v_{GS} > V_{to}$ and $v_{GD} = v_{GS} - v_{DS} = -2 > V_{to}$ the device is operating in the linear (triode) region.

Exercise 5.16

For $v_{GS} = -3$ V and $v_{DS} = 5$ V the device is operating in the saturation region for which we have

$$i_D = K(v_{GS} - V_{to})^2$$

$$K = \frac{i_D}{(v_{GS} - V_{to})^2} = \frac{1 \text{ mA}}{(-3 + 4)^2} = 1 \text{ mA/V}^2$$

$$I_{DSS} = KV_{to}^2 = (1 \text{ mA/V}^2) \times (-4 \text{ V})^2 = 16 \text{ mA}$$

Problem 5.1

See Figures 5.1 and 5.2 in the book.

Problem 5.2

Cutoff: $i_D = 0$ for $v_{GS} \le V_{to}$

Triode: $i_D = K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2]$
for $v_{DS} \le v_{GS} - V_{to}$ (or $v_{GD} \ge V_{to}$) and $v_{GS} \ge V_{to}$

Saturation: $i_D = K(v_{GS} - V_{to})^2$
for $v_{GS} \ge V_{to}$ and $v_{DS} \ge v_{GS} - V_{to}$ (or $v_{GD} \le V_{to}$)

Problem 5.3

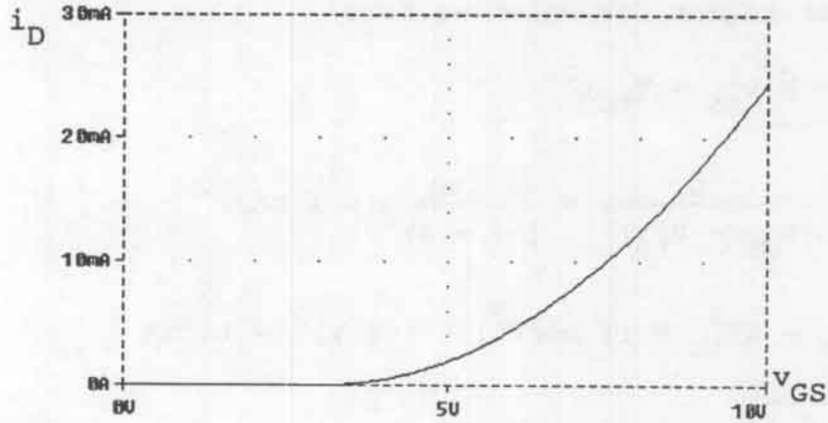
(a) Saturation because we have $v_{GS} \ge V_{to}$ and $v_{DS} \ge v_{GS} - V_{to}$.

(b) Triode because we have $v_{DS} < v_{GS} - V_{to}$ and $v_{GS} \geq V_{to}$.

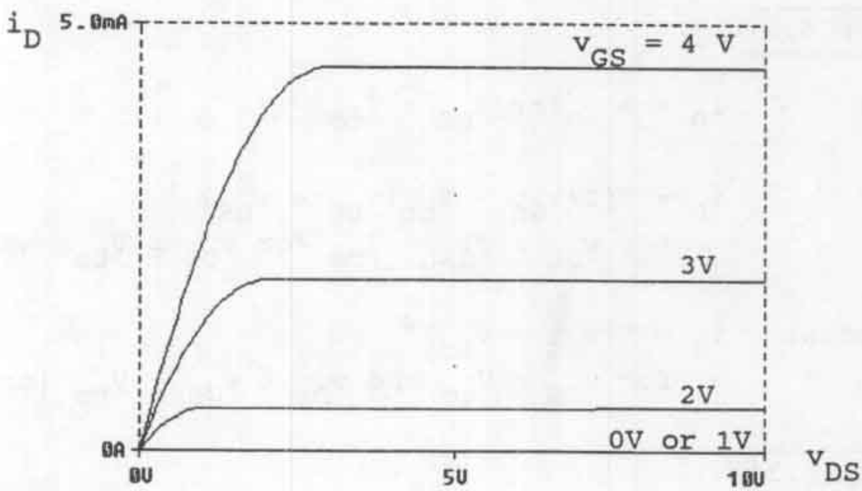
(c) Cutoff because we have $v_{GS} \leq V_{to}$.

Problem 5.4

The device is in saturation for $v_{DS} \geq v_{GS} - V_{to} = 2$ V. The device is in the triode region for $v_{DS} \leq 2$ V. The plot of i_D versus v_{GS} in the saturation region is:



Problem 5.5



Problem 5.6

(a) Cutoff because we have $v_{GS} \leq V_{to}$.

(b) Triode because we have $v_{DS} < v_{GS} - V_{to}$ and $v_{GS} \geq V_{to}$.

(c) Saturation because we have $v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$.

(d) Saturation because we have $v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$.

Problem 5.7

With $v_{GS} = v_{DS} = 5$ V the transistor operates in the saturation region for which we have $i_D = K(v_{GS} - V_{to})^2(1 + \lambda v_{DS})$. Solving for K and substituting values we obtain $K = 31.25\ \mu A/V^2$. However we have $K = (W/L)(KP/2)$. Solving for W/L and substituting values we obtain $W/L = 1.25$. Thus for $L = 2\ \mu m$, we need $W = 2.5\ \mu m$.

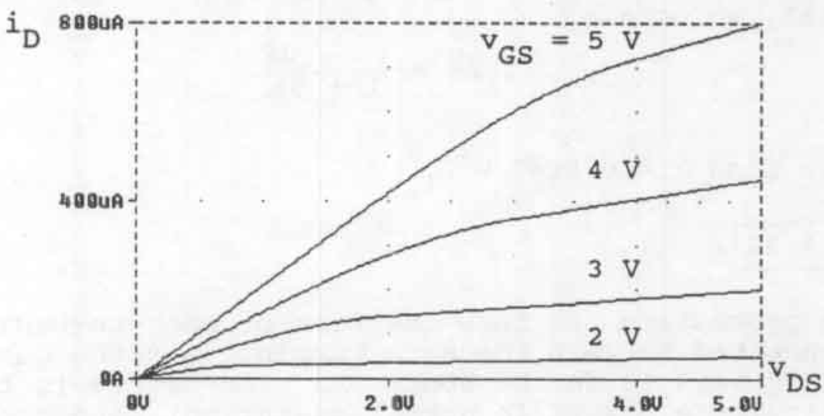
Repeating the calculations with $\lambda = 0.05$, we obtain $K = 25$, $W/L = 1$ and $W = 2\ \mu m$.

Problem 5.8

To obtain the least drain current choose minimum W and maximum L (i.e., $W_1 = 0.5\ \mu m$ and $L_1 = 2\ \mu m$). To obtain the greatest drain current choose maximum W and minimum L (i.e., $W_2 = 2\ \mu m$ and $L_2 = 0.5\ \mu m$). The ratio between the greatest and least drain current is $(W_2/L_2)/(W_1/L_1) = 16$.

Problem 5.9

For minimum chip area choose the minimum values of L and W which are $0.5\ \mu m$. Plots of the drain characteristics are:



Problem 5.10

In the saturation region, we have $i_D = K(v_{GS} - V_{to})^2$. Substituting values we obtain two equations:

$$0.5 \text{ mA} = K(2 - V_{to})^2$$

$$2 \text{ mA} = K(3 - V_{to})^2$$

Dividing each side of the second equation by the respective side of the first, we obtain

$$4 = \frac{(3 - V_{to})^2}{(2 - V_{to})^2}$$

Solving we determine that $V_{to} = 1$ V. Then using either of the two equations we find $K = 0.5 \text{ mA/V}^2$.

Problem 5.11

Both points given are in the saturation region, so we have $i_D = K(v_{GS} - V_{to})^2(1 + \lambda v_{DS})$. Substituting values we obtain two equations:

$$1 \text{ mA} = K(3 - 1)^2(1 + 5\lambda)$$

$$1.25 \text{ mA} = K(3 - 1)^2(1 + 10\lambda)$$

Dividing each side of the second equation by the respective side of the first, we obtain

$$1.25 = \frac{1 + 10\lambda}{1 + 5\lambda}$$

Solving we find $\lambda = 0.0667 \text{ V}^{-1}$.

Problem 5.12

Gate protection can take the form of back-to-back Zener diodes connected between the gate terminal and the substrate as shown in Figure 5.12 in the book. An alternative is two diodes (that are reverse biased in normal operation) connected from the gate to the power supply and from gate to ground. Gate protection is needed so static electric charge does not cause breakdown of the oxide layer in normal handling of the devices. Gate protection is not needed for devices that do not have external terminals.

Problem 5.13

For a device operating in the triode region with $\lambda = 0$, we have

$$i_D = K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2]$$

Assuming that $v_{DS} << v_{GS} - V_{to}$ this becomes

$$i_D \cong K2(v_{GS} - V_{to})v_{DS}$$

Then the resistance between drain and source is given by

$$r_d = v_{DS}/i_D = \frac{1}{K2(v_{GS} - V_{to})}$$

With the device in cutoff (i.e., $v_{GS} \le V_{to}$), the drain current is zero and r_d is infinite.

Evaluating we have:

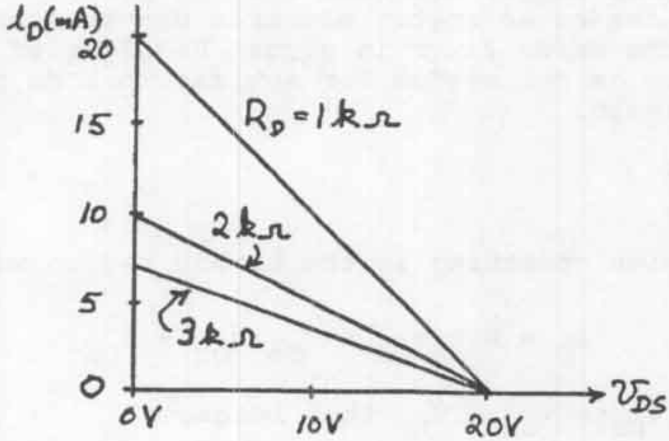
v_{GS} (V)	r_d (kΩ)
0.5	∞
1.0	∞
1.5	4
2.0	2

Problem 5.14

Distortion occurs in FET amplifiers because of curvature and nonuniform spacing of the characteristic curves.

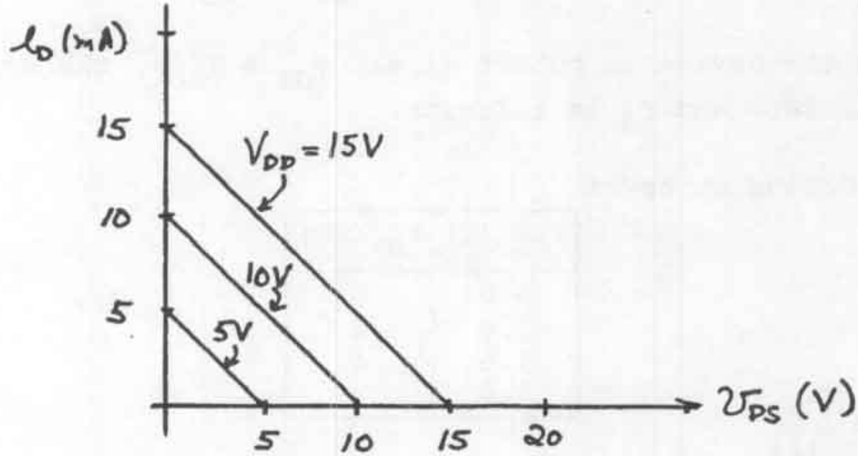
Problem 5.15

The load-line equation is $V_{DD} = R_D i_D + v_{DS}$, and the plots are shown on the next page.



Notice that the load line rotates around the point (V_{DD}, 0) as the resistance changes.

Problem 5.16



Notice that the load lines are parallel as long as R_D is constant.

Problem 5.17

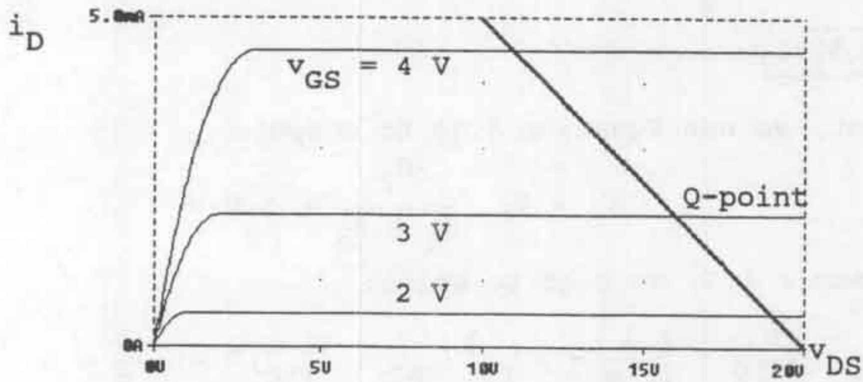
For $V_{GG} = 0$, the FET remains in cutoff so $V_{DSmax} = V_{DSQ} = V_{DSmin} = 20$ V. Thus the output signal is zero and the gain is zero. For amplification to take place, the FET must be biased in the saturation or triode regions.

Problem 5.18

(a) The 1.7 MΩ and 300 kΩ resistors act as a voltage divider that establishes a dc voltage $V_{GSQ} = 3$ V. Then if the capacitor is treated as a short for the signal frequency, we have

$$v_{GS}(t) = 3 + \sin(2000\pi t)$$

(b) (c) and (d)



From the load line we find $V_{DSQ} = 16$ V, $V_{DSmax} = 19$ V and $V_{DSmin} = 11$ V.

Problem 5.19

For $v_{in} = +1$ V we have $v_{GS} = 4$ V. For the FET to remain in saturation, we must have $V_{DSmin} \geq 3$ V at which point the drain current is 4.5 mA. Thus the maximum value of R_D is $R_{Dmax} = (20 - 3)/4.5 \text{ mA} = 3.778$ kΩ.

Problem 5.20

We are given

$$v_{DS}(t) = V_{DC} + V_{1m}\sin(2000\pi t) + V_{2m}\cos(4000\pi t)$$

Evaluating at t = 0.25 ms and observing that the plot gives v_{DS} = 4 V at that instant we have

$$4 = V_{DC} + V_{1m} - V_{2m}$$

Similarly at t = 0 we have

$$11 = V_{DC} + V_{2m}$$

and at t = 0.75 ms we have:

$$16 = V_{DC} - V_{1m} - V_{2m}$$

Solving the previous three equations we have $V_{DC} = 10.5$ V, $V_{2m} = 0.5$ V and $V_{1m} = -6$ V. Thus the percentage second-harmonic distortion is $|V_{2m}/V_{1m}| \times 100\% = 8.33\%$.

Problem 5.21

First, we use Equation 5.16 to compute

$$V_G = V_{DD} \frac{R_2}{R_1 + R_2} = 5 \text{ V}$$

As in Example 5.3, we need to solve:

$$V_{GSQ}^2 + \left(\frac{1}{R_S K} - 2V_{to}\right)V_{GSQ} + (V_{to})^2 - \frac{V_G}{R_S K} = 0$$

Substituting values, we have

$$V_{GSQ}^2 - 1.1489V_{GSQ} - 3.2553 = 0$$

The roots are $V_{GSQ} = 2.4679$ V and -1.319 V. The correct root is $V_{GSQ} = 2.4679$ V which yields $I_{DQ} = K(V_{GSQ} - V_{to})^2 = 0.5387$ mA. Finally we have $V_{DSQ} = V_{DD} - R_D I_{DQ} - R_S I_{DQ} = 9.936$ V.

Problem 5.22

For this circuit we can write

$$V_{GSQ} = 15 - I_{DQ}R_S$$

Assuming operation in saturation, we have

$$I_{DQ} = K(V_{GSQ} - V_{to})^2$$

using the first equation to substitute into the second equation we have

$$I_{DQ} = K(15 - I_{DQ}R_S - V_{to})^2 = 0.25(14 - 3I_{DQ})^2$$

where we have assumed that I_{DQ} is in mA. Rearranging we have

$$I_{DQ}^2 - 9.777I_{DQ} + 21.777 = 0$$

The correct root is the smaller one which is $I_{DQ} = 3.432$ mA. Then we have $V_{DSQ} = 30 - R_D I_{DQ} - R_S I_{DQ} = 16.27$ V.

Problem 5.23

Assuming that the MOSFET is in saturation, we have

$$V_{GSQ} = 10 - I_{DQ}$$
$$I_{DQ} = K(V_{GSQ} - V_{to})^2$$

where we have assumed that I_{DQ} and K are in mA and mA/V^2 respectively.

(a) Using the second equation to substitute in the first, substituting values and rearranging, we have

$$V_{GSQ}^2 - 7V_{GSQ} + 6 = 0$$

which yields

$$V_{GSQ} = 6 \text{ V}$$

(The other root, $V_{GSQ} = 1$ V, is extraneous.)

$$I_{DQ} = 4 \text{ mA}$$

$$V_{DSQ} = 10 - 2I_{DQ} = 12 \text{ V}$$

(b) Similarly we have

$$V_{GSQ}^2 - 3.5V_{GSQ} - 1 = 0$$

$$V_{GSQ} = 3.765 \text{ V}$$

$$I_{DQ} = 6.234 \text{ mA}$$
$$V_{DSQ} = 20 - 2I_{DQ} = 7.53$$

Problem 5.24

Many resistor values will work. In general we want to pick values such that

$$R_D I_{DQ} \cong V_{DD}/4$$

$$V_{DSQ} \cong V_{DD}/2$$

$$R_S I_{DQ} \cong V_{DD}/4$$

Thus we select $R_D = R_S = 3$ kΩ. Then we have K = (KP/2)(W/L) = 0.2 mA/V^2 and $V_{GSQ} = \sqrt{I_{DQ}/K} + V_{to} = 3.236$ V. Next we compute $V_G = V_{GSQ} + R_S I_{DQ} = 6.236 \text{ V} = V_{DD}/(1 + R_1/R_2)$. Solving we find that we need $R_1/R_2 = 0.924$. Using nominal 5% tolerance values we could select $R_1 = 910$ kΩ and $R_2 = 1$ MΩ.

We check the design with a simulation which is stored in the file named P5_24.

Problem 5.25

For a source follower we do not need a drain resistor. Thus we design for

$$V_{DSQ} = V_{DD}/2 = 6 \text{ V}$$
$$R_S I_{DSQ} = 6 \text{ V}$$

Thus we select $R_S = 6.2$ kΩ which is a standard 5% tolerance value. Then we have K = (KP/2)(W/L) = 0.2 mA/V^2 and $V_{GSQ} = \sqrt{I_{DQ}/K} + V_{to} = 3.236$ V. Next we compute $V_G = V_{GSQ} + R_S I_{DQ} = 9.236 \text{ V} = V_{DD}/(1 + R_1/R_2)$. Solving we find that we need $R_1/R_2 = 0.2996$. Using nominal 5% tolerance values we could select $R_1 = 300$ kΩ and $R_2 = 1$ MΩ.

We check the design with a simulation which is stored in the file named P5_25.

Problem 5.26

We have $V_G = V_{GSQ} = 10R_2/(R_1 + R_2) = 2.5$ V. Then we have $I_{DQ} = K(V_{GSQ} - V_{to})^2 = 0.5625$ mA. $V_{DSQ} = V_{DD} - R_D I_{DQ} = 4.375$ V.

Problem 5.27

We have $V_{GSQ} = V_{DSQ} = V_{DD} - R_D I_{DQ}$. Then substituting $I_{DQ} = K(V_{GSQ} - V_{to})^2$, we have

$$V_{GSQ} = V_{DD} - R_D K(V_{GSQ} - V_{to})^2$$

Substituting values and rearranging,we have

$$V_{GSQ}^2 + 2V_{GSQ} - 39 = 0$$

Solving we determine that $V_{GSQ} = 5.325$ V and then we have $I_{DQ} = K(V_{GSQ} - V_{to})^2 = 4.675$ mA.

Problem 5.28

See Figure 5.23 in the book.

Problem 5.29

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q\text{-point}} \qquad 1/r_d = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{Q\text{-point}}$$

Problem 5.30

For $\lambda = 0$ the drain characteristics are horizontal in the saturation region and $r_d = \infty$.

Problem 5.31

For $V_{DSQ} = 0$ the vertical spacing of the drain characteristics is zero. Therefore $g_m = 0$ at this operating point. Then the small-signal equivalent circuit consists only of r_d. FETs are used as electronically controllable resistances at this operating point.

Problem 5.32

In the triode region assuming $\lambda = 0$, we have

$$i_D = K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2]$$

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q\text{-point}} = 2Kv_{DS}\Big|_{Q\text{-point}} = 2KV_{DSQ}$$

Problem 5.33

In the triode region assuming $\lambda = 0$, we have

$$i_D = K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2]$$

$$1/r_d = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{Q\text{-point}} = 2K(v_{GS} - V_{to} - v_{DS})\Big|_{Q\text{-point}}$$

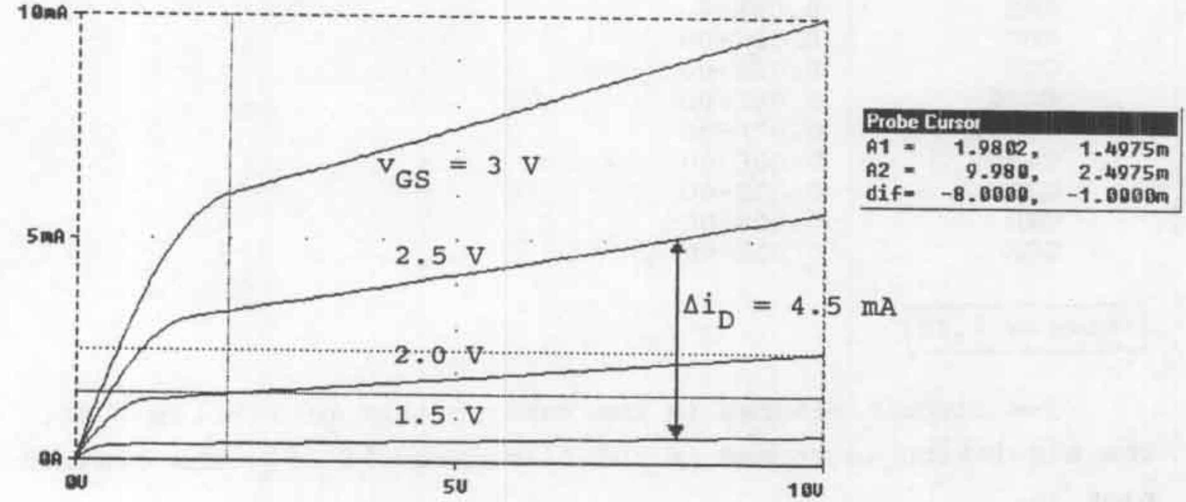
$$r_d = \frac{1}{2K(V_{GSQ} - V_{to} - V_{DSQ})}$$

Problem 5.34

(a) & (b) The simulation to obtain the plots is stored in file P5_34a. The curves are shown on the next page. We used the cursor in Probe to determine the coordinates at two points on the curve for $v_{GS} = 2$ V. Then we compute

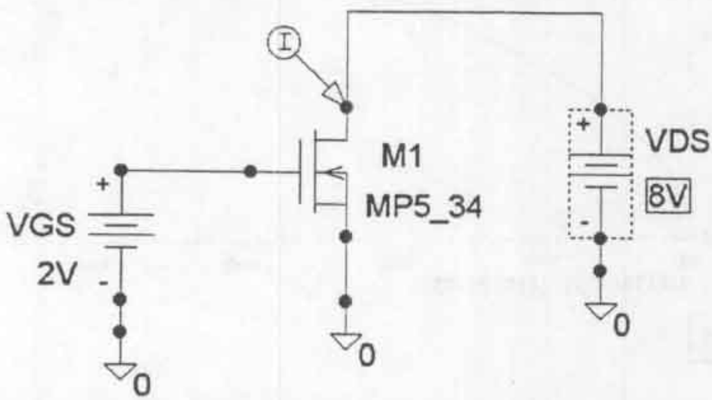
$$1/r_d = \frac{\Delta i_D}{\Delta v_{DS}} \cong \frac{(2.5 - 1.5)\ \text{mA}}{(10\ - 2)\ \ \text{V}} = 125 \times 10^{-6}$$

Then we have $r_d = 8\ k\Omega$.



Then we used the cursor to determine that $\Delta i_D = 4.5$ mA. Thus we have $g_m = \Delta i_D/\Delta v_{GS} = (4.5\text{ mA})/1\text{ V} = 4.5 \times 10^{-3}$ S.

(c) The circuit is:



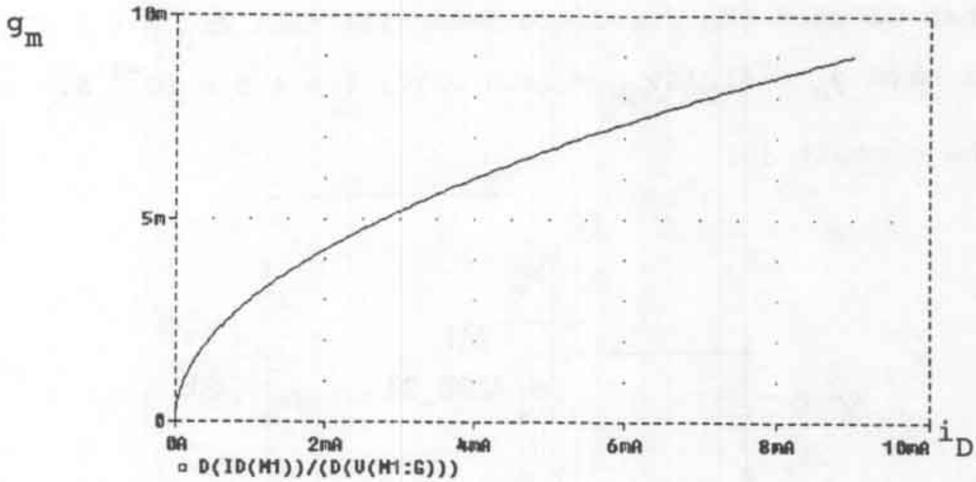
After simulating the circuit we scroll down the output file and find:

NAME	M_M1	
MODEL	MP5_34	
ID	2.25E-03	
VGS	2.00E+00	
VDS	8.00E+00	
VBS	0.00E+00	
VTH	1.00E+00	
VDSAT	1.00E+00	
GM	4.50E-03	This agrees with the g_m found above.

GDS	1.25E-04	(The inverse of GDS is r_d.)
GMB	0.00E+00	
CBD	0.00E+00	
CBS	0.00E+00	
CGSOV	0.00E+00	
CGDOV	0.00E+00	
CGBOV	0.00E+00	
CGS	0.00E+00	
CGD	0.00E+00	
CGB	0.00E+00	

Problem 5.35

The circuit diagram is the same as that of Problem 5.34. The simulation is stored in the file named P5_35. The desired plot is:



Problem 5.36

Coupling capacitors are used in discrete circuits to isolate the various stages for dc. Thus dc currents do not flow in the load. The dc component of the source does not affect the bias point of the input stage. Bias points of the various stages can be determined independently.

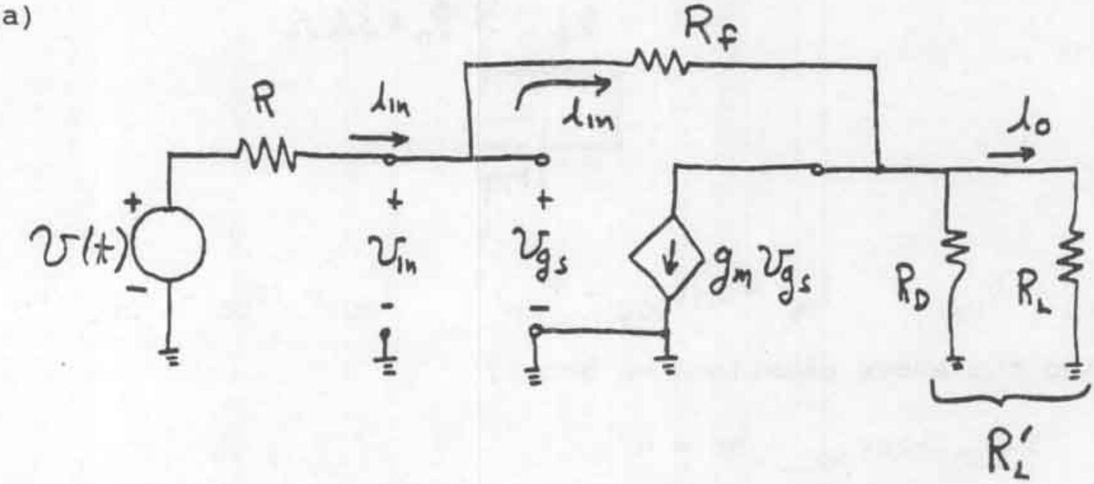
Coupling capacitors are replaced by short circuits in midband small-signal equivalent circuits. They cause the gain of an amplifier to decline as the signal frequency becomes small.

Problem 5.37

See Figure 5.25 in the book.

Problem 5.38

(a)

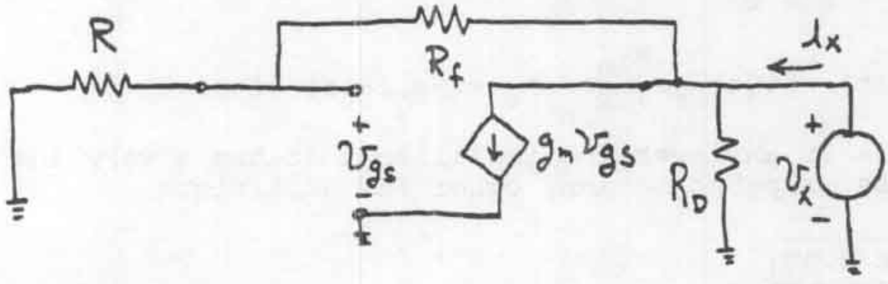


(b) $v_o = R_L'(i_{in} - g_m v_{in})$ $\qquad$ $i_{in} = (v_{in} - v_o)/R_f$

$$A_v = \frac{v_o}{v_{in}} = \frac{R_L' - g_m R_L' R_f}{R_L' + R_f}$$

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{R_f}{1 - A_v}$$

The circuit used to determine output impedance is:

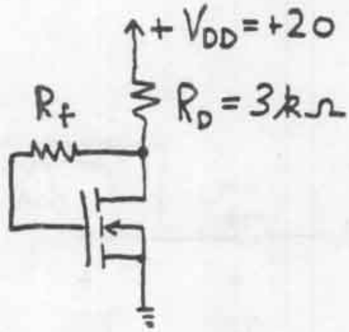


We define $R_D' = R_D || (R + R_f)$

$$v_{gs} = v_x \frac{R}{R + R_f} \qquad i_x = \frac{v_x}{R_D'} + g_m v_{gs}$$

$$R_o = \frac{v_x}{i_x} = \frac{1}{\frac{1}{R_D'} + \frac{g_m R}{R_f + R}}$$

(c) The dc circuit is:



$V_{GSQ} = V_{DSQ}$ $\quad I_{DQ} = K(V_{DSQ} - V_{to})^2$ $\quad I_{DQ} = (V_{DD} - V_{DSQ})/R_D$

Using the above equations we obtain

$$3V_{DSQ}^2 - 29V_{DSQ} + 55 = 0$$

$V_{DSQ} = 7.08$ V and $I_{DQ} = 4.31$ mA

$$g_m = g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q\text{-point}} = 2K(V_{GSQ} - V_{to}) = 4.16 \times 10^{-3} \text{ S}$$

(d) $R_L' = R_D || R_L = 2.31$ kΩ
$A_v = -9.37$
$R_{in} = 9.64$ kΩ
$R_o = 414$ Ω

(e) $v_o(t) = v(t) \frac{R_{in}}{R + R_{in}} A_v = -0.164\sin(2000\pi t)$

(f) This is an inverting amplifier that has a very low input impedance compared to many other FET amplifiers.

Problem 5.39

Referring to the circuit shown in Figure P5.39, we have

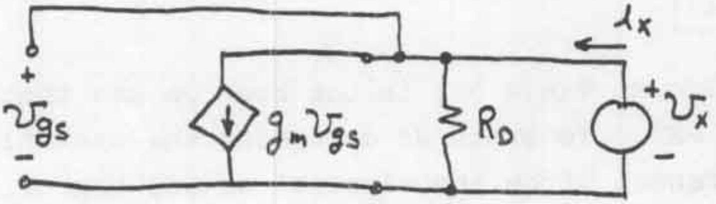
$V_{GSQ} = V_{DSQ}$ $\quad I_{DQ} = K(V_{GSQ} - V_{to})^2$ $\quad I_{DQ} = (V_{DD} - V_{DSQ})/R_D$

From the previous three equations we obtain:

$$1.1V_{DSQ}^2 - 5.6V_{DSQ} - 10.1 = 0$$

$$V_{DSQ} = 6.50 \text{ V and } I_{DQ} = 6.135 \text{ mA}$$

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q\text{-point}} = 2K(V_{GSQ} - V_{to}) = 3.5 \text{ mS}$$



$$R_o = \frac{v_x}{i_x} = \frac{v_x}{v_x/R_D + g_m v_x} = \frac{1}{1/R_D + g_m} = 253\ \Omega$$

Problem 5.40

Refer to Table 5.1 in the book for a compact summary of the characteristics of the various types of FETs. The device in this circuit is a depletion-mode NMOS transistor. The threshold voltage is negative. Otherwise the device equations and equivalent circuit are the same as those of depletion-mode NMOS devices.

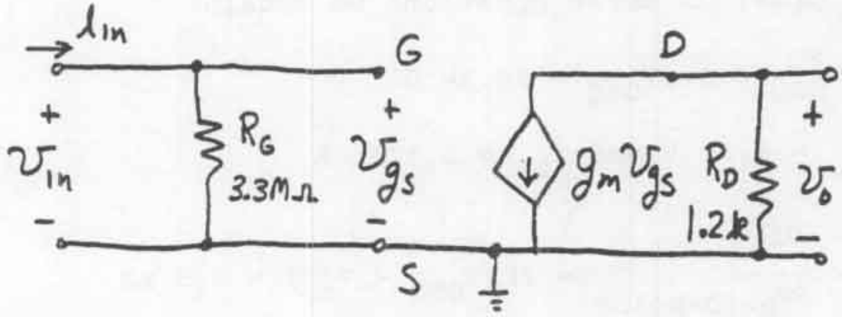
$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q\text{-point}} = 2K(V_{GSQ} - V_{to})$$

$$= 2 \times 10^{-3}[0 - (-3)] = 6 \text{ mS}$$

The small signal equivalent circuit is shown on the next page from which we obtain

$$R_{in} = R_G = 3.3 \text{ M}\Omega \qquad A_v = v_o/v_{in} = -g_m R_D = -7.2$$

$$R_o = R_D = 1.2 \text{ k}\Omega$$

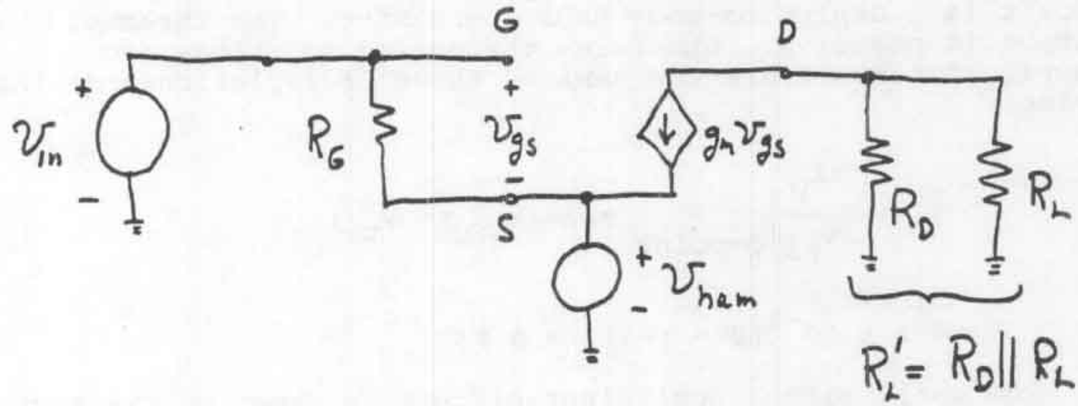


Problem 5.41

Referring to Table 5.1 in the book we see that the device is a p-channel FET. To start we determine the operating point and transconductance. From the circuit, we see that $V_{GSQ} = 0$. Therefore we have $I_{DQ} = I_{DSS} = 2$ mA and

$$g_m = \frac{2\sqrt{I_{DSS}I_{DQ}}}{|V_{to}|} = \frac{2\sqrt{(2\text{ mA}) \times (2\text{ mA})}}{3} = 1.33\text{ mA/V}^2$$

The circuit is a common-source amplifier. The small-signal equivalent circuit is:



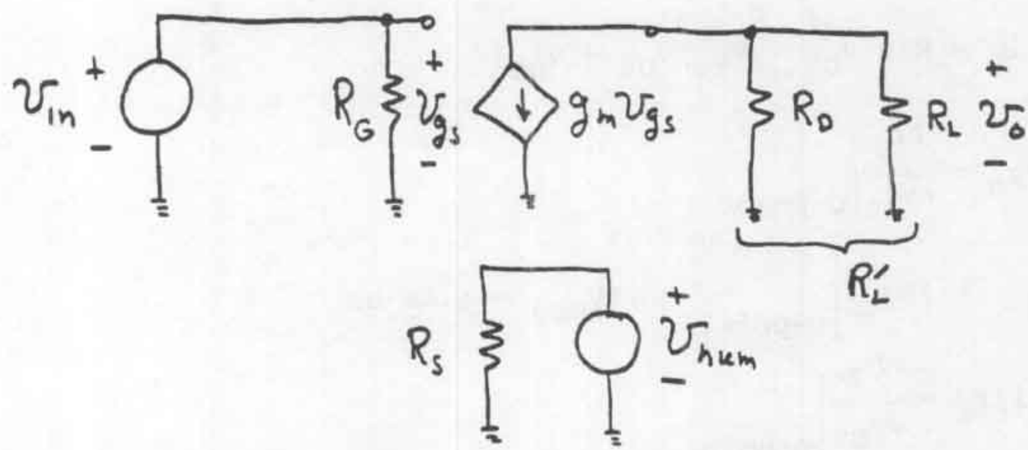
Assuming $v_{hum} = 0$, we have $v_{in} = v_{gs}$ and $v_o = -g_m v_{gs} R_L'$ from which we obtain $A_v = -g_m R_L'$. Evaluating we have $R_L' = 3.20$ kΩ and $A_v = -4.25$.

Problem 5.42

The equivalent circuit is shown in the solution of Problem 5.41. With $v_{in} = 0$, we have $v_{gs} = -v_{hum}$ and $v_o = -g_m R'_L v_{gs}$ from which we find $A_{hum} = v_o/v_{hum} = g_m R'_L = 4.25$. Thus for the circuit of Figure P5.41a we have $A_v = A_{hum}$. In other words the power-supply hum and the signal are amplified equally.

Problem 5.43

The bias current I_{DQ} and the transconductance are the same as those of Problems 5.41 and 5.42. The small-signal midband equivalent circuit is:



Notice that because C_3 shorts the source to ground, there is no connection between v_{hum} and the load. Thus we have $A_{hum} = 0$. For the signal the equivalent circuit is the same as in Problem 5.41 and we have $A_v = -4.25$. Notice that the signal is amplified but the hum is not. We conclude that the circuit of Figure 5.41b is better than that of Figure 5.41a.

Problem 5.44

Refer to Table 5.1 in the book for a compact summary of the characteristics of the various types of FETs. The device in this circuit is a depletion-mode NMOS transistor. The threshold voltage is negative. Otherwise the device equations and equivalent circuit are the same as those of depletion-mode NMOS devices.

(a) It turns out that the FET in this circuit is operating in the triode region. Thus we have

$$I_{DQ} = K[2(V_{GSQ} - V_{to})V_{DSQ} - V_{DSQ}^2]$$

and

$$I_{DQ} = (V_{DD} - V_{DSQ})/R_D$$

Equating the right-hand sides of these equations, substituting values and simplifying we obtain

$$V_{DSQ}^2 - 9V_{DSQ} + 16 = 0$$

which yields $V_{DSQ} = 2.44$ V. Notice that we have $V_{DSQ} \le V_{GSQ} - V_{to}$ so the assumption that the device operates in the triode region is correct. Also we have $I_{DQ} = 13.56$ mA.

(b) $i_D = K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2]$

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q\text{-point}}$$

$$= \left. 2Kv_{DS}\right|_{Q\text{-point}} = 2KV_{DSQ} = 4.88 \text{ mS}$$

$$1/r_d = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{Q\text{-point}}$$

$$= \left. 2K(v_{GS} - V_{to} - v_{DS})\right|_{Q\text{-point}}$$

$$r_d = \frac{1}{2K(V_{GSQ} - V_{to} - V_{DSQ})} = 321\ \Omega$$

(c) $R_i = R_G = 100$ kΩ

$R_L' = R_D || R_L || r_d = 195\ \Omega$

$A_v = -g_m R_L' = -0.954$

$R_o = R_D || r_d = 243\ \Omega$

Problem 5.45

See Figure 5.33 in the book.

Problem 5.46

If we need a voltage-gain magnitude greater than zero we choose a common-source amplifier. To attain lowest output impedance usually a source follower is better.

Problem 5.47

We have

$$K = \left(\frac{W}{L}\right)\frac{KP}{2} = 400\ \mu A/V^2$$

Assuming operation in saturation, we have

$$I_{DQ} = K(V_{GSQ} - V_{to})^2$$

Solving for V_{GSQ} and evaluating we have

$$V_{GSQ} = V_{to} + \sqrt{I_{DQ}/K} = 3.236\ V$$

$$V_G = V_{DD}\frac{R_2}{R_1 + R_2} = 10\ V$$

$$V_G = V_{GSQ} + R_S I_{DQ}$$

Solving for R_S and substituting values we have

$$R_S = (V_G - V_{GSQ})/I_{DQ} = 3.382\ k\Omega$$

We have $g_m = \sqrt{KI_{DQ}} = 0.8944$ mS

$$R_L' = \frac{1}{1/r_d + 1/R_S + 1/R_L} = 1.257\ k\Omega$$

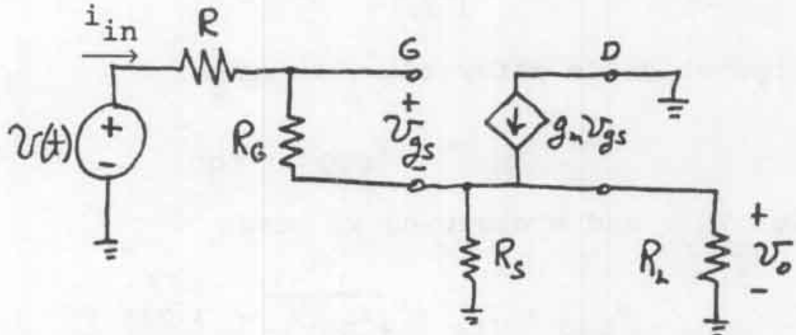
$$A_v = \frac{v_o}{v_{in}} = \frac{g_m R_L'}{1 + g_m R_L'} = 0.5293$$

$$R_{in} = \frac{v_{in}}{i_{in}} = R_G = R_1 || R_2 = 666.7 \text{ k}\Omega$$

$$R_o = \frac{1}{g_m + \frac{1}{R_S} + \frac{1}{r_d}} = 840.0 \ \Omega$$

Problem 5.48

(a)



(b) Let $R_L' = R_S || R_L$

$$v_o = R_L'(i_{in} + g_m v_{gs}) \qquad (1)$$

$$v_{in} = v_{gs} + v_o \qquad (2)$$

$$v_{gs} = i_{in} R_G \qquad (3)$$

Equations (1), (2) and (3) form the set from which we determine the voltage gain. First we use Equation (3) to substitute into Equation (1).

$$v_o = R_L'(i_{in} + g_m i_{in} R_G) \qquad (4)$$

Next we use Equations (3) and (4) to substitute into Equation (2).

$$v_{in} = R_G i_{in} + R_L'(i_{in} + g_m i_{in} R_G) \qquad (5)$$

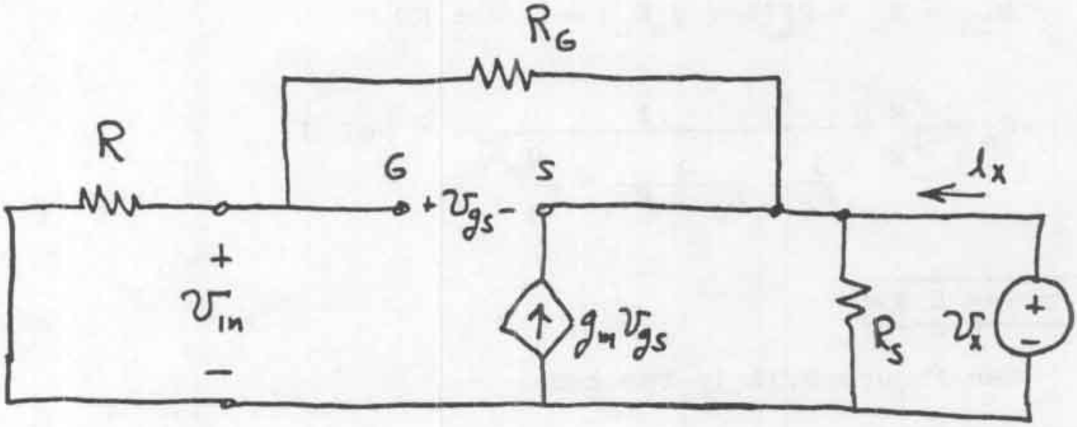
Finally we divide the respective sides of Equations (4) and (5) to obtain

$$A_v = \frac{v_o}{v_{in}} = \frac{R'_L(1 + g_m R_G)}{R_G + R'_L(1 + g_m R_G)}$$

Next we obtain the input resistance from Equation (5).

$$R_{in} = R_G + R'_L(1 + g_m R_G)$$

The equivalent circuit for the analysis of R_o is:



$$v_{in} = v_x R/(R + R_G) \tag{6}$$

$$v_{gs} = v_{in} - v_x \tag{7}$$

$$i_x = v_x/R_S + v_x/(R_G + R) - g_m v_{gs} \tag{8}$$

Now we use Equation (6) to substitute into Equation (7) and the result to substitute into Equation (8).

$$i_x = v_x\left[\frac{1}{R_S} + \frac{1}{R_G + R} + \frac{g_m R_G}{R_G + R}\right]$$

Finally we have

$$R_o = \frac{v_x}{i_x} = \frac{1}{\dfrac{1}{R_S} + \dfrac{1}{R_G + R} + \dfrac{g_m R_G}{R_G + R}}$$

(c) In this circuit we have $V_{GSQ} = 0$. Therefore $I_{DQ} = K(V_{to})^2 = 0.8$ mA. Then we have $g_m = 2\sqrt{KI_{DQ}} = 0.8$ mS.

(d) $R'_L = R_S || R_L = 909.1\ \Omega$

$$A_v = \frac{v_o}{v_{in}} = \frac{R'_L(1 + g_m R_G)}{R_G + R'_L(1 + g_m R_G)} = 0.4213$$

$$R_{in} = R_G + R'_L(1 + g_m R_G) = 3.455\ \text{M}\Omega$$

$$R_o = \frac{v_x}{i_x} = \frac{1}{\dfrac{1}{R_S} + \dfrac{1}{R_G + R} + \dfrac{g_m R_G}{R_G + R}} = 567\ \Omega$$

Problem 5.49

See Figure 5.38 in the book.

Problem 5.50

In normal operation, the junction between the gate and channel of a JFET is reverse biased.

Problem 5.51

The pinch-off voltage V_{to} of a JFET is the value of gate-to-channel bias required for the depletion region to extend completely across the channel. Typically, it is a few volts in magnitude and is negative for *n*-channel devices. I_{DSS} is the drain current in saturation for $v_{GS} = 0$.

Problem 5.52

$$i_D = K(v_{GS} - V_{to})^2(1 + \lambda v_{DS})$$

Problem 5.53

See Figure 5.43 in the book.

Problem 5.54

Cutoff: $v_{GS} \le V_{to}$

Triode: $v_{GS} \ge V_{to}$ $\quad v_{GS} - v_{DS} = v_{GD} \ge V_{to}$

Saturation: $v_{GS} \ge V_{to}$ $\quad v_{GS} - v_{DS} = v_{GD} \le V_{to}$

Problem 5.55

See Figure 5.46 in the book for the n-channel depletion MOSFET.

The p-channel enhancement device is similar in construction to Figure 5.1 except that n and p regions are interchanged. The symbol is shown in Figure 5.2 except that the arrow points in the opposite direction.

Problem 5.56

Refer to Table 5.1. We have $K = I_{DSS}/V_{to}^2 = 1$ mA/V^2. Then we have

$$i_D = K(v_{GS} - V_{to})^2$$

$$4 \times 10^{-3} = 10^{-3}(v_{GS} + 3)^2$$

Solving we find $v_{GS} = -1$ and $v_{GS} = -5$. However $v_{GS} = -5$ corresponds to operation in the cutoff region so the correct answer is $v_{GS} = -1$ V.

Problem 5.57

For operation in saturation we must have $v_{DS} \ge v_{GS} - V_{to}$. Thus for $v_{GS} = -1$ V we must have $v_{DS} \ge -1 - (-3) = 2$ V. For $v_{GS} = -2$ V, saturation requires $v_{DS} \ge 1$ V.

Problem 5.58

(a) We have $v_{GS} > V_{to}$ and $v_{DS} < v_{GS} - V_{to}$. Thus the device is operating in the triode region, and we have

$$i_D = K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2]$$

$$= 10^{-3}[2(-1 + 3)1 - 1^2]$$

$$= 3 \text{ mA}$$

(b) We have $v_{GS} > V_{to}$ and $v_{DS} > v_{GS} - V_{to}$. Thus the device is operating in the saturation region, and we have

$$i_D = K(v_{GS} - V_{to})^2$$

$$= 10^{-3}(-1 + 3)^2$$

$$= 4 \text{ mA}$$

Problem 5.59

The FET is in cutoff for $v_{GS} \le V_{to} = -3$ V.

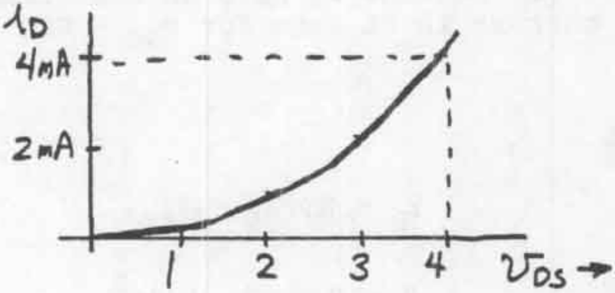
Problem 5.60

Because $v_{GS} = 0$, we have $i_D = I_{DSS}$ provided that $v_{DS} > -V_{to}$. When the meter reading becomes constant the device has reached saturation. Thus we conclude that $I_{DSS} = 13$ mA and $V_{to} = -3$ V.

Problem 5.61

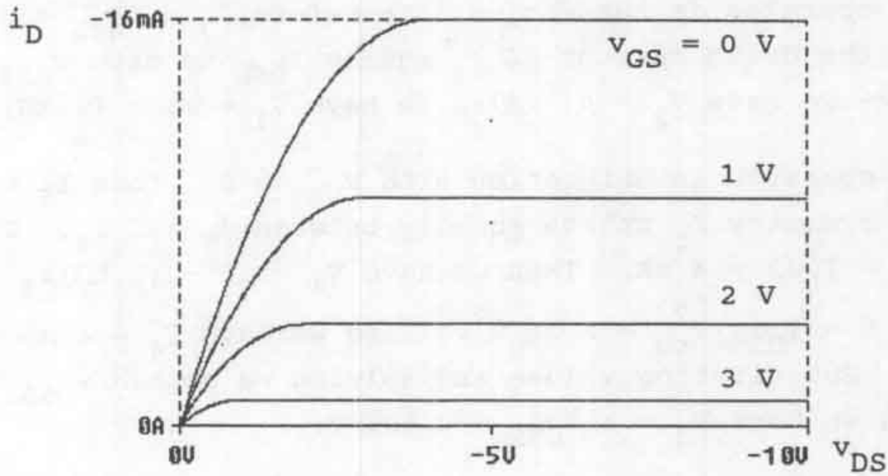
$$I_{DSS} = KV_{to}^2 = 0.25 \times (-4)^2 = 4 \text{ mA}$$

The boundary between the triode and saturation regions is given by Equation 5.55 which is $i_D = Kv_{DS}^2$.



Problem 5.62

First we compute $K = I_{DSS}/V_{to}^2 = 10^{-3}\ A/V^2$. The PSpice model name for K is BETA. Also in the PSpice model the threshold voltage must be given as -4 V. The simulation is stored in the file named P5_62. The plots are shown below. PSpice references all currents into device terminals. Because current flows out of the drain of a p-channel FET the current values reported by PSpice are negative.



Problem 5.63

Because the meter has very high impedance we have $i_D \cong 0$ in both circuits. Also drain current will flow unless v_{GS} is less than V_{to}. In circuit (a) because we have a JFET, we expect that V_{to} is a few volts negative. Thus the voltage across the meter equals $-V_{to}$.

In circuit (b) because we have an enhancement mode MOSFET, we expect the current to be zero for $v_{GS} = 0$. Thus the meter reads zero.

Problem 5.64

$$i_D = K(v_{GS} - V_{to})^2$$

$$3 = 0.5(v_{GS} + 2)^2$$

Solving we find $v_{GS} = -4.449$ V. ($v_{GS} = 0.449$ is extraneous.)

Problem 5.65

(a) $v_{GS} = 0$, therefore $I_1 = I_{DSS} = 8$ mA.

(b) $v_{GS} = 0$, therefore $I_2 = I_{DSS} = 8$ mA.

(c) J_4 operates in saturation. Therefore $I_3 = I_{DSS} = 8$ mA. Because the drain current of J_3 equals I_{DSS} we have $v_{GS3} = 0$. Therefore we have $V_2 = 0$. Also we have $V_1 = 15 - (1\ k\Omega)I_3 = 7$ V.

(d) J_7 operates in saturation with $v_{GS7} = 0$. Thus $I_5 = I_{DSS} = 8$ mA. By symmetry I_5 splits equally between J_5 and J_6. Thus we have $I_4 = I_5/2 = 4$ mA. Then we have $V_4 = 15 - (1\ k\Omega)I_5 = 7$ V. We have $K = I_{DSS}/V_{to}^2 = 2\ mA/V^2$. Also we have $I_4 = 4\ mA = K(v_{GS5} - V_{to})$. Substituting values and solving we obtain $v_{GS5} = -0.586$ V. Then we have $V_5 = -v_{GS5} = 0.586$ V.

Problem 5.66

(a) $v_{GS} = 0$ $\quad i_D = I_{DSS} = 8$ mA $\quad v_{DS} = 15 - (1\ k\Omega)i_D = 7$ V

(b) We have $v_{GS} = 0$ and $K = I_{DSS}/V_{to}^2$. It turns out that the FET is operating in the triode region, and we have

$$i_D = K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2] = K(8v_{DS} - v_{DS}^2)$$

$$v_{DS} = 15 - R_D i_D$$

Substituting and rearranging we obtain

$$1.5v_{DS}^2 - 13v_{DS} + 15 = 0$$

Solving we find $v_{DS} = 1.37$ V. (The other root $v_{DS} = 7.3$ is extraneous.) Then we compute $i_D = 4.54$ mA.

(c) $v_{GS} = -i_D$ (Assuming i_D is in mA.)

$i_D = K(v_{GS} - V_{to})^2$ (Assuming operation in saturation.)

Substituting we obtain

$$-v_{GS} = 0.5(v_{GS} + 4)^2$$

which yields $v_{GS} = -2$ V. Then we can compute $i_D = K(v_{GS} - V_{to})^2 = 2$ mA and $v_{DS} = 15 - (2.7\ \text{k}\Omega + 1\ \text{k}\Omega)i_D = 7.6$ V.

(d) $V_G = 20 \times \dfrac{400\ \text{k}\Omega}{(400\ \text{k}\Omega) + (1.6\ \text{M}\Omega)} = 4$ V

$v_{GS} = V_G - 3i_D$ (Assuming i_D is in mA.)

$i_D = K(v_{GS} - V_{to})^2$ (Assuming operation in saturation.)

Substituting we have

$$v_{GS} = V_G - 3K(v_{GS} - V_{to})^2 = 4 - 1.5(v_{GS} + 4)^2$$

Solving we find $v_{GS} = -2$ V. Then we have $i_D = 2$ mA and $v_{DS} = 8$ V.

Problem 5.67

$$K = I_{DSS}/V_{to}^2 = 2\ \text{mA/V}^2.$$

$$I_{DQ} = K(V_{GSQ} - V_{to})^2$$

$$4 = 2(V_{GSQ} + 3)^2 \quad \Rightarrow \quad V_{GSQ} = -1.59 \text{ V}$$

$$V_{GSQ} = -R_S I_{DQ} \quad \Rightarrow \quad R_S = 398\ \Omega$$

The FET is in saturation if $V_{GSQ} - V_{DSQ} < V_{to}$ which implies $V_{DSQ} > 1.41$ V. We have $V_{DSQ} = 20 - (R_S + R_D)I_{DQ}$. Finally we find that the maximum value allowed for R_D is 4.25 kΩ.

Problem 5.68

First we have $K = I_{DSS}/V_{to}^2 = 1$ mA/V^2. Then from $I_{DQ} = 9$ mA $= K(V_{GSQ} - V_{to})^2$ we determine that $V_{GSQ} = 1$ V. Then we have

$$V_{GSQ} = 20\frac{R_2}{R_2 + R_1} - R_S I_{DQ}$$

Substituting values and solving, we determine that $R_2 = 1$ MΩ.

For operation in saturation we require $V_{DSQ} > V_{GSQ} - V_{to} = 3$ V. Thus we need $20 - (R_D + R_S)I_{DQ} > 3$, which yields $R_D < 889\ \Omega$.

Problem 5.69

From $I_{DQ} = 9$ mA $= K(V_{GSQ} - V_{to})^2$ we determine that $V_{GSQ} = 7$ V. Then we have

$$V_{GSQ} = 20\frac{R_2}{R_2 + R_1} - R_S I_{DQ}$$

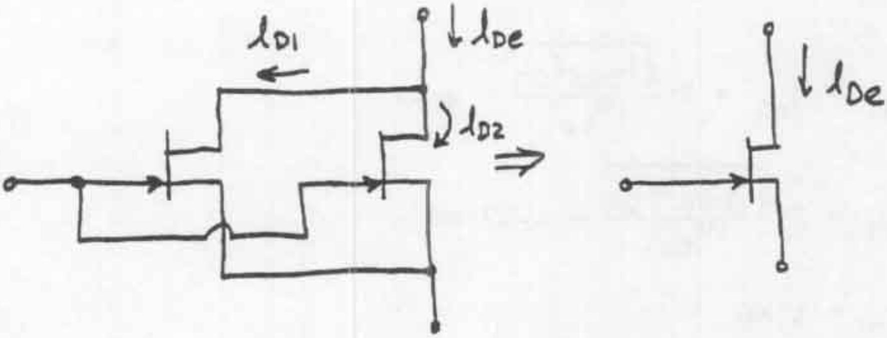
Substituting values and solving we determine that $R_2 = 4$ MΩ.

For operation in saturation we require $V_{DSQ} > V_{GSQ} - V_{to} = 3$ V. Thus we need

$$20 - (R_D + R_S)I_{DQ} > 3$$

which yields $R_D < 889\ \Omega$.

Problem 5.70



For equivalence

$$i_{D1} + i_{D2} = 2\frac{I_{DSS}}{V_{to}^2}(v_{GS} - V_{to})^2 = \frac{I_{DSSe}}{V_{toe}^2}(v_{GS} - V_{toe})^2$$

Thus we have $I_{DSSe} = 2I_{DSS}$ and $V_{toe} = V_{to}$. Furthermore

$$g_{me} = \left.\frac{\partial i_{De}}{\partial v_{GS}}\right|_{Q\text{-point}} = \left.\frac{\partial (2i_{D1})}{\partial v_{GS}}\right|_{Q\text{-point}} = 2g_m$$

Problem 5.71

(a) J_1 is a common-source amplifier.
J_2 is a common-source amplifier.
J_3 is a source follower.

(b) J_1 and J_2 have $V_{GSQ} = 0$. Therefore $I_{DQ1} = I_{DQ2} = I_{DSS} = 3$ mA.

The voltage at the gate of J_3 is $20 - (3\text{ k}\Omega)I_{DQ2} = 11$ V. Thus we have

$$11 = V_{GSQ3} + (10\text{ k}\Omega)I_{DQ3}$$

and

$$I_{DQ3} = K(V_{GSQ3} - V_{to})^2 \qquad \text{in which } K = \frac{I_{DSS}}{V_{to}^2} = 0.333\text{ mA/V}^2$$

Substituting and solving we find $I_{DQ3} = 1.21$ mA. Next we compute the transconductances of the FETs.

$$g_{m1} = g_{m2} = 2\frac{\sqrt{I_{DSS}I_{DQ}}}{|V_{to}|} = 2 \text{ mS}$$

$$g_{m3} = 2\frac{\sqrt{I_{DSS}I_{DQ3}}}{|V_{to}|} = 1.27 \text{ mS}$$

(c) $R_{in} = 1$ MΩ

$$A_{v1} = -g_{m1}R'_{L1} = -g_{m1}[(3\text{ k}\Omega)||(1\text{ M}\Omega)] = -5.98$$

$$A_{v2} = -g_{m2}R'_{L2} = -g_{m2}(3\text{ k}\Omega) = -6.00$$

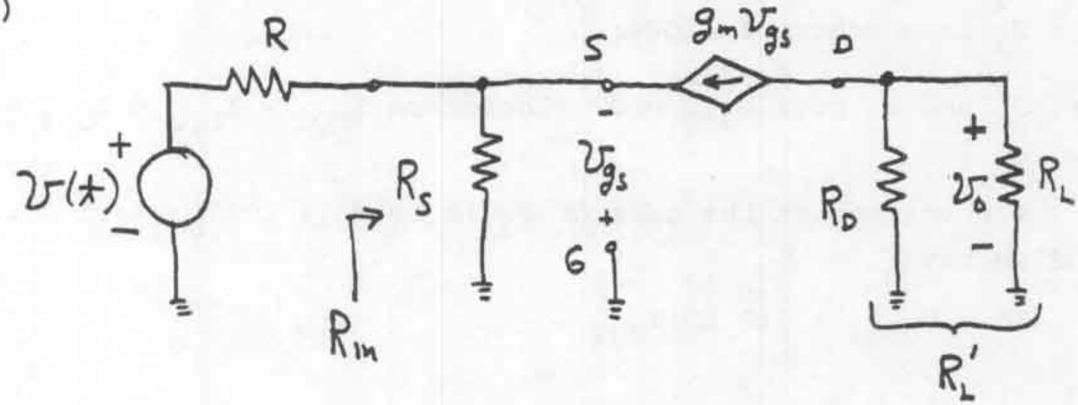
$$A_{v3} = \frac{g_{m3}(10\text{ k}\Omega)}{1 + g_{m3}(10\text{ k}\Omega)} = 0.927$$

$$A_v = A_{v1}A_{v2}A_{v3} = 33.3$$

$$R_o = \frac{1}{1/R_{S3} + g_{m3}} = 730\ \Omega$$

Problem 5.72

(a)



(b) $R_{in} = \dfrac{1}{g_m + 1/R_S}$

$A_v = g_m R_L'$ where $R_L' = R_D || R_L$

$R_o = R_D$

(c) $V_{GSQ} = -R_S I_{DQ}$ $\quad I_{DQ} = K(V_{GSQ} - V_{to})^2$

Solving we eventually find $I_{DQ} = 1.22$ mA and

$$g_m = \frac{2\sqrt{I_{DSS} I_{DQ}}}{|V_{to}|} = 3.11 \text{ mS}$$

(d) $R_{in} = \dfrac{1}{g_m + 1/R_S} = 243\ \Omega$ $\quad R_L' = R_D || R_L = 4.05\ \text{k}\Omega$

$A_v = g_m R_L' = 12.6$ $\quad R_o = R_D = 6.8\ \text{k}\Omega$

(e) $v_o(t) = v(t) \dfrac{R_{in}}{R + R_{in}} A_v = 0.893\sin(2000\pi t)$

(f) This is a noninverting amplifier. Its input resistance is very low compared to that of a common-source amplifier.

Problem 5.73

$$K = \frac{I_{DSS}}{V_{to}^2} = 2 \text{ mA/V}^2$$

With $V_{DSQ} = 0$ the device is in the triode or cutoff region. In the triode region we have

$$1/r_d = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{Q\text{-point}}$$

$$= \left.\frac{\partial}{\partial v_{DS}} K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2]\right|_{Q\text{-point}}$$

$$r_d = \left.\frac{1}{2K(V_{GSQ} - V_{to} - V_{DSQ})}\right|_{Q\text{-point}} = \frac{1}{2K(V_{GSQ} - V_{to})}$$

V_{GSQ} (V)	r_d (Ω)
-3	∞ (cutoff)
-2	∞ (cutoff)
-1	250
0	125
+1	83.3

Problem 5.74

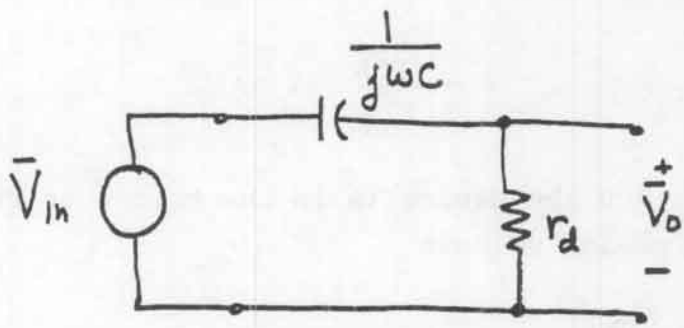
$$K = \frac{I_{DSS}}{V_{to}^2} = 1 \text{ mA/V}^2$$

With $V_{DSQ} = 0$, the FET operates either in cutoff or in saturation. The small signal parameters are $g_m = 0$ and

$$r_d = \frac{1}{2K(V_{GSQ} - V_{to})}$$

(See the solution to Problem 5.73.)

(a)



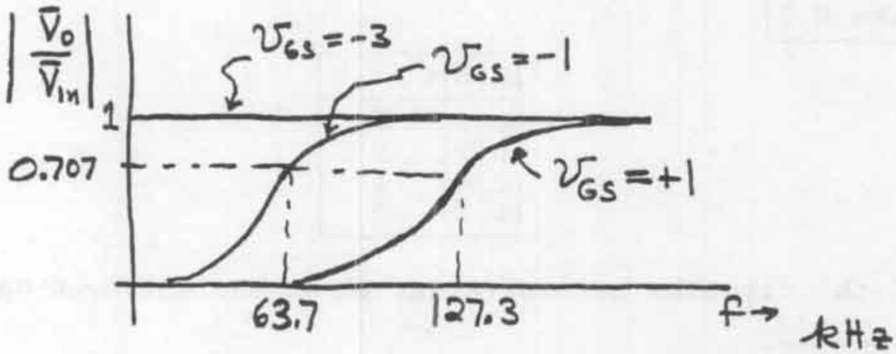
(b) $$\frac{V_o}{V_{in}} = \frac{r_d}{r_d + 1/(j\omega C)} = \frac{1}{1 - j(f_B/f)}$$

where $f_B = 1/(2\pi r_d C)$ is the half-power frequency.

(c)

v_{GS} (V)	r_d (Ω)	f_B (kHz)
−3	∞	0
−1	250	63.7
+1	125	127

(d) This is a high-pass filter.



(e) The PSpice simulation is stored in the file named P5_74.

Chapter 6

Exercise 6.1

See Figure 6.6 in the book.

Exercise 6.2

A	B	C or D
0	0	0
0	1	1
1	0	1
1	1	0

Each of the circuits is equivalent to an exclusive-OR gate.

Exercise 6.3

$NM_H = V_{OH} - V_{IH} = 4.5 - 4 = 0.5$ V

$NM_L = V_{IL} - V_{OL} = 2 - 1 = 1$ V

Exercise 6.4

Refer to the circuits shown in Figure 6.17 in the book.

(a) If either A or B (or both) is high the corresponding switch is closed and the output is low. If both A and B are low both switches are open and the output is high. Thus we have $C = \overline{A + B}$. In other words this is a NOR gate.

(b) If any of the inputs are low, the corresponding switch(es) is open and the output is high. If all of the inputs are high all of the switches are closed and the output is low. Thus we have $D = \overline{ABC}$. In other words this is a NAND gate.

(c) If either (or both) of the inputs are low, the corresponding switch(es) is open and the output is low. If both of the inputs are high, both of the switches are closed and the output is high. Thus we have C = AB. In other words this is an AND gate.

(d) If either A or B (or both) is high the corresponding switch is closed and the output is high. If both A and B are low, both switches are open and the output is low. Thus we have $C = A + B$. In other words this is an OR gate.

Exercise 6.5

$$P_{dynamic} = fC_L(V_{SS})^2 = (100 \times 10^6)(2 \times 10^{-12})5^2 = 5 \text{ mW}$$

Exercise 6.6

$$C_L = \frac{P_{dynamic}}{f(V_{SS})^2} = \frac{10/(50 \times 10^3)}{200 \times 10^6 \times 5^2} = 40 \times 10^{-15} \text{ F}$$

Exercise 6.7

As in Example 6.1 we have

$$P_{static} = 0.25 \times 10^{-3} = I_{DD}V_{DD}$$

$$I_{DD} = \frac{P_{static}}{V_{DD}} = 50 \ \mu A$$

$$i_D = \frac{V_{DD}}{R_{on} + R_D}$$

$$R_{on} + R_D = \frac{V_{DD}}{i_D} = \frac{5 \text{ V}}{50 \ \mu A} = 100 \text{ k}\Omega$$

$$R_{on} = \frac{V_{OL}}{V_{DD}}(R_D + R_{on}) = \frac{0.25}{5.0} \times 100 \text{ k}\Omega = 5 \text{ k}\Omega$$

$$R_D = 95 \text{ k}\Omega$$

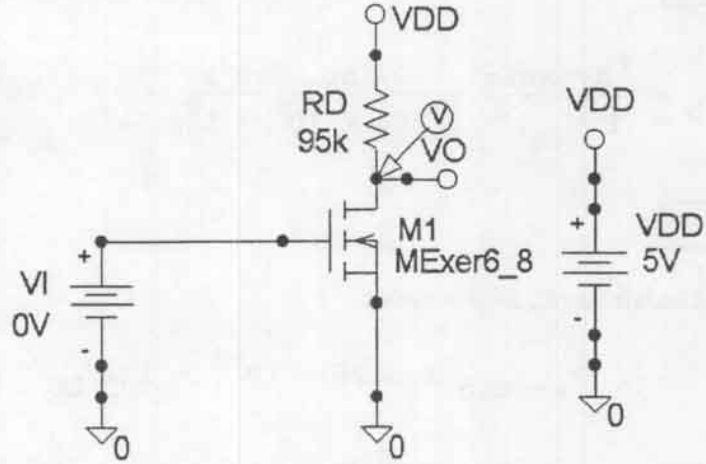
$$K = \frac{1}{2R_{on}(v_I - V_{to})} = \frac{1}{10^4 \ (5 - 1)} = 25 \ \mu A/V^2$$

$$\left(\frac{W}{L}\right) = \frac{2K}{KP} = \frac{2(25 \times 10^{-6})}{50 \times 10^{-6}} = \frac{1}{1}$$

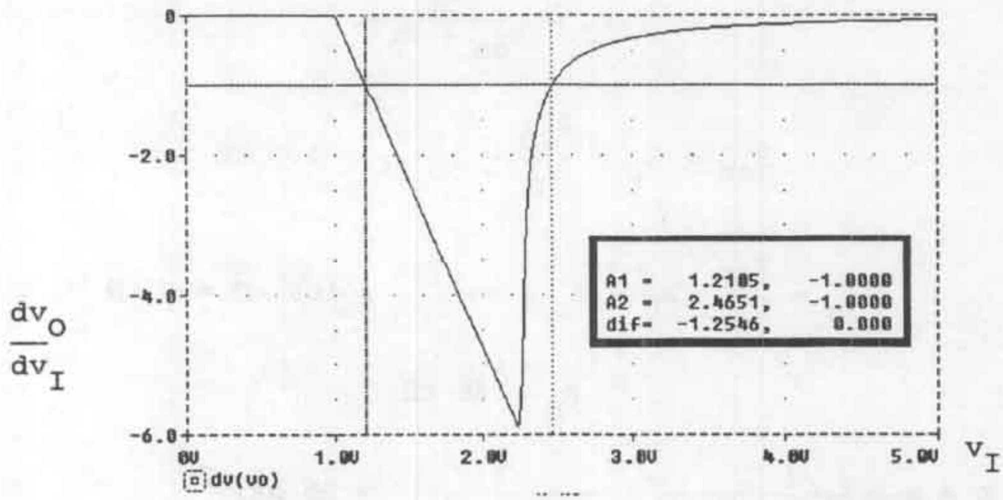
Exercise 6.8

The circuit is shown below:

W = L = 1 μm
V_{to} = 1 V
KP = 50 μA/V^2
λ = 0



The simulation is stored in the file named Exer6_8. After running the simulation we request a plot of the derivative of the output voltage with respect to the input voltage as shown:



Then we used the cursor to determine the input voltages for which the slope is -1, which yields V_{IH} = 2.47 V and V_{IL} = 1.21 V. Next we plotted V_O versus V_I and used the cursor to determine

$V_{OH} = 5.0$ V and $V_{OL} = 0.259$ V. Finally we compute the noise margins.

$$NM_H = V_{OH} - V_{IH} = 5.0 - 2.47 = 2.53 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 1.21 - 0.259 = 0.95 \text{ V}$$

Exercise 6.9

$$\text{Number of gates} = \frac{P_{total}}{P_{gate}} = \frac{20}{0.25 \times 10^{-3}} = 80{,}000$$

Exercise 6.10

We simulated the cascade connection of three inverters. Except for resistor values and transistor parameters the circuit is identical to Figure 6.23 in the book. The simulation is stored in the file named Exer6_10. After running the simulation the input and output of the last gate are plotted. The plot is similar to Figure 6.24 in the book. Using the cursor we determined that $t_{PHL} = 19$ ns and $t_{PLH} = 68$ ns.

Exercise 6.11

(a) Increasing R_D increases t_{PLH} because the load capacitance must be charged through R_D.

(b) Increasing R_D has negligible effect on t_{PHL} because the load capacitance is discharged through the transistor.

(c) Increasing R_D has no effect on V_{OH} which is equal to the power-supply voltage.

(d) Increasing R_D reduces V_{OL} because less current flows through the on resistance of the FET in the low state.

(e) Larger resistances usually require greater chip area.

Exercise 6.12

(a) Increasing W/L has virtually no effect on t_{PLH} because the load capacitance charges through R_D.

(b) Increasing W/L decreases t_{PHL} because higher currents flow through the transistor discharging the load capacitance more quickly.

(c) Increasing W/L has no effect on V_{OH} which equals the power-supply voltage.

(d) Increasing W/L reduces the on resistance of the transistor thereby decreasing V_{OL}.

Exercise 6.13

(a) Increasing the load capacitance increases t_{PLH} because the time constant $R_D C$ is greater.

(b) Increasing the load capacitance increases t_{PHL} because more charge must be removed from C.

(c) and (d) Increasing the load capacitance has no effect on the steady-state operation of the circuit. Thus V_{OH} and V_{OL} are unaffected.

Exercise 6.14

See Table 6.2 in the book.

Exercise 6.15

See Figure 6.34 in the book.

Exercise 6.16

Referring to the transfer characteristic in Figure 6.34 we see that for $v_I = V_{DD}/2$ we have $v_O = V_{DD/2}$. For the NMOS transistor, $v_{GS} = v_I = 1.5$ and $v_{DS} = v_O = 1.5$ Notice that the NMOS operates in the saturation region. Thus the current flowing through the NMOS is $i_{Dn} = = K(v_{GS} - V_{to})^2 = 100 \times 10^{-6}(1.5 - 0.6)^2 = 81\ \mu A$.

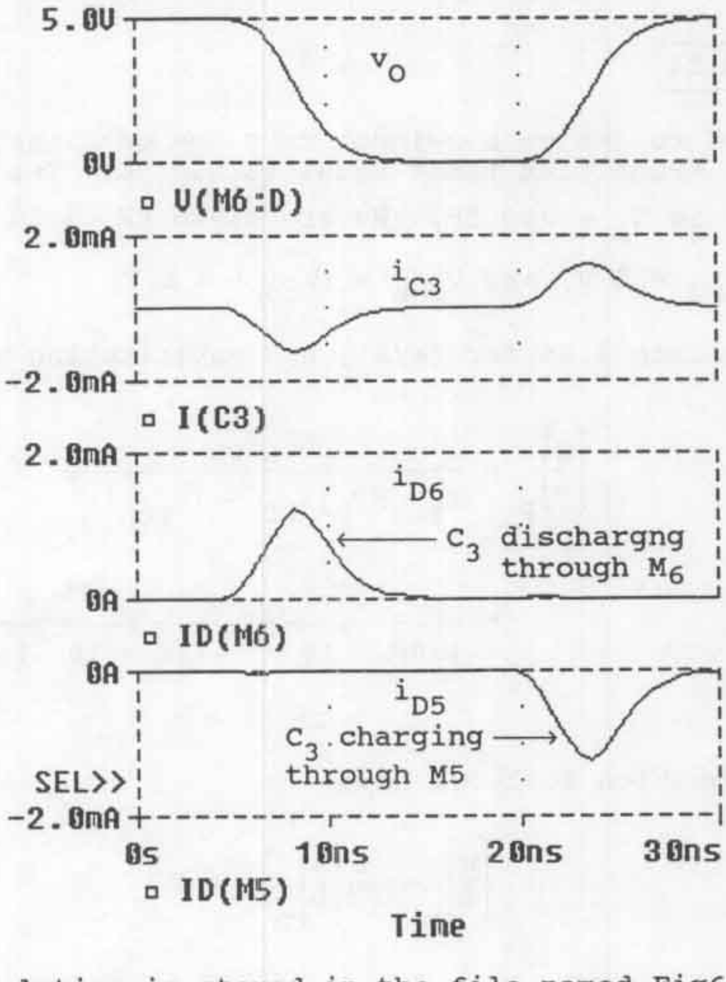
Exercise 6.17

The simulation is stored in the file named Exer6_17. After running the simulation we used the cursor to determine that $t_{PLH} = t_{PHL} \cong 1.62$ ns.

Exercise 6.18

The circuit schematic is stored in file Exer6_18. After running the simulation we used the cursor to determine that $t_{PHL} = t_{PLH} = 2.33$ ns.

Exercise 6.19



The simulation is stored in the file named Fig6_37. After running the simulation we used Probe to obtain plots of the currents and output voltage as shown. The drain current of the PMOS is negative because PSpice references currents into the device terminals. On the other hand, in the book we have referenced drain currents out of the device for PMOS transistors.

Exercise 6.20

A	B	M1	M2	M3	M4	X
Low	Low	On	On	Off	Off	High
Low	High	On	Off	Off	On	High
High	Low	Off	On	On	Off	High
High	High	Off	Off	On	On	Low

Exercise 6.21

We need to design a 2-input CMOS NOR gate that has symmetrical transition times equal to 200 ps. The total load capacitance is $C_L = 200$ fF. We are given $KP_n = 50\ \mu A/V^2$, $KP_p = 25\ \mu A/V^2$, $V_{DD} = 5$ V, and $V_{ton} = |V_{top}| = 1$ V.

Solving Equation 6.36 for $(W/L)_p$ and substituting values we have

$$\left(\frac{W}{L}\right)_p = \frac{MC_L V_{DD}}{t_{PLH} KP_p (V_{DD} - |V_{top}|)^2}$$

$$= \frac{2(200 \times 10^{-15})5}{(200 \times 10^{-12})(25 \times 10^{-6})(5 - 1)^2}$$

$$= 25$$

Now using Equation 6.31, we have

$$\left(\frac{W}{L}\right)_n = \frac{1}{2M}\left(\frac{W}{L}\right)_p = 6.25$$

Exercise 6.22

The circuit is the same as the NOR gate shown in Figure 6.49 in the book except that transistors $M_A, M_B, \ldots, M_M$ must be connected in series rather than parallel.

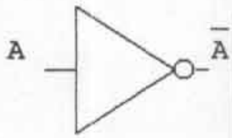
Problem 6.1

A truth table lists all combinations of the input variables and the corresponding output values.

Problem 6.2

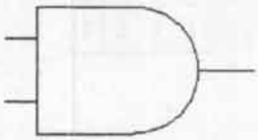
$$AB = \overline{\overline{A} + \overline{B}} \quad \text{and} \quad (A + B) = \overline{\overline{A}\,\overline{B}}$$

Problem 6.3

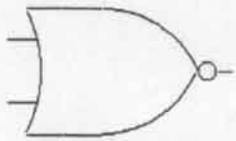


A	$\overline{A}$
0	1
1	0

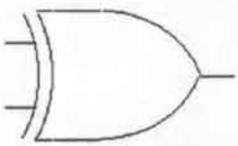
Inverter



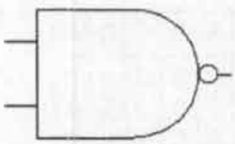
AND



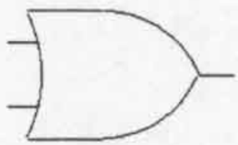
NOR



Exclusive OR



NAND



OR

A	B	AND	OR	XOR	NAND	NOR
0	0	0	0	0	1	1
0	1	0	1	1	1	0
1	0	0	1	1	1	0
1	1	1	1	0	0	0

Problem 6.4

One way to prove the validity of a Boolean algebra equation is to show that both sides yield the same result for all combinations of the logic variables.

Problem 6.5

(a) $D = ABC + A\overline{B}$

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

(b) $E = AB + A\overline{B}C + \overline{C}D$

A	B	C	D	E
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

(c) $Z = WX + \overline{(W + Y)}$

W	X	Y	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Problem 6.6

(a) $F = (A + B)\overline{C}$ (b) $F = A + B + \overline{BC}$ (c) $F = D + AB + \overline{BC}$

Problem 6.7

A	B	A + B	AB	$\overline{A}$	$\overline{A}$ + AB	(A + B)($\overline{A}$ + AB)
0	0	0	0	1	1	0
0	1	1	0	1	1	1
1	0	1	0	0	0	0
1	1	1	1	0	1	1

The columns for $(A + B)(\overline{A} + AB)$ and B are the same. Thus we have shown that $(A + B)(\overline{A} + AB) = B$.

Problem 6.8

A	B	C	A + B	A + C	(A + B)(A + C)	A + BC
0	0	0	0	0	0	0
0	0	1	0	1	0	0
0	1	0	1	0	0	0
0	1	1	1	1	1	1
1	0	0	1	1	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

The two right-most columns are the same thus we have shown that

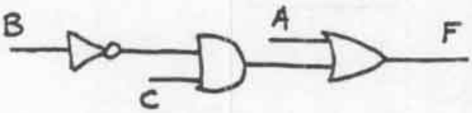
$$(A + B)(A + C) = A + BC$$

Problem 6.9

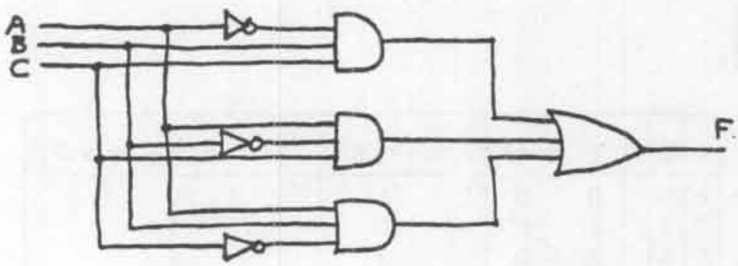
A	B	$A + \bar{A}B$	$A + B$
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1

Problem 6.10

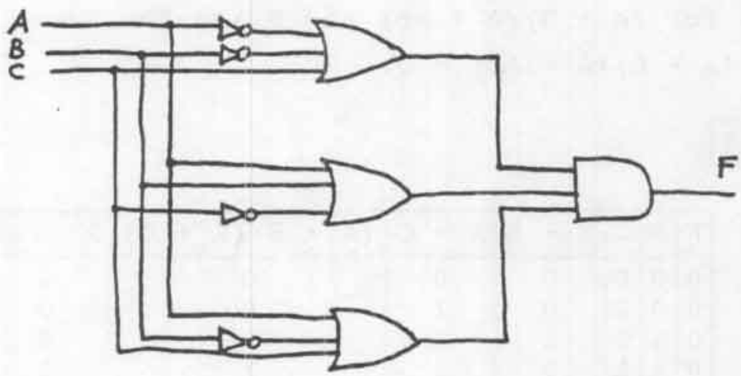
(a)



(b)



(c)



Problem 6.11

(a) $F = AB + (\bar{C} + A)\bar{D} = \overline{(\bar{A} + \bar{B})(\bar{A}C + D)}$

(b) $F = A(\bar{B} + C) + D = \overline{(\bar{A} + B\bar{C})\bar{D}}$

(c) $F = A\bar{B}C + A(B + C) = \overline{(\bar{A} + B + \bar{C})(\bar{A} + \bar{B}\,\bar{C})}$

Problem 6.12

- V_{IL} is the highest input voltage guaranteed to be accepted as logic 0.
- V_{IH} is the lowest input voltage guaranteed to be accepted as logic 1.
- V_{OL} is the highest logic-0 output voltage produced (provided that the input voltages are higher than V_{IH} or lower than V_{IL}).
- V_{OH} is the lowest logic-1 output voltage produced (provided that the input voltages are lower than V_{IL} or higher than V_{IH}).
- $NM_H = V_{OH} - V_{IH}$
- $NM_L = V_{IL} - V_{OL}$
- I_{OH} is the current that the output is capable of sourcing when the output is high.
- I_{OL} is the maximum current that the output can sink when the gate output is in the low state.
- I_{IL} is the worst-case (maximum magnitude) input current, provided that the input voltage is in the acceptable logic-0 input range.
- I_{IH} is the worst-case input current for a high input.

Problem 6.13

When a logic inverter is sourcing current, current flows out of its output terminal.

Problem 6.14

Fanout is the number of input terminals connected to the output of the driver.

Problem 6.15

The power delivered to the inverter by the power supply when the logic levels are constant is called the static power or quiescent power.

Dynamic power is the energy required to charge the load capacitance divided by the switching period.

Problem 6.16

$$P_{dynamic} = fC_L(V_{SS})^2$$
$$= (400 \times 10^6)(100 \times 10^{-15})3^2$$
$$= 0.36 \text{ mW}$$

Problem 6.17

See Figure 6.15 in the book.

Problem 6.18

The speed-power product of a logic inverter is the product of the power dissipation and the propagation delay.

Problem 6.19

See Figure 6.9 in the book.

Problem 6.20

$$NM_H = V_{OH} - V_{IH} = 4.5 - 3 = 1.5 \text{ V}$$
$$NM_L = V_{IL} - V_{OL} = 1.5 - 1 = 0.5 \text{ V}$$

Problem 6.21

Many correct answers can be given. See Figure 6.16 in the book for one example.

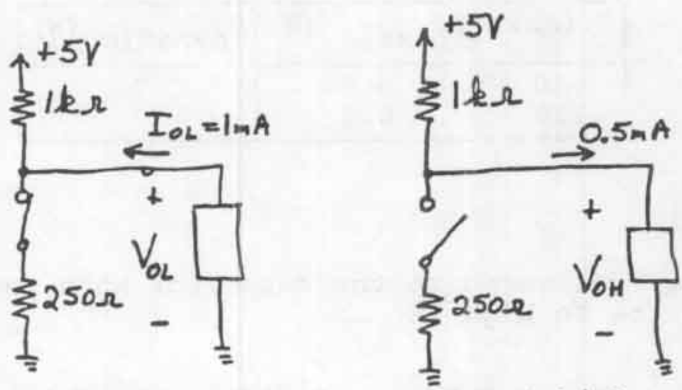
Problem 6.22

With the output connected to the input we have $v_O = v_I$. If we plot this on the inverter characteristic the operating point is at the intersection of the line and the characteristic.

An alternative solution is to obtain the equation for the appropriate portion of the characteristic which is $v_O = -3.6v_I + 11.2$. Then we substitute $v_O = v_I$ and solve obtaining $v_O = v_I = 2.43$ V.

Problem 6.23

Because the switch is open for $v_I \le 2$ V we conclude that $V_{IL} = 2$ V. Similarly because the switch is closed for $v_I \ge 3.5$ V we conclude that $V_{IH} = 3.5$ V. Given that $I_{OL} = -1$ mA we can compute the largest output voltage in the low state by solving the circuit with the switch closed as shown below.



Input low Input high

Writing a current equation for the circuit with the switch closed we have

$$\frac{V_{OL}}{250} + \frac{V_{OL} - 5}{1000} = 1 \text{ mA}$$

Solving we obtain $V_{OL} = 1.2$ V. Similarly solving the circuit with the switch open we obtain $V_{OH} = 4.5$ V. Finally the noise margins are

$$NM_H = V_{OH} - V_{IH} = 4.5 - 3.5 = 1 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 2.0 - 1.2 = 0.8 \text{ V}$$

Problem 6.24

Dynamic power is proportional to frequency $P_{dynamic} = If$. The total power dissipation is the sum of the static dissipation and the dynamic power.

$$P = P_{static} + Kf$$

Using the data given, we can write the following two equations

$$1.5 = P_{static} + 10^7 K$$

$$2.5 = P_{static} + 2 \times 10^7 K$$

Solving we find $P_{static} = 0.5$ W and $K = 10^{-7}$.

f (MHz)	P_{static} (W)	$P_{dynamic}$ (W)
10	0.5	1
20	0.5	2

Problem 6.25

The energy delivered to the capacitor when the output switches from low to high is

$$\text{Energy} = \frac{1}{2} CV_{OH}^2 - \frac{1}{2} CV_{OL}^2 = 0.5(20 \times 10^{-12})(4^2 - 1^2) = 150 \text{ pJ}$$

When the output switches low this energy is dissipated. Thus the dynamic power is the energy dissipated per cycle times the frequency.

$$P_{dynamic} = \text{Energy} \times f = 150 \times 10^{-12} \times 25 \times 10^6 = 3.75 \text{ mW}$$

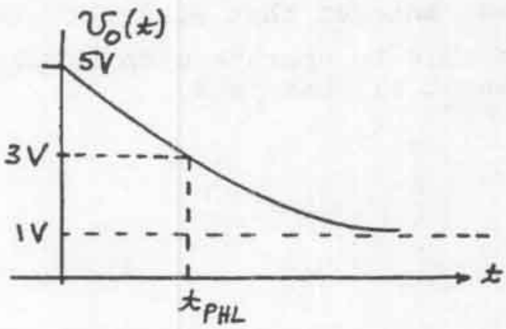
Problem 6.26

(a) With the switch closed, we have

$$V_{OL} = 5 \frac{250}{1000 + 250} = 1 \text{ V}$$

With the switch open, the output voltage is $V_{OH} = 5$ V.

(b) The figure shows the waveform for the high-to-low transition.



The output voltage is given by

$$v_O(t) = 1 + 4\exp(-t/\tau)$$

where τ is the time constant of the circuit. The time constant is the product of the capacitance and the Thévenin resistance of the gate with the switch closed. The Thévenin resistance is the parallel combination of the 1 kΩ and 250 Ω resistances which is 200 Ω. Thus we have $\tau = 200C = 0.4$ ns. t_{PLH} is the time required for the output voltage to make half of the transition (at which time we have $v_O = 3$ V). Thus we can write:

$$3 = 1 + 4\exp(-t_{PHL}/\tau)$$

Solving we find $t_{PHL} = \tau\ln(2) = 0.277$ ns.

Equation 6.23 in the book applies for the low-to-high transition with $R_D = 1$ kΩ. Thus we have

$$t_{PLH} = -R_D C\ln(0.5) = 0.6931 R_D C = 1.386 \text{ ns}$$

Finally we have

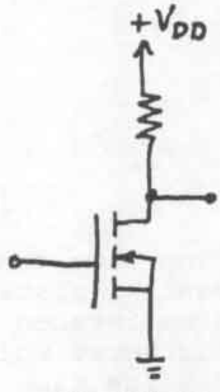
$$t_{PD} = (1/2)(t_{PHL} + t_{PLH}) = 0.832 \text{ ns}$$

(c) The static power dissipation with the output high is zero. With the output low the current taken from the power supply in steady state is (5 V)/(1000 + 250) = 4 mA. Thus the power dissipation in the low output state is 5 V × 4 mA = 20 mW.

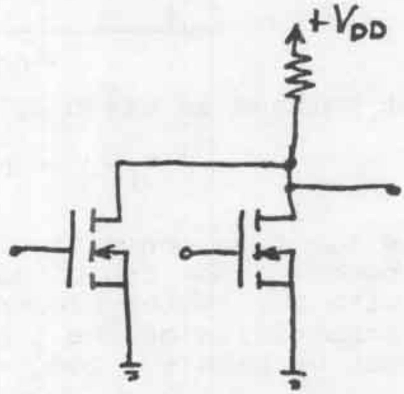
Problem 6.27

In the high state the maximum fanout is the largest integer that does not exceed $|I_{OH}|/I_{IH} = 6$. In the low state the maximum fanout is the largest integer that does not exceed $I_{OL}/|I_{IL}| = 4$. The circuit must be able to operate with outputs in either state. Thus the maximum fanout allowed is 4.

Problem 6.28



Inverter



Two-input NOR gate

Problem 6.29

To ensure large noise margins, we need $V_{OL} \ll V_{DD}$. To achieve this, we must have $R_D \gg R_{on}$.

Problem 6.30

To decrease static power dissipation in the low output state we should (a) increase R_D; (b) reduce W; (c) increase L; (d) reduce V_{DD}.

Problem 6.31

The advantages of increasing R_D are reduced power dissipation and reduced V_{OL}. Disadvantages are longer switching times and increased chip area.

Problem 6.32

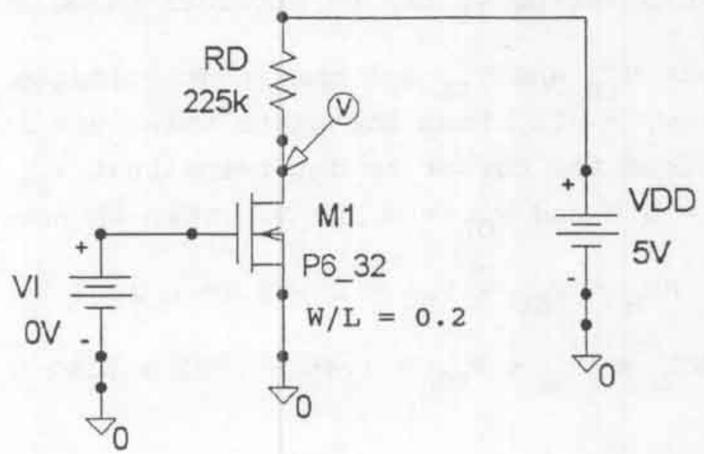
To achieve static power of 0.1 mW in the low output state, we require $I_{DD} = (0.1 \text{ mW})/(5 \text{ V}) = 20\ \mu\text{A}$. Then we have $R_D + R_{on} = (5 \text{ V})/(20\ \mu\text{A}) = 250\ \text{k}\Omega$.

To achieve $V_{OL} = V_{DD}R_{on}/(R_D + R_{on}) = 0.5$ V we need to design for $R_D = 9R_{on}$. Then because we need $R_D + R_{on} = 250\ \text{k}\Omega$, we find that $R_D = 225\ \text{k}\Omega$ and $R_{on} = 25\ \text{k}\Omega$. Solving Equation 6.15 for K and substituting values, we have

$$K = \frac{1}{2R_{on}(v_{GS} - V_{to})} = \frac{1}{2(25 \times 10^3)(5 - 1)} = 5\ \mu\text{A/V}^2$$

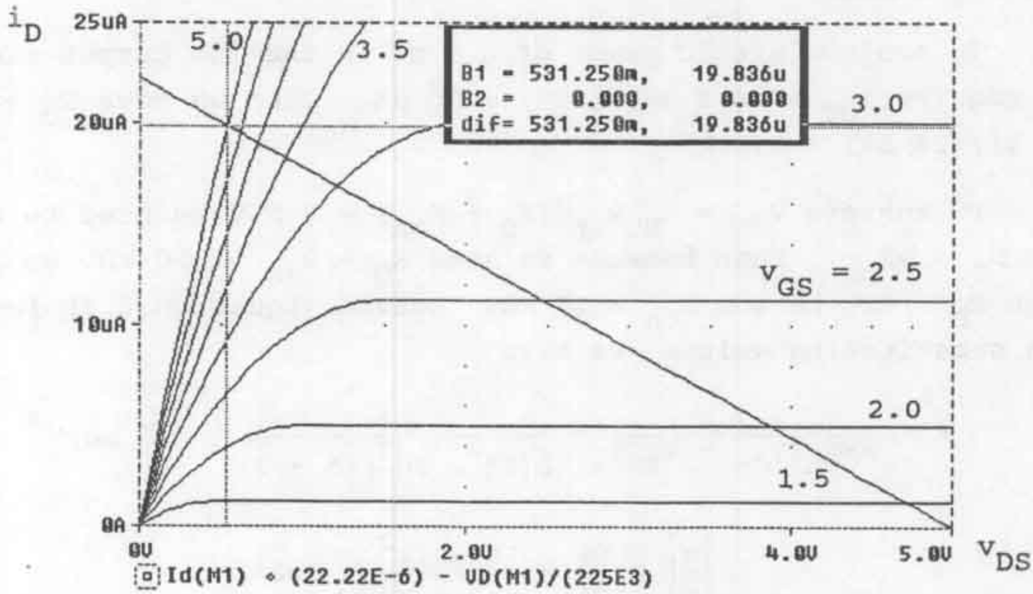
$$\left(\frac{W}{L}\right) = \frac{2K}{KP} = \frac{10\ \mu\text{A/V}^2}{50\ \mu\text{A/V}^2} = 0.2$$

(Actually it would be better to design for W/L = 1 because this would consume less chip area and would produce a lower value of V_{OL}.) The circuit diagram is:



Problem 6.33

We used the simulation stored in P6_33b to plot the characteristics. Then we used Probe to plot the load line and the cursor to determine that V_{OL} = 0.532 which is slightly higher than the design goal of 0.5 V. This is due to the curvature of the NMOS characteristics in the triode region. We could modify W/L by trial and err to attain V_{OL} = 0.5 V if desired.



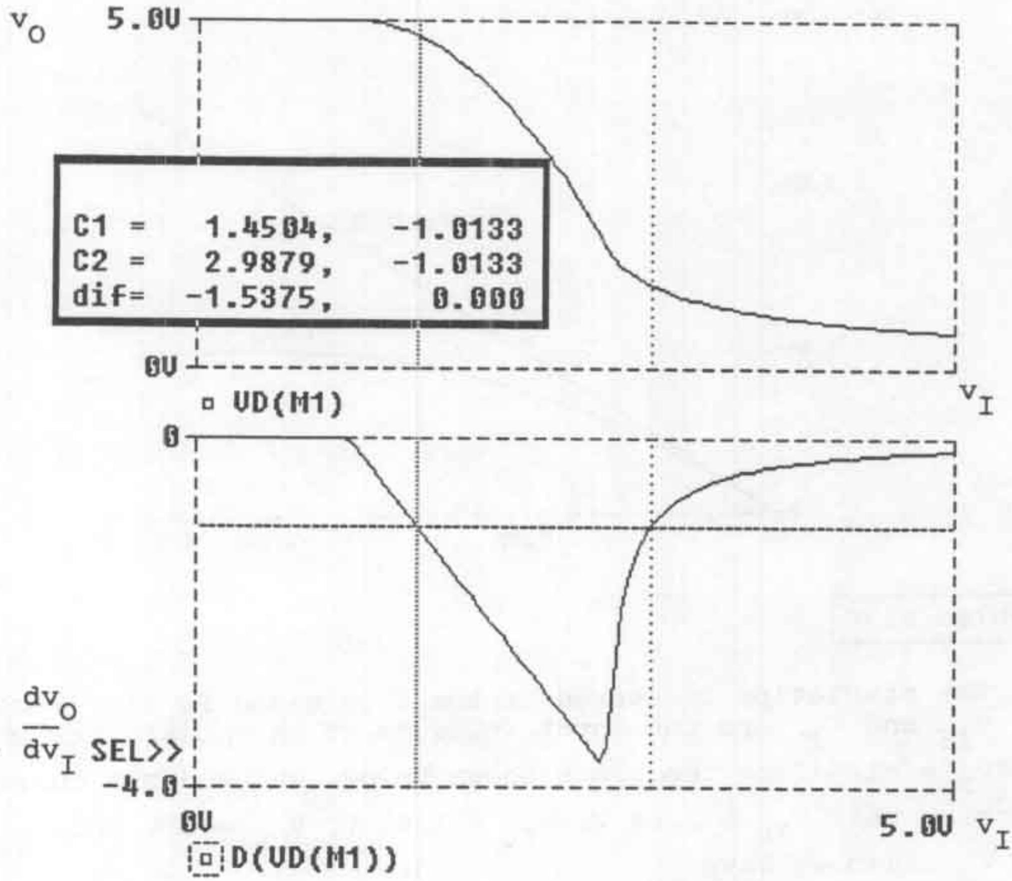
Problem 6.34

The circuit diagram is shown in the solution for Problem 6.32. The simulation is stored in the file named P6_34. Plots of v_O and dv_O/dv_I versus v_I can be obtained using Probe.

Recall that V_{IH} and V_{IL} are the input voltages at the points for which $dv_O/dv_I = -1$. From the plots which are shown on the next page, we used the cursor to determine that V_{IH} = 2.99 V, V_{IL} = 1.45 V, V_{OH} = 5 V and V_{OL} = 0.532 V. Then we have

$$NM_H = V_{OH} - V_{IH} = 5 - 2.99 = 2.01 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 1.45 - .532 = 0.92 \text{ V}$$



Problem 6.35

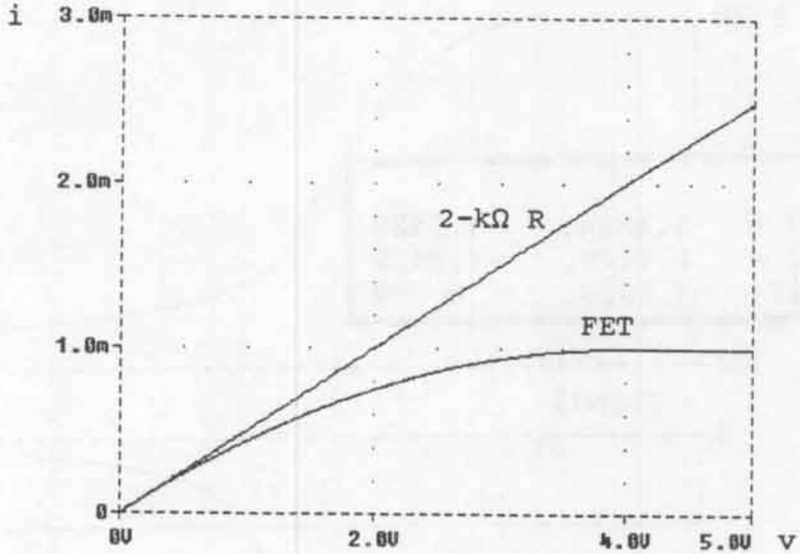
First we solve Equation 6.15 for K and substitute values.

$$K = \frac{1}{2R_{on}(v_{GS} - V_{to})} = \frac{1}{2(2000)(5 - 1)} = 62.5\ \mu A/V^2$$

$$\left(\frac{W}{L}\right) = \frac{2K}{KP} = \frac{2 \times 62.5}{50} = 2.5$$

The simulation is stored in the file named P6_35. The plot of i_D versus v_{DS} is shown on the next page along with the i-v plot for a 2-kΩ resistance.

Of course the two curves match only for small values of voltage. At 1 V the current for the FET is 12.6% less than that of the resistor.

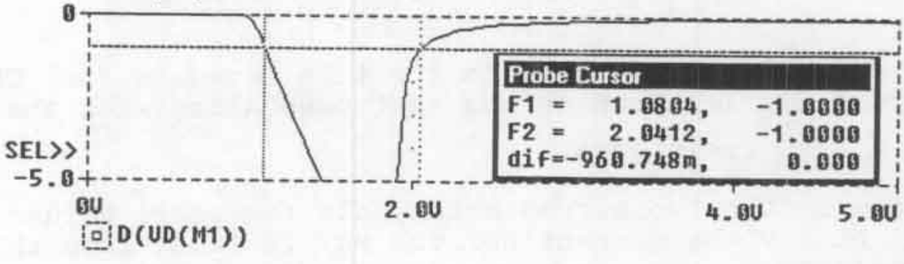


Problem 6.36

The simulation is stored in the file named P6_36. Recall that V_{IH} and V_{IL} are the input voltages at the points for which $dv_O/dv_I = -1$. From the plots shown below, we used the cursor to determine that $V_{IH} = 1.08$ V, $V_{IL} = 2.04$ V, $V_{OH} = 5$ V and $V_{OL} = 0.12$ V. Then we have

$$NM_H = V_{OH} - V_{IH} = 5 - 2.04 = 2.96 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 1.08 - 0.12 = 0.96 \text{ V}$$



Problem 6.37

The analysis to determine t_{PHL} is more difficult than that for t_{PLH} in the resistor-pull-up inverter because the nonlinear relationships for the NMOS need to be taken into account. In the analysis of t_{PLH} we have a simple RC circuit because the NMOS acts as an open circuit.

Problem 6.38

To improve (reduce) the switching intervals of a resistor-pull-up NMOS inverter we should (a) decrease R_D; (b) increase W; (c) decrease L; and (d) increase V_{DD}.

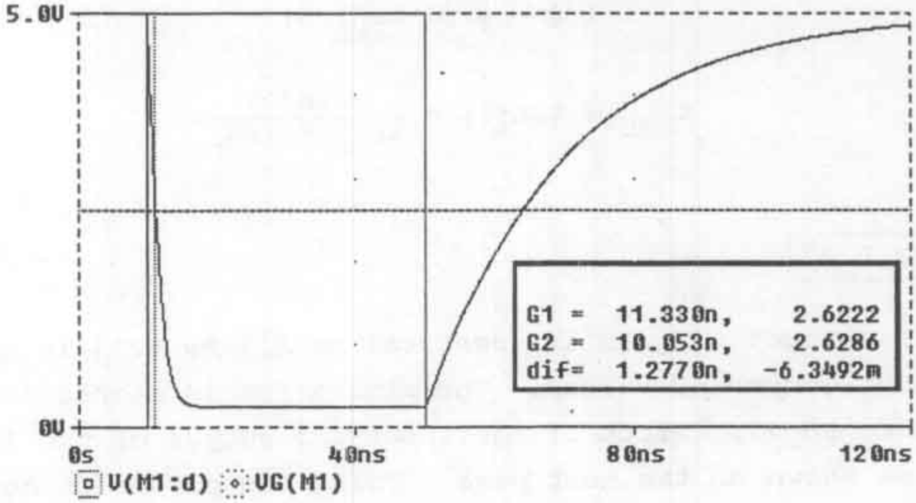
Problem 6.39

Using Equations 6.22 and 6.23, we have

$$t_r = 2.20R_DC = 44 \text{ ns}$$

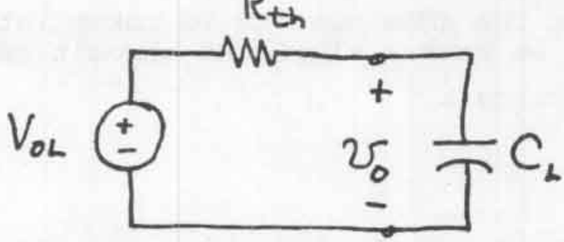
$$t_{PLH} = 0.6931R_DC = 13.9 \text{ ns}$$

The simulation is stored in the file named P6_39. A plot of the transient response is shown below. With the cursor we can verify that t_{PLH} = 13.9 ns and determine that t_{PHL} = 1.3 ns.



Problem 6.40

The Thévenin equivalent circuit with the switch closed is:



The Thévenin resistance is $R_{th} = R_D || R_{on}$ and the Thévenin voltage is $V_{OL} = V_{DD}R_{on}/(R_D + R_{on})$. Assuming that the input switches from low to high at t = 0 and that the circuit was in steady state prior to t = 0, we have

$$v_O(t) = V_{OL} + (V_{DD} - V_{OL})\exp(-t/\tau)$$

where $\tau = R_{th}C_L$ is the time constant. Furthermore t_{PHL} is the time at which $v_O = V_{DD} - (V_{DD} - V_{OL})/2 = (V_{DD} + V_{OL})/2$. Thus we can write

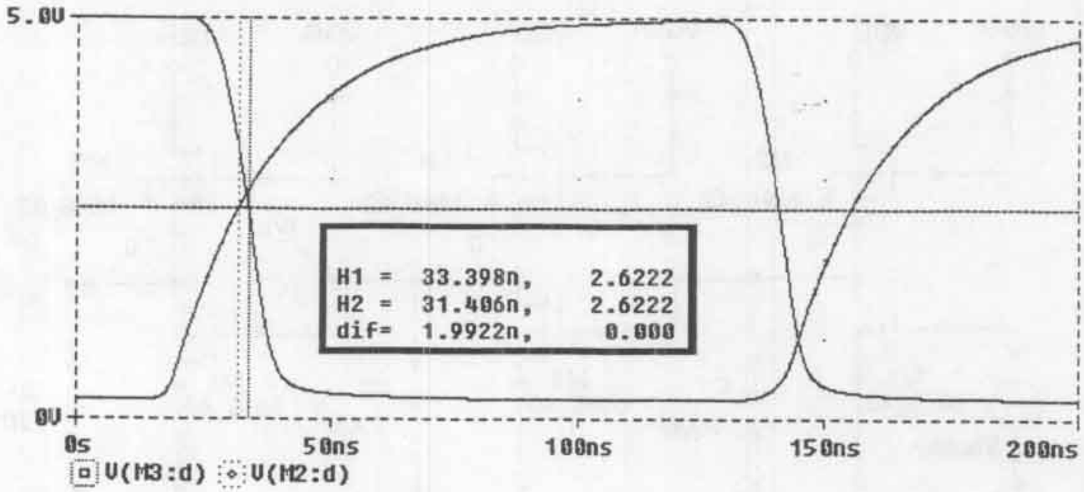
$$(V_{DD} + V_{OL})/2 = V_{OL} + (V_{DD} - V_{OL})\exp(-t_{PHL}/\tau)$$

$$1/2 = \exp(-t_{PHL}/\tau)$$

$$t_{PHL} = \tau\ln(2) = \frac{C\ln(2)}{1/R_D + 1/R_{on}}$$

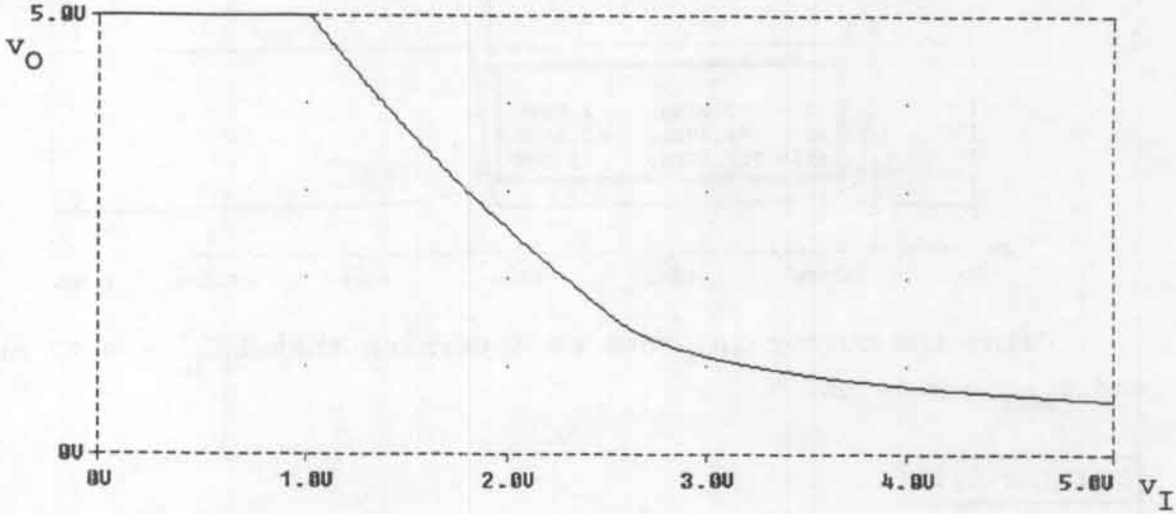
Problem 6.41

The circuit diagram is identical to Figure 6.23 in the book except for component values. The simulation is stored in the file named P6_41. Plots of the input and output of the last stage are shown on the next page. Using the cursor we determine that t_{PHL} = 1.99 ns and t_{PLH} = 14.4 ns.



Problem 6.42

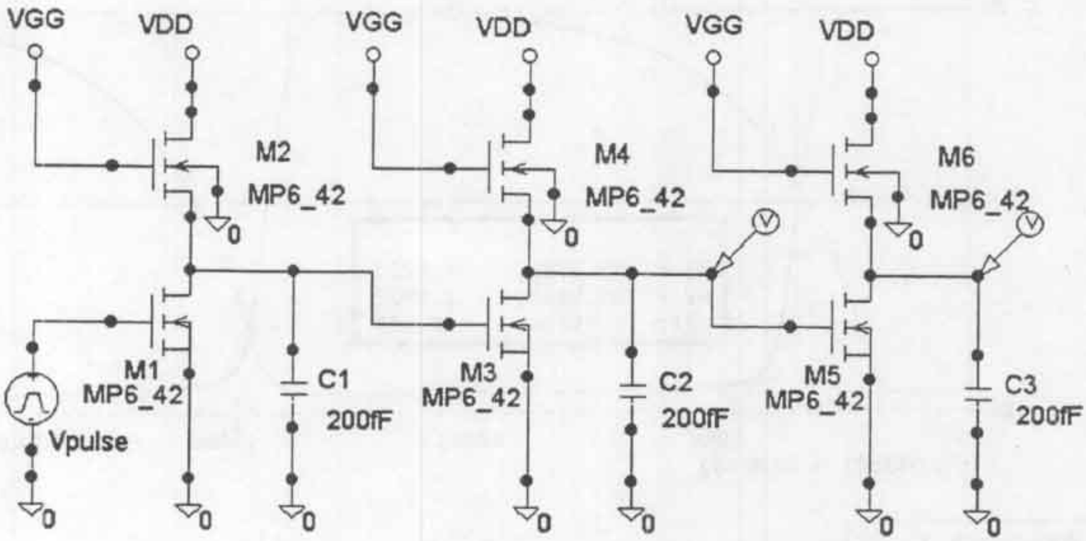
The schematic is stored in the file named P6_42. The transfer characteristic is

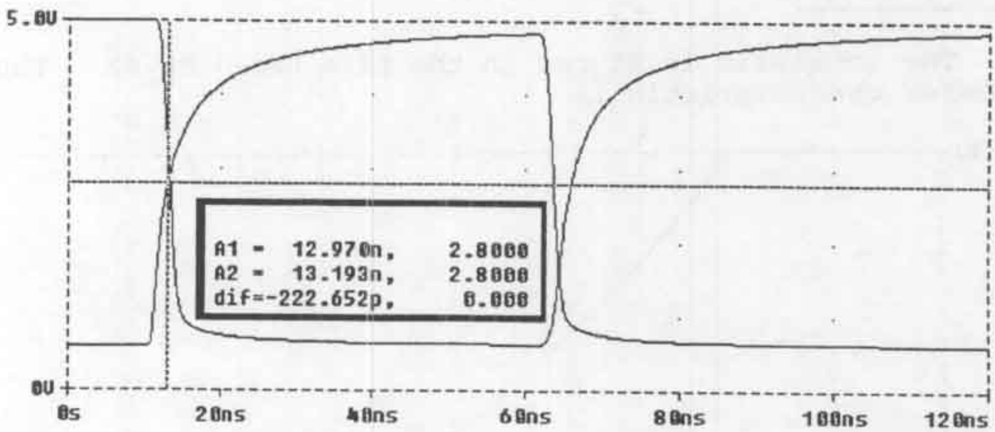


With the output high, the supply current is zero and the static power dissipation is zero. With the output low, the supply current is 477 μA and the static power dissipation is 2.39 mW.

Problem 6.43

The schematic is stored in the file named P6_43 and is shown on the next page with the input and output waveforms for the final stage.





Using the cursor in Probe we determine that t_{PHL} = 0.22 ns and t_{PLH} = 2.26 ns.

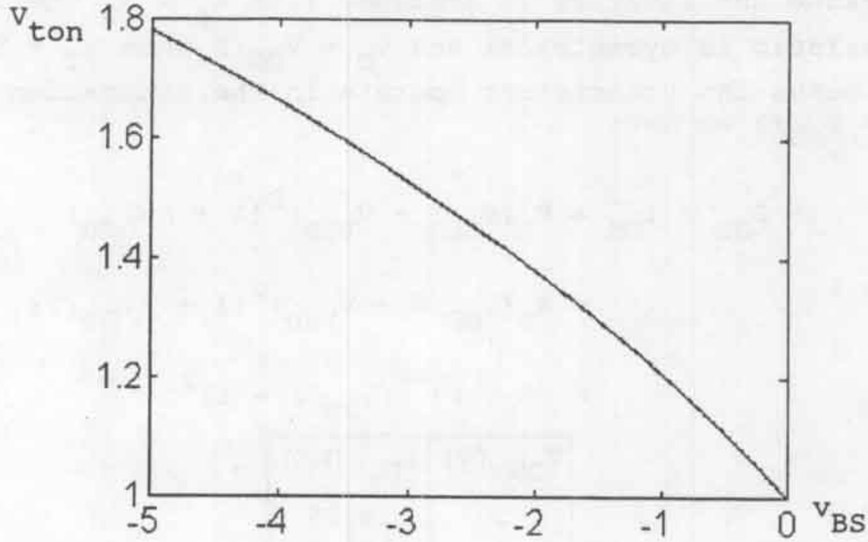
Problem 6.44

Substituting values into Equation 6.24, we have

$$V_{ton} = V_{ton-0} + \gamma_{\nu}\left(\sqrt{2\phi_p - V_{BS}} - \sqrt{2\phi_p}\right)$$

$$= 1 + 0.6\left(\sqrt{1.6 - v_{BS}} - \sqrt{1.6}\right)$$

The plot is shown on the next page.



Problem 6.45

See Figure 6.25e in the book.

Problem 6.46

The output impedance of a CMOS inverter is the on resistance of either the PMOS or the NMOS depending on whether the output is high or low, respectively.

Problem 6.47

Ideally the static power consumption of a CMOS inverter is zero.

Problem 6.48

$$K_n = \left(\frac{W}{L}\right)_n \times \frac{KP_n}{2} = 75\ \mu A/V^2$$

$$K_p = \left(\frac{W}{L}\right)_p \times \frac{KP_p}{2} = 75\ \mu A/V^2$$

Because the inverter is designed with $K_p = K_n$ the transfer characteristic is symmetrical and $v_O = V_{DD}/2$ when $v_I = V_{DD}/2$. For all cases the transistors operate in the saturation region. For $v_I = V_{DD}/2$ we have

$$I_{DD} = i_{Dn} = K_n(v_{GSn} - V_{ton})^2(1 + \lambda v_{DSn})$$

$$= K_n(V_{DD}/2 - V_{ton})^2(1 + \lambda V_{DD}/2)$$

$$= 75 \times 10^{-6}(V_{DD}/2 - 1)^2$$

V_{DD} (V)	I_{DD} (μA)
3	18.75
5	168.8
10	1200

For $v_I = 0$, we have $I_{DD} = 0$ for all values of V_{DD}.

Problem 6.49

In this case the PMOS delivers current to the short circuit. The PMOS has $v_{GS} = -V_{DD}$, $v_{DS} = -V_{DD}$ and $K_p = 75\ \mu A/V^2$. Thus the current is

$$i_{short} = i_{Dp} = K_p(v_{GS} - V_{top})^2 = K_p(-V_{DD} + 1)^2$$

V_{DD} (V)	I_{DD} (mA)	P (mW)
3	0.3	0.9
5	1.2	6.0
10	6.08	60.8

Problem 6.50

For v_I high and $v_O = 0.5$ V, the PMOS is cutoff and the NMOS is operating in the triode region. The current drawn by the NMOS is

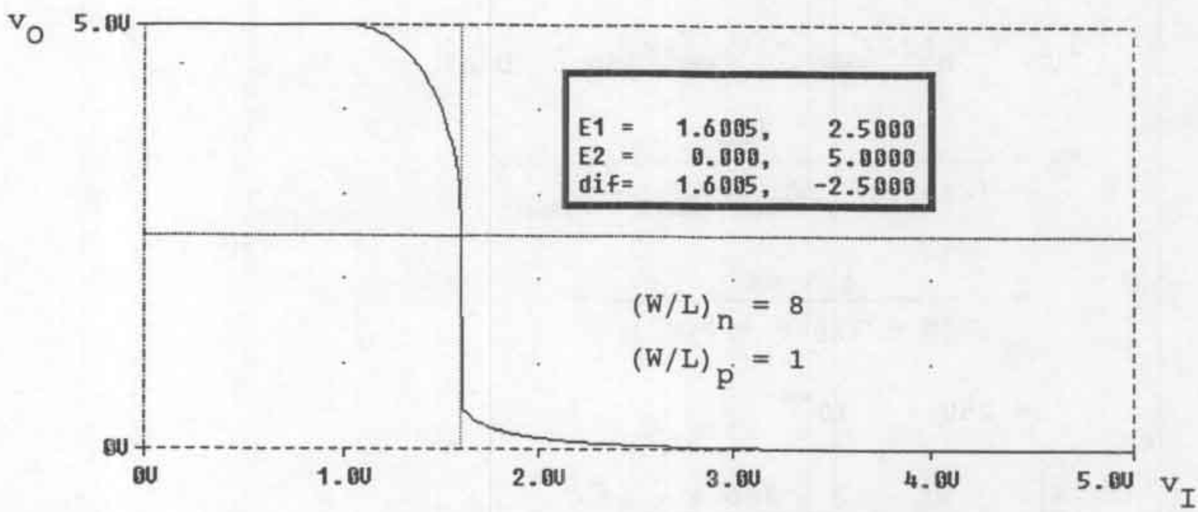
$$i_O = i_{Dn} = K_n[2(v_{GSn} - V_{ton})v_{DSn} - v_{DSn}^2]$$

$$i_O = 75 \times 10^{-6}[2(5 - 1)0.5 - (0.5)^2] = 0.281 \text{ mA}$$

(We are referencing the current i_O into the output terminal of the inverter.) Because this inverter has a symmetrical transfer characteristic we have $i_O = -0.281$ mA for $v_I = 0$ and $v_O = 4.5$ V.

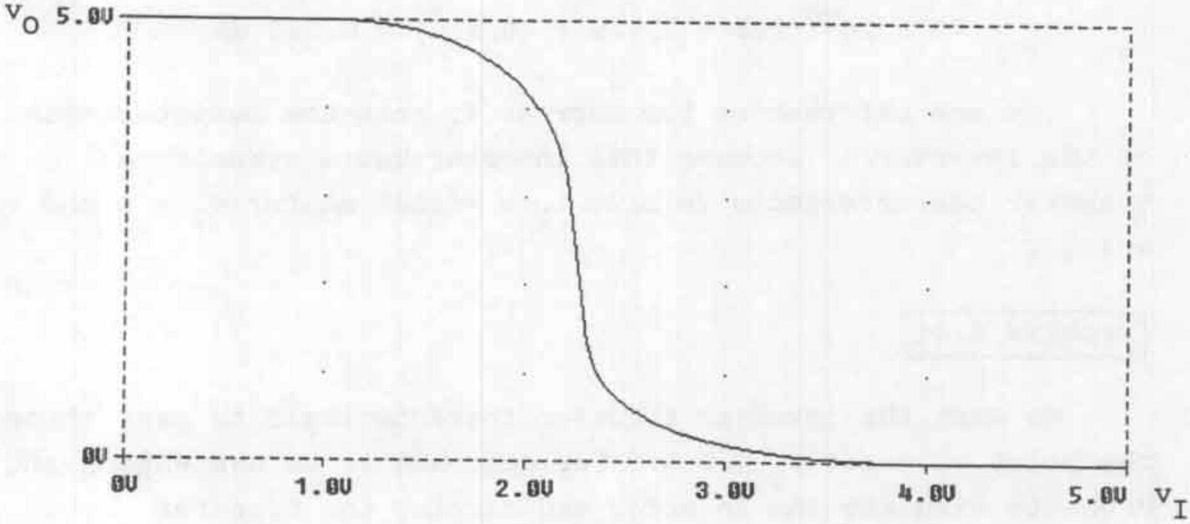
Problem 6.51

We want the inverter transfer characteristic to pass through the point $v_I = 1.6$ $v_O = 2.5$. Our approach is to use PSpice and Probe to simulate the inverter and display the transfer characteristic. We adjust $(W/L)_n$ by trial and err. We find that $(W/L)_n \cong 8$ produces the desired result. The simulation is stored in the file named P6_51 and the transfer characteristic is shown below.



Problem 6.52

The schematic is stored in the file named P6_52. The transfer characteristic is shown on the next page.



Problem 6.53

Let us start by computing the W/L ratio needed for the NMOS to be able to sink 1.5 mA for $v_O = v_{DSn} = 0.8$ V. Here the NMOS operates in the triode region with $v_{GSn} = 5$ V, $v_{DSn} = 0.8$ and $i_{Dn} = 1.5$ mA. We have

$$i_{Dn} = K_n[2(v_{GSn} - V_{ton})v_{DSn} - v_{DSn}^2]$$

$$K_n = \frac{i_{Dn}}{[2(v_{GSn} - V_{ton})v_{DSn} - v_{DSn}^2]}$$

$$= \frac{1.5 \text{ mA}}{[2(5 - 1)0.8 - 0.8^2]} =$$

$$= 260.4 \times 10^{-6}$$

$$\left(\frac{W}{L}\right)_n = \frac{2K}{KP_n} = \frac{2 \times 260.4 \times 10^{-6}}{50 \times 10^{-6}} = 10.4$$

Similarly we solve for $(W/L)_p$ for the PMOS to source 60 μA for $v_O = 2.4$ V.

$$K_p = \frac{i_{Dp}}{[2(v_{GSp} - V_{top})v_{DSp} - v_{DSp}^2]}$$

$$= \frac{60 \times 10^{-6}}{[2(-5 + 1)(-2.6) - (-2.6)^2]}$$

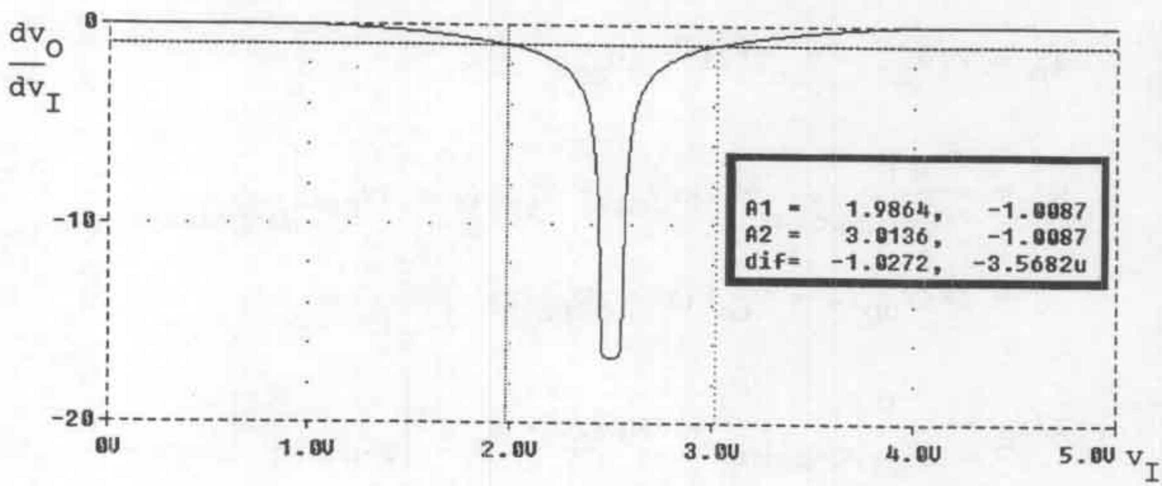
$$= 4.27 \times 10^{-6}$$

$$\left(\frac{W}{L}\right)_p = \frac{2K}{KP_p} = \frac{2 \times 4.27 \times 10^{-6}}{25 \times 10^{-6}} = 0.342$$

Because $(W/L)_p = 0.342$ is a minimum requirement, we could save chip space by selecting $(W/L)_p = 1$ and exceed the requirements. In practice we would also want to allow some design margin.

Problem 6.54

For all three parts we have $V_{OH} = 5$ V and $V_{OL} = 0$ V. The schematic is stored in the file named P6_64. We sweep the input voltage and then use Probe to plot dv_O/dv_I. Finally we determine the input voltages for which the slope equals minus unity. The plot is shown for part (a).

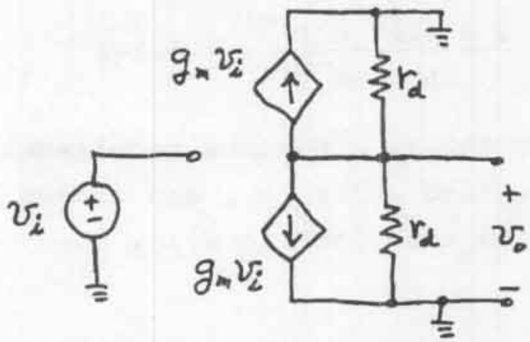


The answers are shown in the table on the next page.

	V_{IL} (V)	V_{IH} (V)	NM_L (V)	NM_H (V)
(a)	1.98	3.01	1.98	1.99
(b)	3.02	3.82	3.02	1.18
(c)	1.18	1.97	1.18	3.03

Problem 6.55

The small-signal equivalent circuit for the CMOS inverter is:



Because the transistors are identical except for polarity, the g_m and r_d values are equal. From the circuit, we have

$$\frac{dv_O}{dv_I} = \frac{v_o}{v_i} = -g_m r_d$$

For the NMOS transistor we have

$$i_D = K(v_{GS} - V_{to})^2(1 + \lambda v_{DS})$$

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q\text{-point}} = 2K(v_{GS} - V_{to})(1 + \lambda v_{DS})\Big|_{Q\text{-point}}$$

$$= 2K(V_{DD}/2 - V_{to})(1 + \lambda V_{DD}/2)$$

$$1/r_d = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{Q\text{-point}} = \lambda K(v_{GS} - V_{to})^2\Big|_{Q\text{-point}}$$

$$= \lambda K(V_{DD}/2 - V_{to})^2$$

$$\frac{dv_O}{dv_I} = -g_m r_d = -\frac{2K(V_{DD}/2 - V_{to})(1 + \lambda V_{DD}/2)}{\lambda K(V_{DD}/2 - V_{to})^2}$$

$$= \frac{-2(1 + \lambda V_{DD}/2)}{\lambda(V_{DD}/2 - V_{to})}$$

Problem 6.56

We assumed that $\lambda_n = 0$, that the input switches instantaneously, and that the NMOS remains in saturation during the entire transient. In other words we assumed that the boundary between the saturation and triode regions (point D in Figure 6.35) is on the left-hand side of point C.

Problem 6.57

From Equations 6.29 and 6.30 we see that the switching times are inversely proportional to W/L. Thus we should increase the W/L ratios of the transistors by a factor of 1.25. (In practice increasing W/L may also increase C_L and an even larger factor may be needed. This can be determined by trial and err using SPICE.)

Problem 6.58

We can compute the switching times using Equations 6.29 and 6.30 which are:

$$t_{PHL} = \frac{C_L V_{DD}}{\left(\frac{W}{L}\right)_n KP_n \ (V_{DD} - V_{ton})^2} \qquad t_{PLH} = \frac{C_L V_{DD}}{\left(\frac{W}{L}\right)_p KP_p \ (V_{DD} - |V_{top}|)^2}$$

	t_{PHL} (ns)	t_{PLH} (ns)
(a)	4.17	4.17
(b)	4.17	0.417
(c)	0.417	4.17

Problem 6.59

This inverter has a symmetrical transfer characteristic. Maximum supply current occurs when $v_I = v_O = V_{DD}/2$. The current is given by

$$I_{DDmax} = K_n(v_{GSn} - V_{to})^2$$

$$= \left(\frac{W}{L}\right)_n \frac{KP_n}{2}(V_{DD}/2 - V_{to})^2$$

$$= 281.3\ \mu A$$

Problem 6.60

For each cycle of the pulse train, a charge of $Q = C_L V_{DD} = 5$ pC is taken from the supply to charge the load capacitance. The average current is Q/T where T is the period of the pulse train. Thus $I_{DDavg} = C_L V_{DD} f = 0.25$ mA. $P_{DDavg} = V_{DD} I_{DDavg} = 1.25$ mW.

Problem 6.61

We solve Equations 6.29 and 6.30 for (W/L) and substitute values.

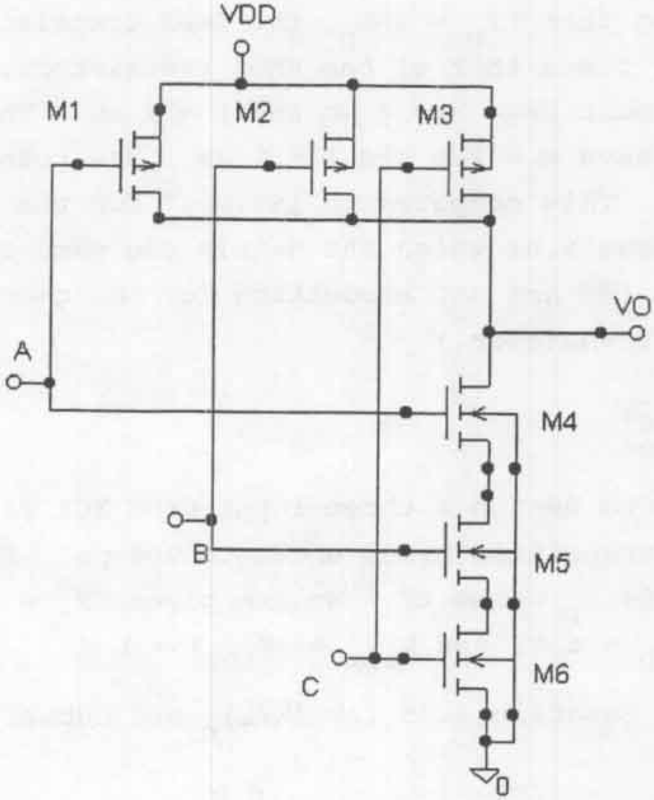
$$\left(\frac{W}{L}\right)_n = \frac{C_L V_{DD}}{KP_n t_{PHL}(V_{DD} - V_{ton})^2}$$

$$= \frac{2 \times 10^{-12} \times 5}{50 \times 10^{-6} \times 500 \times 10^{-12}(5 - 1)^2}$$

$$= 25$$

Similarly we find $(W/L)_p = 50$.

Problem 6.62



Problem 6.63

NAND gates consume less chip area than NOR gates.

Problem 6.64

Assuming that $KP_n = 2KP_p$, all of the transistors have the same dimensions in a two-input NAND gate. For symmetrical operation we have required two NMOS and two PMOS transistors each with W = 4 μm and L = 1 μm. Thus the total area consumed is 16 $(\mu m)^2$. (We are not accounting for the guard bands needed around each transistor.)

Problem 6.65

Assuming that $KP_n = 2KP_p$, the PMOS transistors require W/L that is four times that of the NMOS transistors. Thus the PMOS transistors must have $W = 8\ \mu m$ and $L = 1\ \mu m$. The NMOS transistors have $W = 2 \mu m$ and $L = 1\ \mu m$. The total area consumed is $20\ (\mu m)^2$. This compares to $16\ (\mu m)^2$ for the two-input NAND gate of Problem 6.64 which has nearly the same speed and drive capability. (We are not accounting for the guard bands needed around each transistor.)

Problem 6.66

We need to design a three-input CMOS NOR gate that has symmetrical transition times equal to 200 ps. The total load capacitance is $C_L = 200$ fF. We are given $KP_n = 50\ \mu A/V^2$, $KP_p = 25\ \mu A/V^2$, $V_{DD} = 5$ V, and $V_{ton} = |V_{top}| = 1$ V.

Solving Equation 6.35 for $(W/L)_n$ and substituting values we have

$$\left(\frac{W}{L}\right)_n = \frac{C_L V_{DD}}{t_{PHL}\ KP_n\ (V_{DD} - V_{ton})^2}$$

$$= \frac{(200 \times 10^{-15})5}{(200 \times 10^{-12})(50 \times 10^{-6})(5 - 1)^2}$$

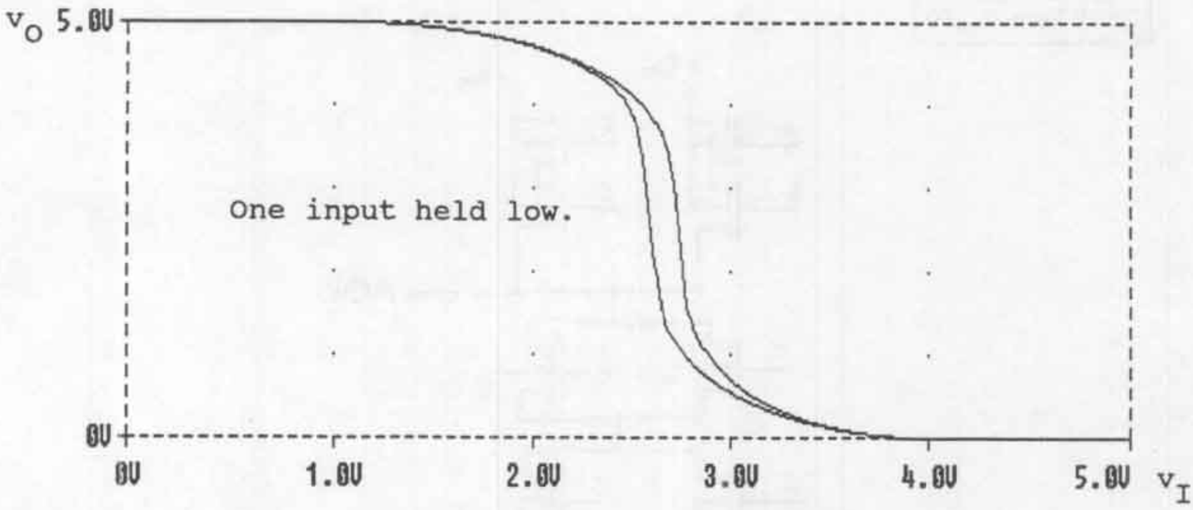
$$= 6.25$$

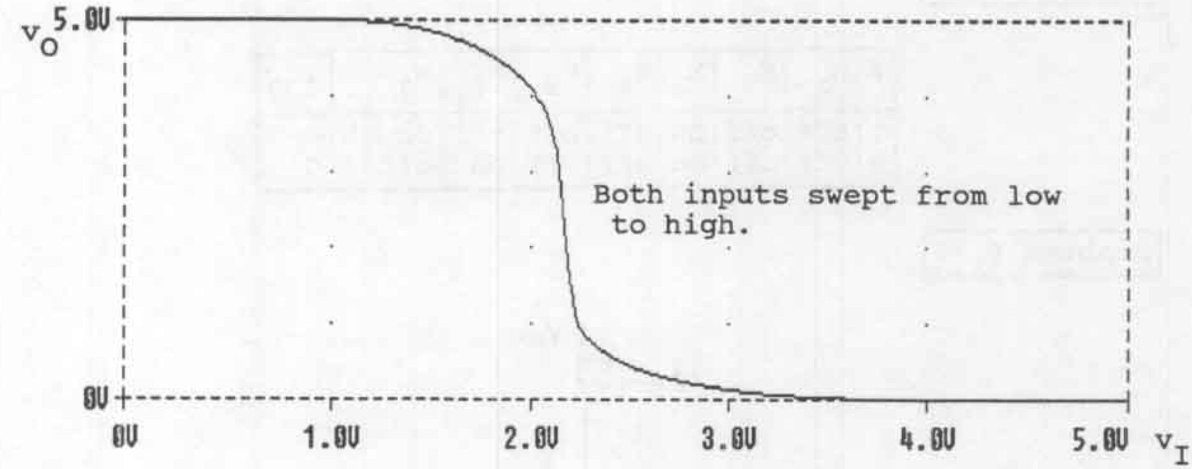
Now using Equation 6.31, we have

$$\left(\frac{W}{L}\right)_p = 2M\left(\frac{W}{L}\right)_n = 37.5$$

Problem 6.67

The schematic is stored in the file named P6_67. The transfer characteristics are shown on the next page.





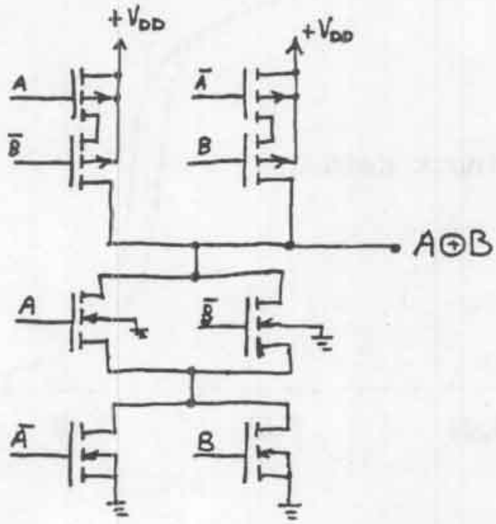
Problem 6.68

The schematic is stored in the file named P6_68. The worst case delays are t_{PHL} = 1.52 ns and t_{PLH} = 2.01 ns.

Problem 6.69

$$F = \overline{A(B + C)} = \overline{A} + \overline{B}\ \overline{C}$$

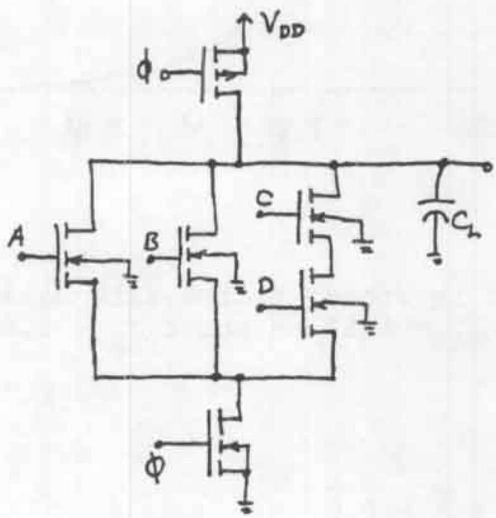
Problem 6.70



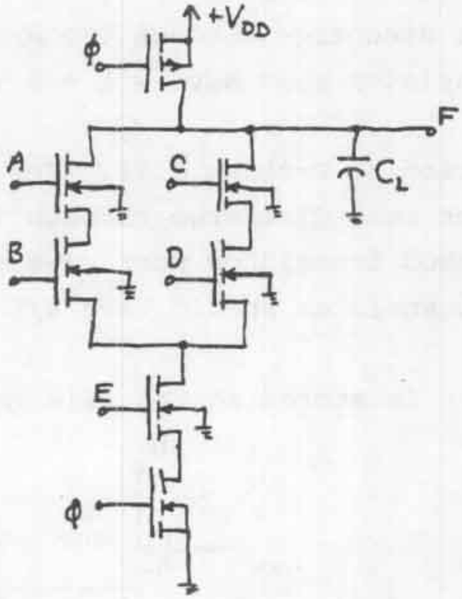
Problem 6.71

ϕ	M_1	M_2	M_3	M_4	M_5	M_6	M_7	F	I_{DD}
1	off	off	on	off	off	off	on	0	0
0	off	off	on	off	off	on	off	1	0

Problem 6.72



Problem 6.73



Problem 6.74

Consider a capacitor that is discharged through an NMOS transistor. Assume that the transistor operates in saturation during the transient. Then the time required to discharge the capacitor to half of the initial voltage is given by Equation 6.35.

$$t_{PHL} = \frac{C_L V_{DD}}{\left(\frac{W}{L}\right)_n KP_n \ (V_{DD} - V_{ton})^2}$$

$$\left(\frac{W}{L}\right)_n = \frac{C_L V_{DD}}{t_{PHL} KP_n \ (V_{DD} - V_{ton})^2} = \frac{(500 \times 10^{-15})5}{(500 \times 10^{-12})(50 \times 10^{-6})(5 - 1)^2}$$

$$= 6.25$$

Now in the worst case, the capacitor must discharge through the series combination of three NMOS transistors. Three NMOS devices in series is equivalent to a single transistor with 1/3 of the W/L for each transistor. Thus transistors M_1, M_2, M_4, M_5 and M_7 need to have W/L = 3 × 6.25 = 18.75. Transistor M_3 should have W/L = 18.75/2 = 9.375. The PMOS M_6 requires W/L = 12.5.

Problem 6.75

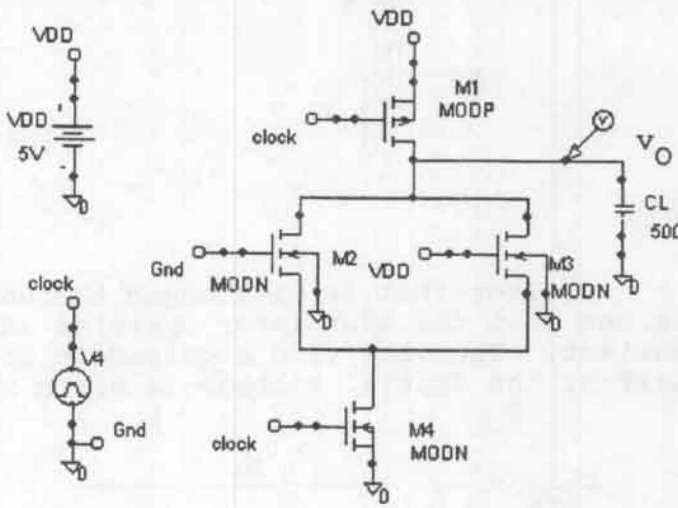
See the solution to Problem 6.74. For a two-input NOR gate, the capacitor must discharge through two NMOS transistors in series. Each transistor must have W/L = 2 × 6.25 = 12.5.

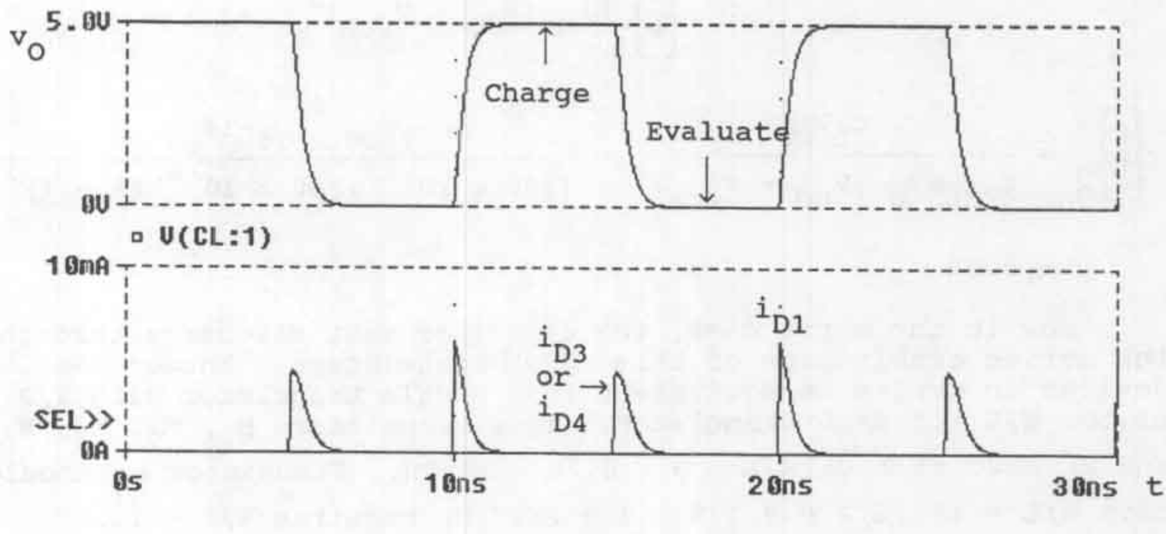
Problem 6.76

See the solution to Problem 6.74. For a two-input NAND gate, the capacitor must discharge through three NMOS transistors in series. Each NMOS transistor must have W/L = 3 × 6.25 = 18.75. The PMOS transistor should have W/L = 12.5.

Problem 6.77

The simulation is stored in the file named P6_77.





Problem 6.78

See Figure 6.51 in the book.

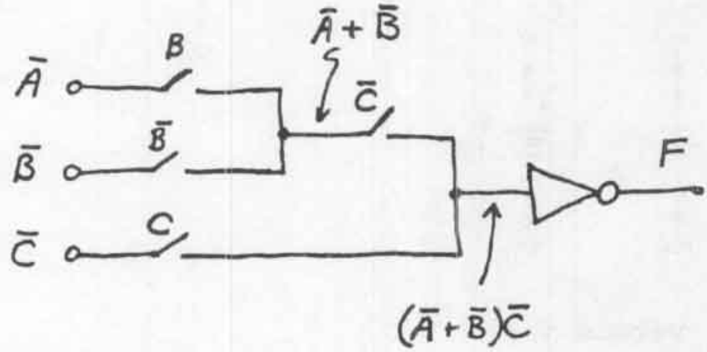
Problem 6.79

The schematic is stored in the file named P6_79. For C high the output voltage is nearly equal to v_I. The maximum magnitude of $v_O - v_I$ is 163 mV. For C low the output is nearly zero.

Problem 6.80

Applying DeMorgan's law we have

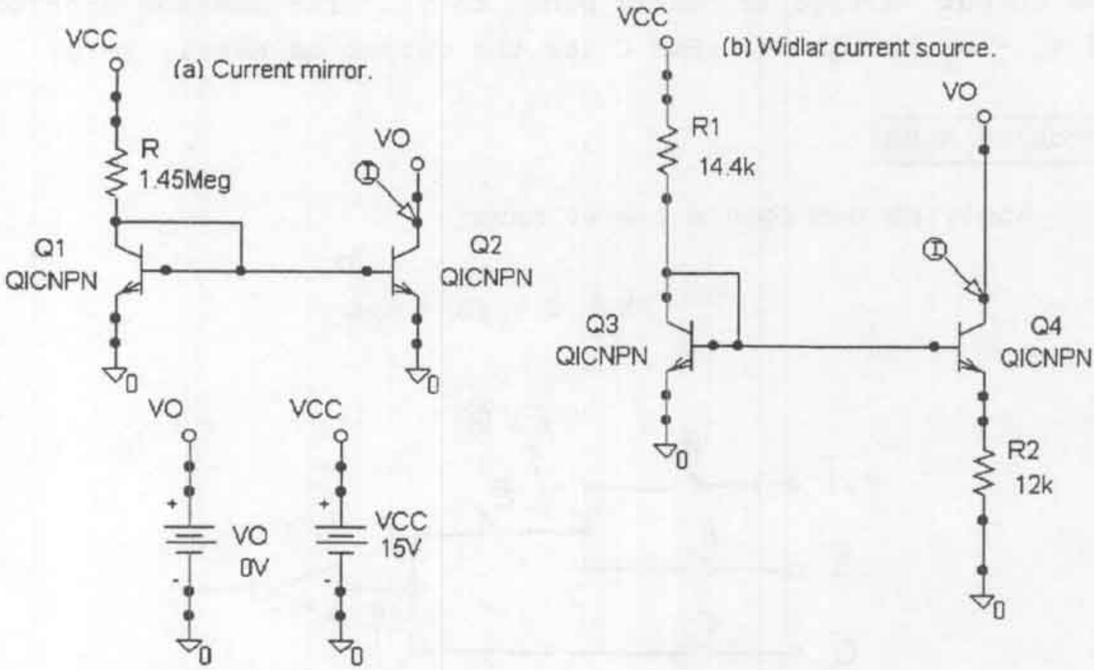
$$F = AB + C = \overline{(\overline{A} + \overline{B})\overline{C}}$$



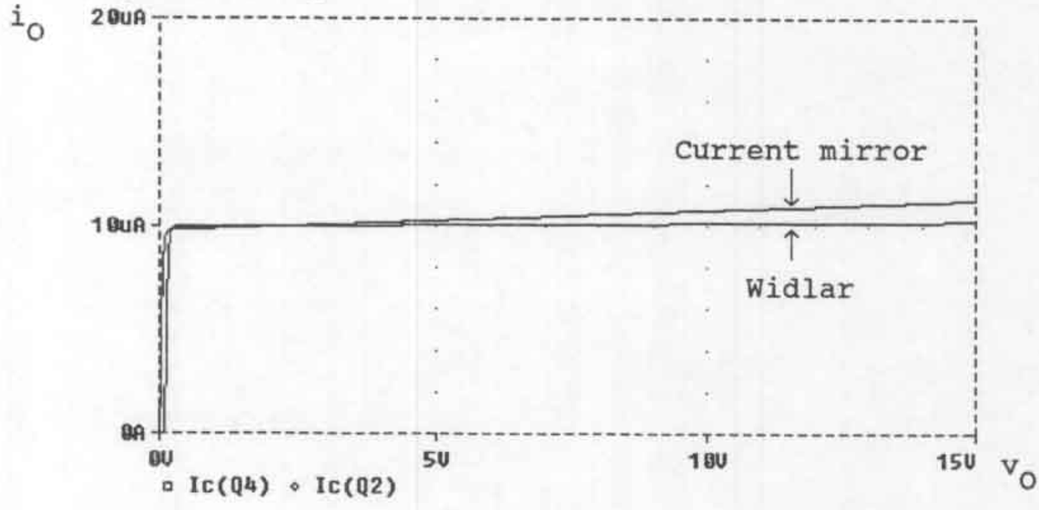
Chapter 7

Exercise 7.1

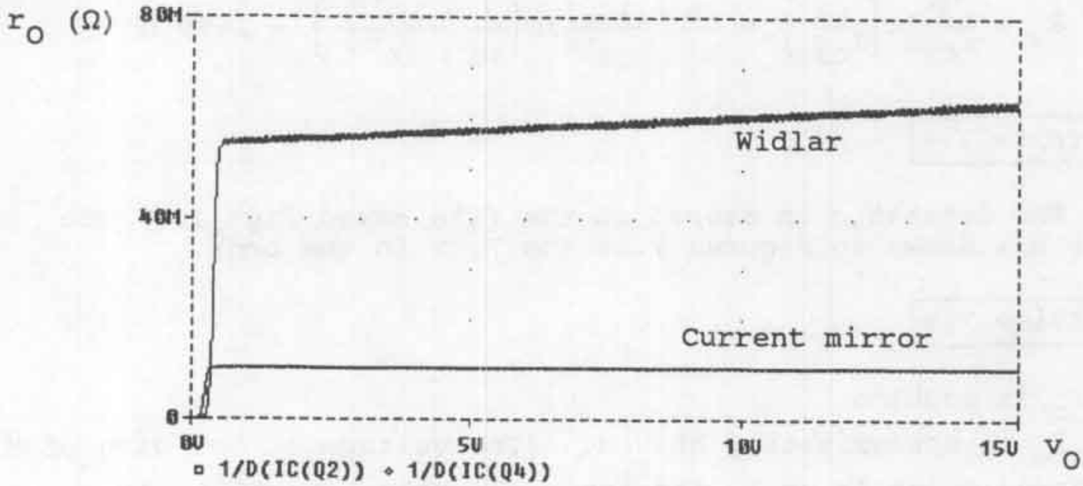
The simulation is stored in the file named Exer7_1. The circuit diagram is:



Plots of i_O versus v_O:



Plots of the output resistance:



For the Widlar source, the compliance range extends from 0.5 to 15 V, and the output resistance is approximately 60 MΩ in the compliance range. For the current mirror the compliance range extends from 0.35 to 15 V and the output resistance is approximately 10 MΩ in the compliance range.

Exercise 7.2

The circuits are shown in Figure 7.13. The schematic is stored in file Fig7_13. The simulation results show that the mirror has an output resistance of approximately 100 kΩ in the compliance range, whereas the Wilson sink has an output resistance ranging from 8 MΩ to 10 MΩ. [Hint: To obtain a plot of the output resistance of the Wilson source, use the **analysis/setup/options** command and change the parameter RELTOL to 10^{-9}, then after the simulation request a plot of 1/D(IC(Q4)).]

Exercise 7.3

Because we are given $A_2 = A_1$, we have $I_{ref} = I_2$. Furthermore, I_2 is specified to be 1 mA. Thus, we must design for $I_{ref} = 1$ mA. Then we have $R_1 = (V_{CC} - V_{EE} - 1.4)/(1\text{ mA}) = 28.6$ kΩ. Because I_5 is specified to be 3 mA we must have $A_5 = 3A_4 = 3$. Then we have

$$R_2 \cong \frac{V_T}{I_{C6}}\ln\left(\frac{I_{C4}}{I_{C6}}\right) = \frac{26 \times 10^{-3}}{100 \times 10^{-6}}\ln\left(\frac{1 \times 10^{-3}}{100 \times 10^{-6}}\right) = 599\ \Omega$$

$$R_3 \cong \frac{V_T}{I_{C3}} \ln\left(\frac{I_{C1}}{I_{C3}}\right) = \frac{26 \times 10^{-3}}{50 \times 10^{-6}} \ln\left(\frac{1 \times 10^{-3}}{50 \times 10^{-6}}\right) = 1558\ \Omega$$

Exercise 7.4

The schematic is stored in the file named Fig7_17. The plots are shown in Figures 7.18 and 7.19 in the book.

Exercise 7.5

(a) I_o is doubled.
(b) I_o is approximately halved. (The voltage at the gate of M_1 decreases slightly so I_1 increases slightly. However, by Equation 7.20, the output current becomes half of I_1.)

Exercise 7.6

(a) I_o is approximately halved.
(b) I_o is doubled.
(c) I_o remains nearly constant.

Exercise 7.7

Many correct answers exist to this exercise. One circuit is shown in Figure 7.20 in the book. First we decided to design for $W_1/L_1 = 2(W_2/L_2)$ so that $I_{D1} \cong 2I_O = 400\ \mu A$. Then we used Equation 7.21 (modified for PMOS transistors) to estimate $R_1 = (V_{DD} - |V_{to}|)/I_{D1} = 35\ k\Omega$. If desired a simulation can be used and R_1 can be adjusted to obtain the exact value of I_O desired. The simulation for Figure 7.20 is stored in the file named Exer7_7.

Exercise 7.8

Many correct answers exist to this exercise. One circuit is shown in Figure 7.21 in the book. First we decided to design for $W_1/L_1 = 2(W_2/L_2)$ so that $I_{D1} \cong 2I_O = 400\ \mu A$. Then we used Equation 7.22 (modified for PMOS transistors) to estimate $R_W =$

$(V_{DD} - 2|V_{to}|)/I_{D1} = 32.5$ kΩ. Then we simulated the circuit and adjusted R_W to 26.6 kΩ by trial and error. The simulation is stored in the file named Exer7_8.

Exercise 7.9

(a) With $v_{i1} = 1$ V and $v_{i2} = 1$ V, the current splits equally between Q_1 and Q_2 so we have $I_{C1} = I_{C2} = 1$ mA. Then $v_{o1} = R_{C1}I_{C1} - 15 = -10$ V, $v_{o2} = R_{C2}I_{C2} - 15 = -10$ V, and $v_{od} = v_{o1} - v_{o2} = 0$.

(b) With $v_{i1} = -1$ V and $v_{i2} = 1$ V the current flows entirely through Q_1 so we have $I_{C1} = 2$ mA and $I_{C2} = 0$ mA. Then $v_{o1} = R_{C1}I_{C1} - 15 = -5$ V, $v_{o2} = R_{C2}I_{C2} - 15 = -15$ V, and $v_{od} = v_{o1} - v_{o2} = 10$.

(c) With $v_{i1} = 1$ V and $v_{i2} = -1$ V, the current flows entirely through Q_2 so we have $I_{C1} = 0$ mA and $I_{C2} = 2$ mA. Then $v_{o1} = R_{C1}I_{C1} - 15 = -15$ V, $v_{o2} = R_{C2}I_{C2} - 15 = -5$ V, and $v_{od} = v_{o1} - v_{o2} = -10$.

Exercise 7.10

See Figure 7.31 in the book.

Exercise 7.11

See Figure 7.32 in the book.

Exercise 7.12

Refer to Figure 7.36 in the book. We can write the following equations:

$$v_{icm} = r_\pi i_{b1} + (R_{EF} + 2R_{EB})(\beta + 1)i_{b1}$$

$$v_{ocm} = -R_C\beta i_{b1}$$

(a) $R_{icm} = \dfrac{v_{icm}}{i_{b1} + i_{b2}} = \dfrac{v_{icm}}{2i_{b1}}$

$$= [r_\pi + (R_{EF} + 2R_{EB})(\beta + 1)]/2$$

(b) $$A_{vcm} = \frac{v_{o1}}{v_{icm}} = \frac{-\beta R_C}{r_\pi + (R_{EF} + 2R_{EB})(\beta + 1)}$$

Exercise 7.13

(a) For the dc analysis, we assume that $v_{in} = 0$. Then by symmetry, we have $I_{E1} = I_{E2} = \frac{1}{2} \times \frac{15 - 0.6}{R_{EB}} = 9.6$ mA. Then $I_{C1} = I_{C2} = \beta I_{E1}/(\beta + 1) = 4.78$ mA. Furthermore, we have $V_{CE1} = V_{CC} + V_{BE1} = 15.6$ V and $V_{CE2} = V_{CC} - I_{C1}R_1 + V_{BE2} = 10.82$ V.

$r_{\pi 1} = r_{\pi 2} = \beta V_T/I_{CQ} = (200 \times 26\text{ mV})/(4.78\text{ mA}) = 1088\ \Omega$

(c) We have

$$v_{id} = v_{i1} - v_{i2} = v_{in} \quad \text{and} \quad v_{icm} = (v_{i1} + v_{i2})/2 = v_{in}/2$$

However, the differential gain is much greater than the common-mode gain, so we can ignore the common-mode component. We have

$$A_{vds} = \frac{v_{o2}}{v_{id}} = \frac{v_{o2}}{v_{in}} = \frac{\beta(R_1 || R_L)}{2r_\pi}$$

$$= \frac{200 \times 667}{2 \times 1088} = 61.3 = 35.7 \text{ dB}$$

$$R_{in} = v_{in}/i_{in} = v_{id}/i_{b1} = 2r_\pi = 2180\ \Omega$$

$$R_o = R_1 = 1000\ \Omega$$

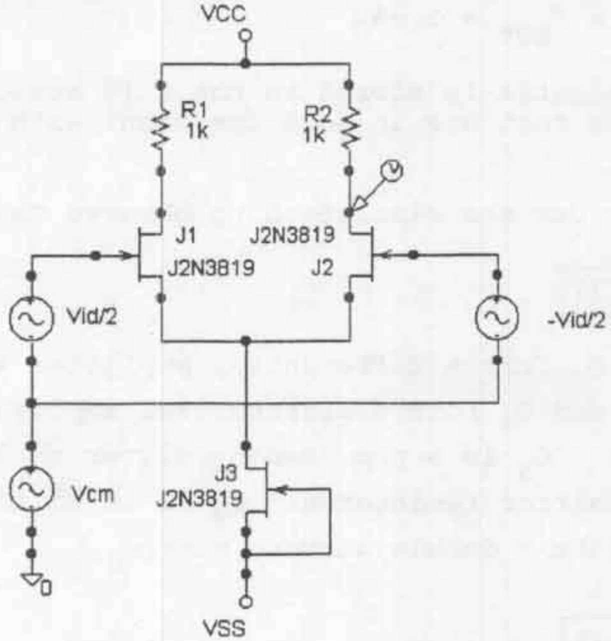
(d) The simulation is stored in file Exer7_13. To obtain a plot of the input impedance versus frequency request a plot of 1/IB(Q1).

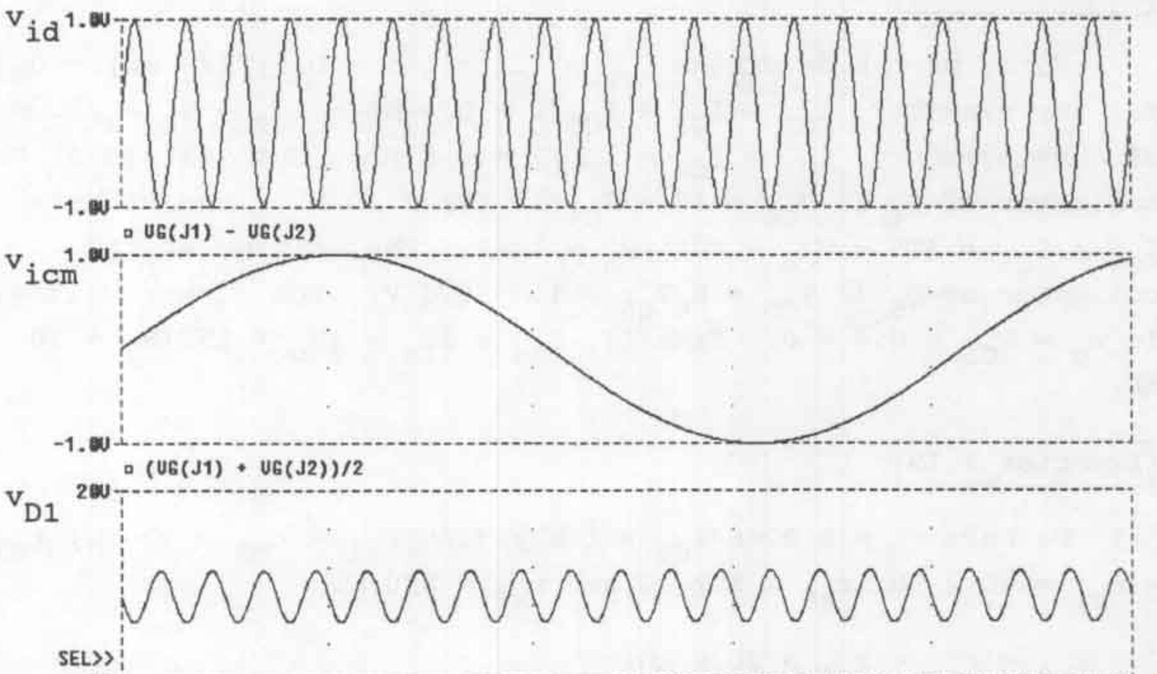
Exercise 7.14

The simulation is stored in the file named Fig7_41.

Exercise 7.15

The simulation is stored in the file named Exer7_15.





Exercise 7.16

(a) $I_{DQ8} = I_{set} = 1$ mA, $I_{DQ1} \cong 2$ mA, $I_{DQ2} = I_{DQ7} = 4$ mA, $I_{DQ3} = I_{DQ4} = I_{DQ5} = I_{DQ6} = 1$ mA.

(b) The schematic is stored in the file named Exer7_16 and it gives results that are in good agreement with the answers given for part a.

(c) and (d) Use the simulation to observe the waveforms.

Exercise 7.17

Q_1 and Q_2 form a differential amplifier with a balanced output. Q_3 and Q_4 form a differential amplifier with a single-ended output. Q_5 is a pnp common-emitter amplifier with unbypassed emitter resistance. Q_6 is an emitter follower. Q_7, Q_8, and Q_9 form a double current source.

Exercise 7.18

First we can determine $I_{C8} = I_{C7} = (15 - 0.6)/(72\ \text{k}\Omega) = 0.2$ mA. By symmetry, $I_{C1} = I_{C2} = I_{C8}/2 = 0.1$ mA. $I_{C9} = I_{C7}A_9/A_7 = 1$ mA. By symmetry, $I_{C3} = I_{C4} = I_{C9}/2 = 0.5$ mA. The voltage at the collector of Q_4 is $V_{C4} = 15 - I_{C4}(10\ \text{k}\Omega) = 10$ V. Thus we have $I_{C5} = I_{E5} = (15 - V_{C4} - 0.6)/R_5 = 1$ mA. The voltage at the collector of Q_5 is $V_{C5} = R_6I_{C5} - 15 = 0.6$ V. The output voltage is $V_o = V_{C5} - 0.6 = 0$. Finally, $I_{C6} = I_{E6} = (V_o + 15)/R_7 = 10$ mA.

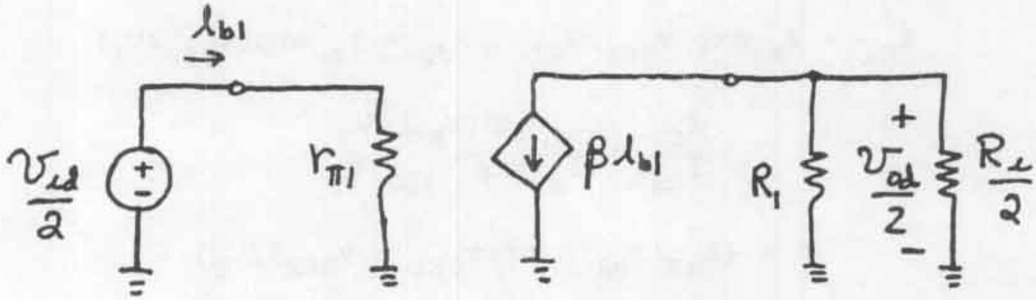
Exercise 7.19

(a) We have $r_\pi = 0.026\beta/I_{CQ}$ which yields $r_{\pi1} = r_{\pi2} = 52\ \text{k}\Omega$, $r_{\pi3} = r_{\pi4} = 10.4\ \text{k}\Omega$, $r_{\pi5} = 5.2\ \text{k}\Omega$ and $r_{\pi6} = 520\ \Omega$.

(b) $R_{i2} = r_{\pi3} + r_{\pi4} = 20.8\ \text{k}\Omega$.

(c) See Figure 7.56 in the book.

(d) For a pure differential input signal, the equivalent circuit is



$v_{id}/2 = r_{\pi 1} i_{b1}$ $\quad v_{od}/2 = -\beta i_{b1} R_L'$ $\quad$ where $R_L' = R_1 || (R_i/2)$

$A_{vd} = v_{od}/v_{id} = -\beta R_L'/r_{\pi 1}$

$R_L' = (100\ k\Omega)||[(20.8/2)\ k\Omega] = 9.42\ k\Omega$

$A_{vd} = -200(9.42)/52 = 36.23$

$A_{vdb1} = 20\log(A_{vd}) = 31.2\ dB$

Problem 7.1

Relatively high precision, capacitors, inductors, and resistors are available in wide ranges of values in discrete circuits. Furthermore, many special types of transistors and other devices are available.

In ICs, resistors and capacitors are avoided if possible. Inductors are not practical in integrated circuits. The range of device types available for a given circuit design is much more limited.

Problem 7.2

The variety of devices available to the IC designer is limited by the complexity of the fabrication process and the need to minimize chip area. Active device characteristics are tailored to a given application by selection of device dimensions.

Problem 7.3

An advantage of integrated devices is good matching.

Problem 7.4

$$I_{C1} = I_{s1}\exp(v_{BE1}/V_T) \quad I_{C2} = I_{s2}\exp(v_{BE2}/V_T)$$

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{s1}\exp(v_{BE1}/V_T)}{I_{s2}\exp(v_{BE2}/V_T)}$$

$$1 = (I_{s1}/I_{s2})\exp[(v_{BE1} - v_{BE2})/V_T]$$

$$v_{BE1} - v_{BE2} = V_T\ln(I_{s2}/I_{s1})$$

$$= 0.026\ln(0.952) = -1.27 \text{ mV}$$

Problem 7.5

$$R_{max} = (10 \text{ k}\Omega) \times 1.2 \times 0.98 = 11.76 \text{ k}\Omega$$

$$R_{min} = (10 \text{ k}\Omega) \times 1.2 \times 1.02 = 12.24 \text{ k}\Omega$$

Problem 7.6

$$I_{DQ} = \left(\frac{W}{L}\right)\frac{KP}{2}(V_{GSQ} - V_{to})^2(1 + \lambda V_{DSQ})$$

Therefore if W/L varies by ±5%, I_{DQ} varies by ±5%.

Problem 7.7

1. V_{CEQ} and I_{CQ} must be large enough so clipping does not occur.

2. Device limits for V_{CE}, I_C, and power dissipation must not be exceeded.

3. Desired impedance levels for the circuit must be considered.

4. The desired frequency response must be considered.

Problem 7.8

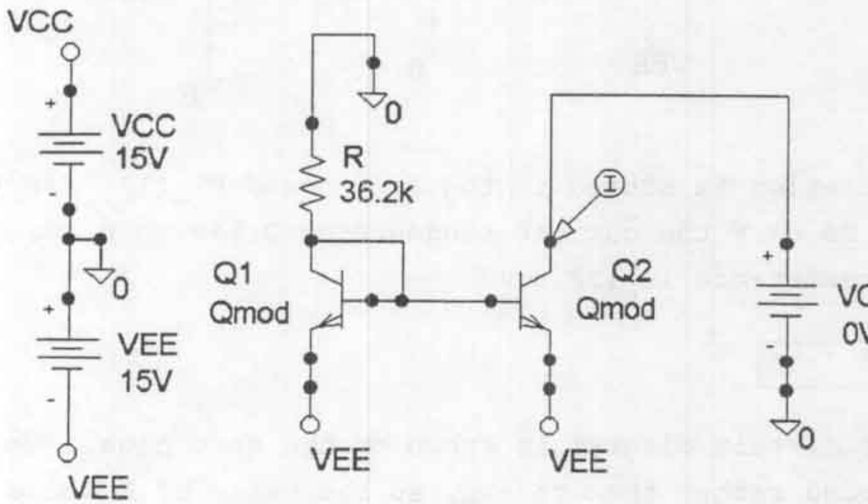
The current mirror is shown in Figure 7.1a on page 415 in the book, the Wilson current source is shown in Figure 7.10 on page 422 in the book, and the Widlar source is shown in Figure 7.11 (page 422). The Wilson source is used to attain high output impedance, and the Widlar source is used to attain small current values.

Problem 7.9

A current sink draws current from the load, whereas the current sink delivers current to the load.

Problem 7.10

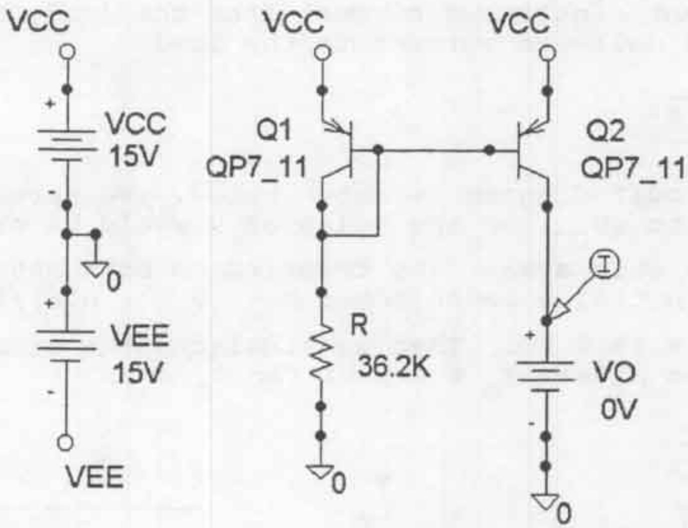
The circuit diagram is shown below. We returned R to ground rather than to $+V_{CC}$, so the value of R would be smaller and require less chip area. The transistors both have relative areas of unity. Initially we selected $R = (V_{EE} - 0.6)/I_{ref} = (14.4\ \text{V})/(0.5\ \text{mA}) = 28.8\ \text{k}\Omega$. Then we simulated the circuit and adjusted R to attain $I_O \cong 0.5$ mA for $V_O = 0$.



The simulation is stored in the file named P7_10. For V_O ranging from -5 to +5 V the current ranges from 0.462 to 0.540 mA. The output resistance is 128.5 kΩ.

Problem 7.11

The circuit diagram is shown below. We returned R to ground rather than to $+V_{CC}$ so the value of R would be smaller and require less chip area. The transistors both have relative areas of unity. Initially we selected $R = (V_{EE} - 0.6)/I_{ref} = (14.4\ V)/(0.5\ mA) = 28.8\ k\Omega$. Then we simulated the circuit and adjusted R to attain $I_O \cong 0.5$ mA for $V_O = 0$.

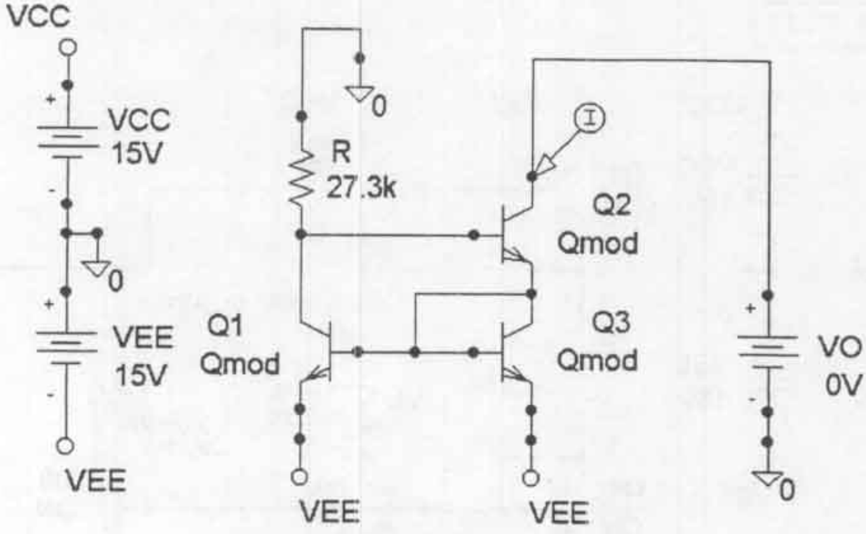


The simulation is stored in the file named P7_11. For V_O ranging from -5 to +5 V the current ranges from 0.540 to 0.462 mA. The output resistance is 128.5 kΩ.

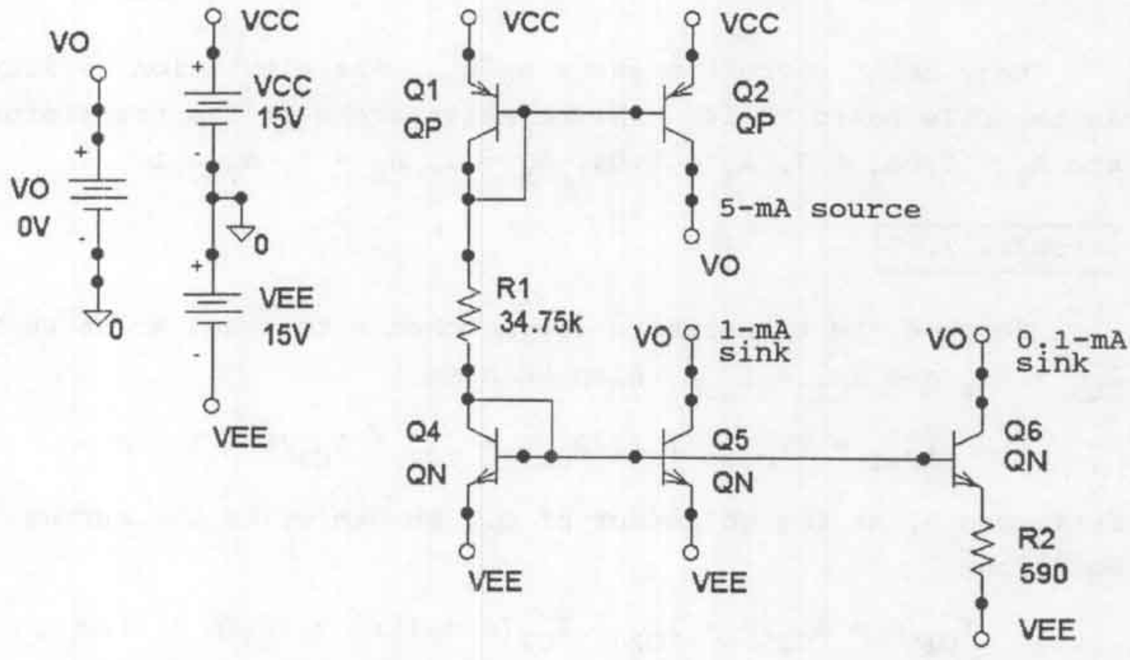
Problem 7.12

The circuit diagram is shown on the next page. We returned R to ground rather than to $+V_{CC}$ so the value of R would be smaller and require less chip area. The transistors all have relative areas of unity. Initially we selected $R = (V_{EE} - 1.2)/I_{ref} = (13.8\ V)/(0.5\ mA) = 27.6\ k\Omega$. Then we simulated the circuit and adjusted R to attain $I_O \cong 0.5$ mA for $V_O = 0$.

The simulation is stored in the file named P7_12. For V_O ranging from -5 to +5 V the current ranges from 0.49807 to 0.49948 mA. The output resistance is 7.12 MΩ.

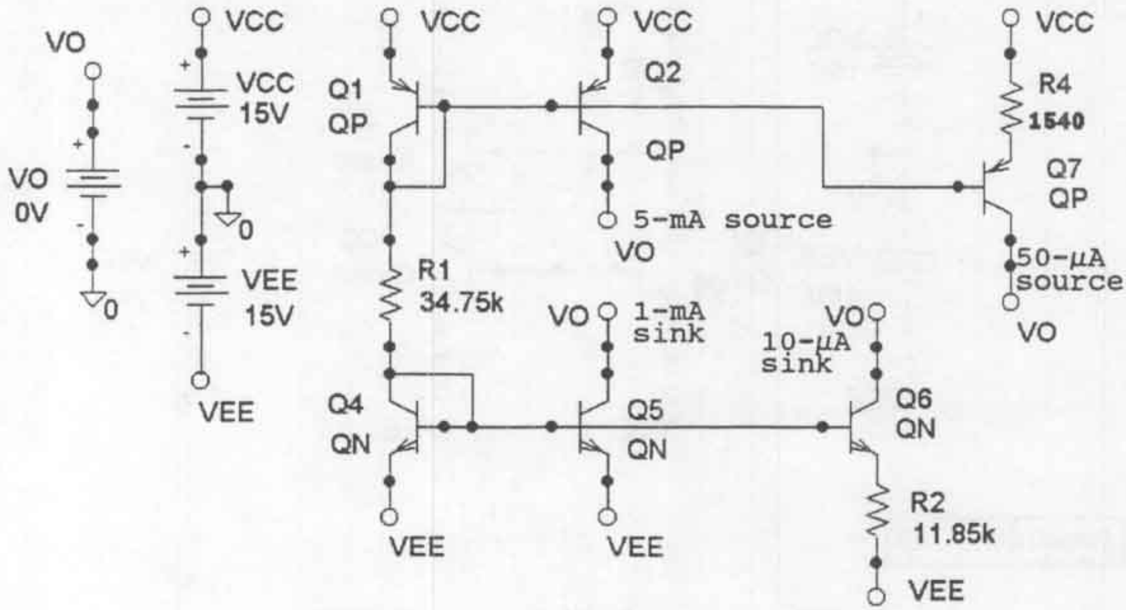


Problem 7.13



Many other correct answers exist. The simulation is stored in the file named P7_13. The relative areas of the transistors are $A_1 = 1$, $A_2 = 5$, $A_4 = 1.04$, $A_5 = 1$, $A_6 = 1$.

Problem 7.14



Many other correct answers exist. The simulation is stored in the file named P7_14. The relative areas of the transistors are $A_1 = 1$, $A_2 = 5$, $A_4 = 1.04$, $A_5 = 1$, $A_6 = 1$, $A_7 = 1$.

Problem 7.15

Because the transistors are matched with equal areas we have $I_{C3} = I_{C4}$ and $I_{C1} = I_{C2}$. Also we have

$$I_{ref} = (V_{CC} - 1.2)/R_{ref} = I_{C1} + I_{C3}/\beta + I_{C4}/\beta$$

Furthermore, at the collector of Q_2, we can write the current equation

$$I_{C1}/\beta + I_{C2}/\beta + I_{C2} = I_{C3}(\beta + 1)/\beta + I_{C4}(\beta + 1)/\beta$$

From these equations, we eventually have

$$I_{C3} = I_{C4} = \frac{\beta^2 + 2\beta}{2(\beta^2 + 2\beta + 2)} \times \frac{V_{CC} - 1.2}{R_{ref}} \cong I_{ref}/2$$

Problem 7.16

Because the transistors are matched with equal areas except Q_2 which has an area of 2, we have $I_{C4} = 2I_{C3}$ and $I_{C1} = I_{C2}$. Also we have

$$I_{ref} = (V_{CC} - 1.2)/R_{ref} = I_{C1} + I_{C3}/\beta + I_{C4}/\beta$$

Furthermore at the collector of Q_2, we can write the current equation

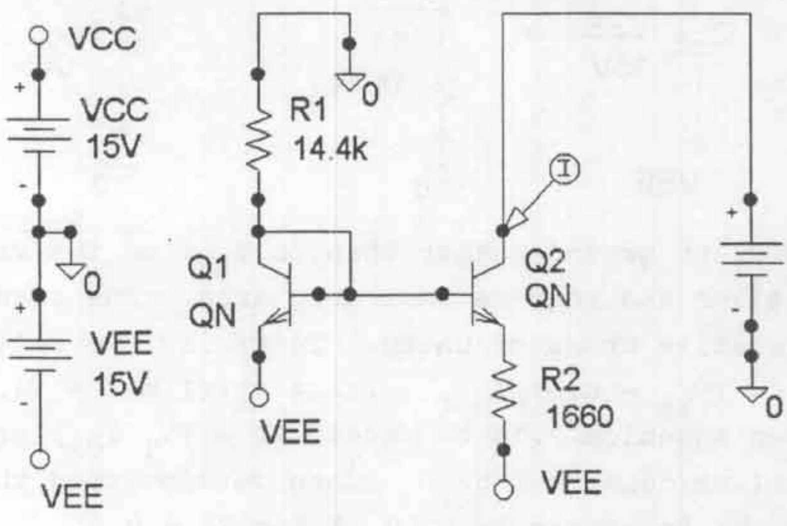
$$I_{C1}/\beta + I_{C2}/\beta + I_{C2} = I_{C3}(\beta + 1)/\beta + I_{C4}(\beta + 1)/\beta$$

From these equations we eventually have

$$I_{C3} = I_{C4}/2 = \frac{\beta^2 + 2\beta}{3\beta^2 + 6\beta + 6} \times \frac{V_{CC} - 1.2}{R_{ref}} \cong I_{ref}/3$$

Problem 7.17

Many correct answers exist. One is shown below.



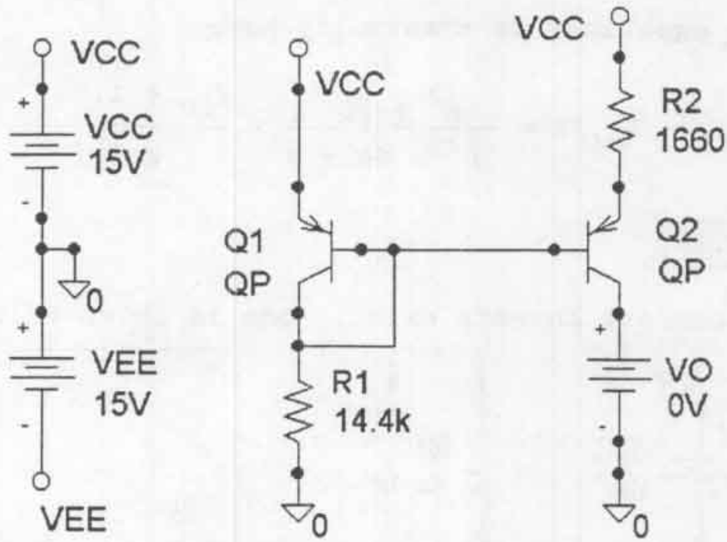
We returned R_1 to ground rather than to $+V_{CC}$, so the value of R_1 would be smaller and require less chip area. The transistors both have relative areas of unity. Initially, we selected I_{ref} = 1 mA and $R_1 = (V_{EE} - 0.6)/I_{ref}$ = (14.4 V)/(1 mA) = 14.4 kΩ.

Also, we used Equation 7.16 to obtain $R_2 = (V_T/I_{C2})\ln(I_{C1}/I_{C2})$ = (26mV/50μA)ln(1mA/50μA) = 1557 Ω. Then we simulated the circuit and adjusted R_2 to attain $I_O \cong 50$ μA for $V_O = 0$.

The simulation is stored in the file named P7_17. For V_O ranging from -5 to +5 V, the current ranges from 49.0 to 50.9 μA. The output resistance is 5.31 MΩ.

Problem 7.18

Here is one correct answer:

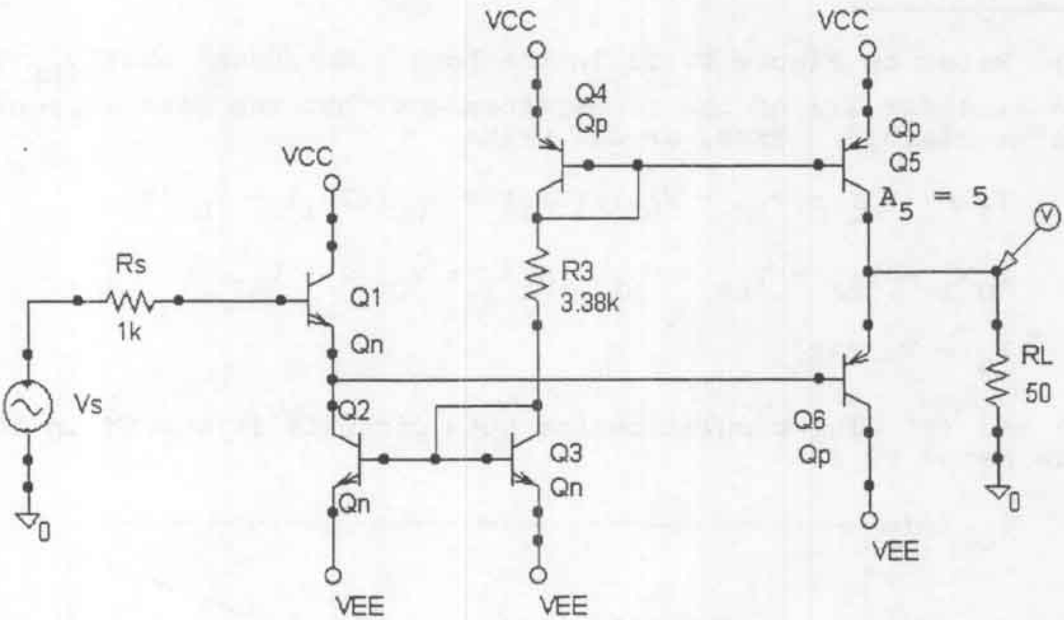


We returned R_1 to ground rather than to V_{EE}, so the value of R_1 would be smaller and require less chip area. The transistors both have relative areas of unity. Initially, we selected I_{ref} = 1 mA and $R_1 = (V_{EE} - 0.6)/I_{ref}$ = (14.4 V)/(1 mA) = 14.4 kΩ. Also, we used Equation 7.16 to obtain $R_2 = (V_T/I_{C2})\ln(I_{C1}/I_{C2})$ = 26mV/50μA)ln(1mA/50μA) = 1557 Ω. Then we simulated the circuit and adjusted R_2 to attain $I_O \cong 50$ μA for $V_O = 0$.

The simulation is stored in the file named P7_18. For V_O ranging from -5 to +5 V the current ranges from 50.9 to 49.0 μA. The output resistance is 5.31 MΩ.

Problem 7.19

The circuit diagram is shown below. Q_1 and Q_6 are the emitter followers. The other transistors form the current sources. With maximum output, the load current is 10 mA. Unless I_{CQ6} is larger than 10 mA, clipping due to cutoff will occur. Thus, we have chosen $I_{CQ6} \cong 13$ mA to ensure some design margin. We also want high input impedance and low power supply drain. Thus, we have biased Q_1 at a lower current. Furthermore, we want $v_O = 0$ for $v_s = 0$. Thus, we initially chose $A_1 = 1$, $A_6 = 5$ and $I_{C1} \cong I_{C6}/5$, because these choices result in $V_{BE1} \cong -V_{BE6}$ and the output voltage will be close to zero for zero input. Finally, we simulated the circuit and adjusted the values to attain a relatively undistorted output and close to zero dc offset.



Problem 7.20

$$I_{ref} = (V_{CC} - 0.6)/R = 1.44 \text{ mA}$$

$$I_{C2min} = \frac{I_{ref}}{1 + 2/\beta} = \frac{1.44}{1 + 2/100} = 1.4117$$

$$I_{C2max} = \frac{I_{ref}}{1 + 2/\beta} = \frac{1.44}{1 + 2/200} = 1.4257$$

Thus the percentage increase in I_{C2} is

$$\frac{I_{C2max} - I_{C2min}}{I_{C2min}} \times 100\% = 0.995\%$$

Problem 7.21

Because we have $I_{C2} \cong (A_2/A_1)I_{ref}$, I_{C2} will vary by ±5% if A_2 varies by ±5%.

Problem 7.22

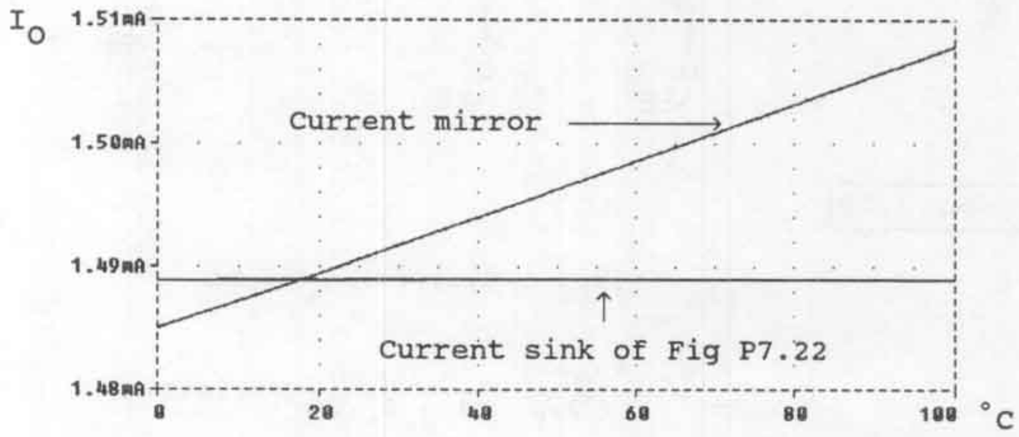
(a) Refer to Figure P7.22 in the book. We assume that V_{BE} is the same for all of the transistors and that the base currents are negligible. Thus, we can write

$$I_1 = (V_{CC} - V_{BE} - V_{BE})/(2R_1) = V_{CC}/(2R_1) - V_{BE}/R_1$$

$$I_O R_1 + V_{BE} = V_{BE} + V_{BE} + R_1 I_1 = V_{CC}/2 + V_{BE}$$

$$I_O = V_{CC}/2R_1$$

(b) and (c) The simulation for both circuits is stored in the file named P7_22.



Problem 7.23

For I_O to remain constant, V_O must be large enough so Q_3 operates in the active region. Thus, we must have $V_{CE3} > 0.2$. However, using the result of Problem 7.22, we have $I_O = V_{CC}/2R_1 = 1.5$ mA. Then we have $V_{CE3} = V_O - I_O R_1 = V_O - 7.5 > 0.2$. Thus, the compliance range is $V_O > 7.7$ V.

Problem 7.24

(a) $I_1 = (V_{CC} - 2V_{BE})/R_1$

$$I_{C3} = I_{C1} = I_1 - I_{B2}$$

$$= I_1 - I_{E2}/(\beta + 1)$$

$$= I_1 - (I_{B1} + I_{B3})/(\beta + 1)$$

$$= I_1 - 2I_{C3}/[\beta(\beta + 1)]$$

$$I_{C3} = \frac{(V_{CC} - 2V_{BE})\beta(\beta + 1)}{R_1(\beta^2 + \beta + 2)}$$

(b) Evaluating we have

β	I_{C3} (mA)
100	0.453244
110	0.453259

Percentage increase = 0.0033%

(c) For the current mirror of Figure 7.1 we have $I_{ref} = (V_{CC} - V_{BE})/R$ and $I_{C2} = I_{ref}/(1 + 2/\beta)$. Evaluating we have

β	I_{C2} (mA)
100	0.467320
110	0.468154

Percentage increase = 0.178%

(d) The compliance range is $V_O > 0.2$ V.

Problem 7.25

$$I_{C2} = I_{C1} = I_{C3} = I_{C4} = I_{C5} = \frac{V_{CC} - V_{BE}}{2(9.3\ k\Omega)} = 0.5\ mA$$

$$V_O = I_{C2} \times (10\ k\Omega) = 5\ V$$

Problem 7.26

$$I_{C1} = I_{C2} = I_{C3} = (V_{CC} - 2V_{BE})/(13.6\ k\Omega) = 1\ mA$$

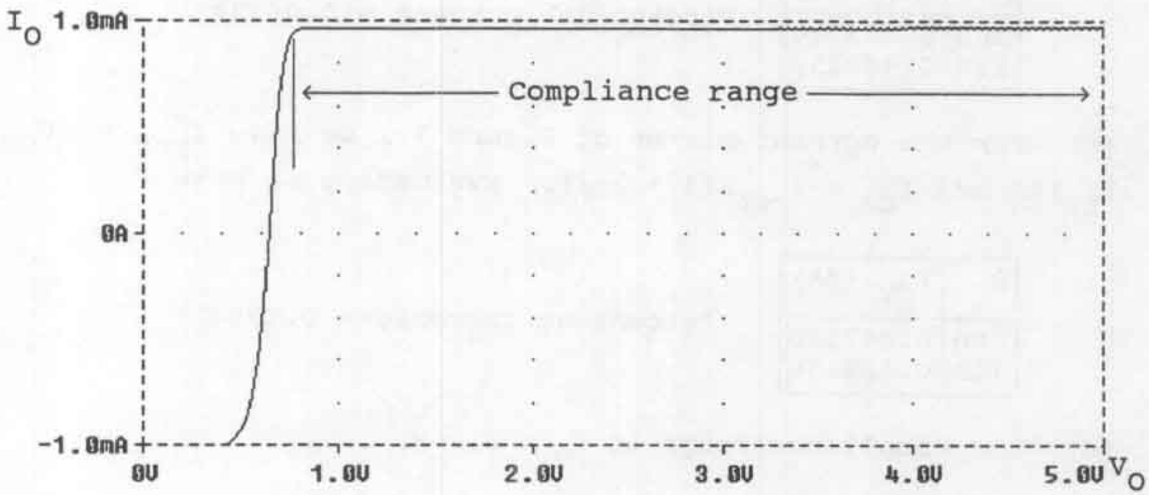
Q_1 Q_2 and Q_3 operate in the active region. However Q_4 is in saturation. $I_{C4} = I_{C2} = 1$ mA. $V_O \cong 0.2$ V.

Problem 7.27

Refer to Figure P7.27 in the book. Writing a voltage equation we obtain

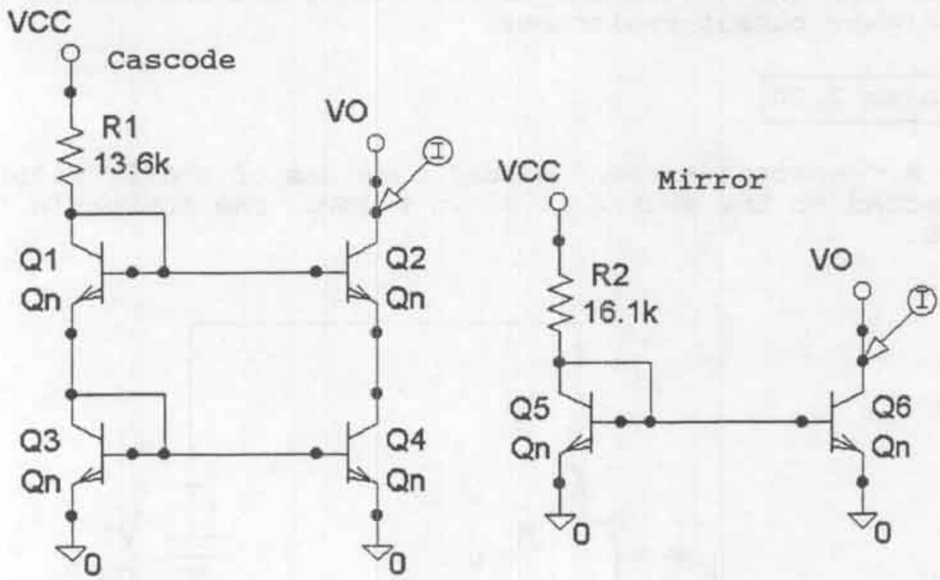
$$V_{BE2} + V_{CE4} = V_{BE1} + V_{BE3}$$

However we assume that $V_{BE1} = V_{BE2} = V_{BE3} = 0.7$ V. Thus we have $V_{CE4} = 0.7$ V. Also we have $V_{CE2} = V_O - V_{CE4}$. For operation in the compliance range, we must have $V_{CE2} > 0.2$ V, which implies $V_O > 0.9$ V. Also, $I_{C1} = I_{C2} = I_{C3} = I_{C4} = I_O = (V_{CC} - 2V_{BE})/(13.6\ k\Omega) = 1$ mA. The simulation is stored in the file named P7_27. The plot of I_O versus V_O is

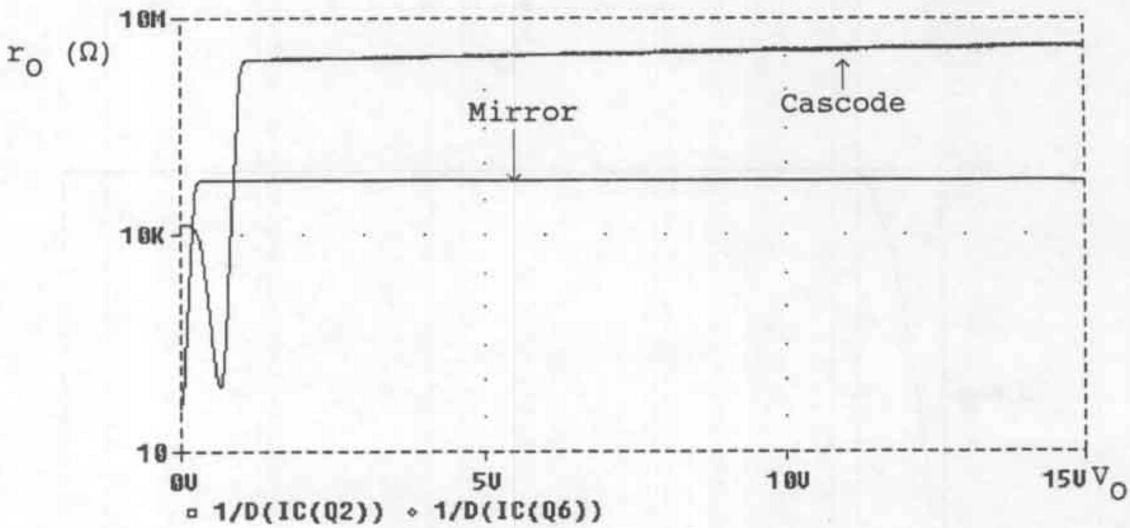


Problem 7.28

The circuit diagram is



The simulation is in the file named P7_27. It is necessary to use the **Analysis/Setup/Options** menu to set RELTOL = 1E-7 to obtain smooth plots of r_o.



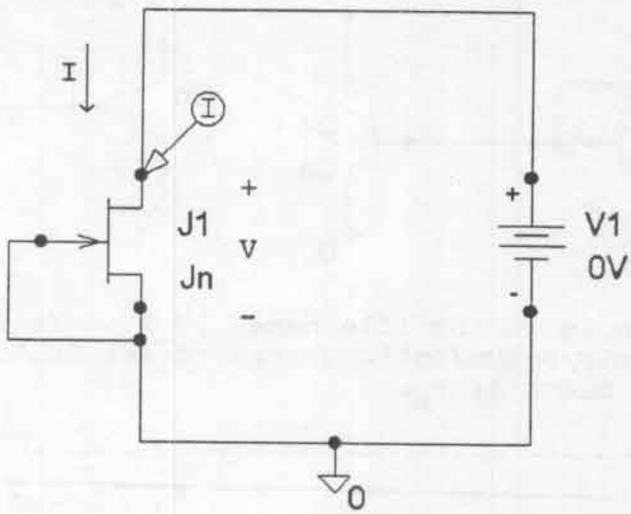
Notice that the output resistance of the cascode current source is much higher than that of the simple mirror.

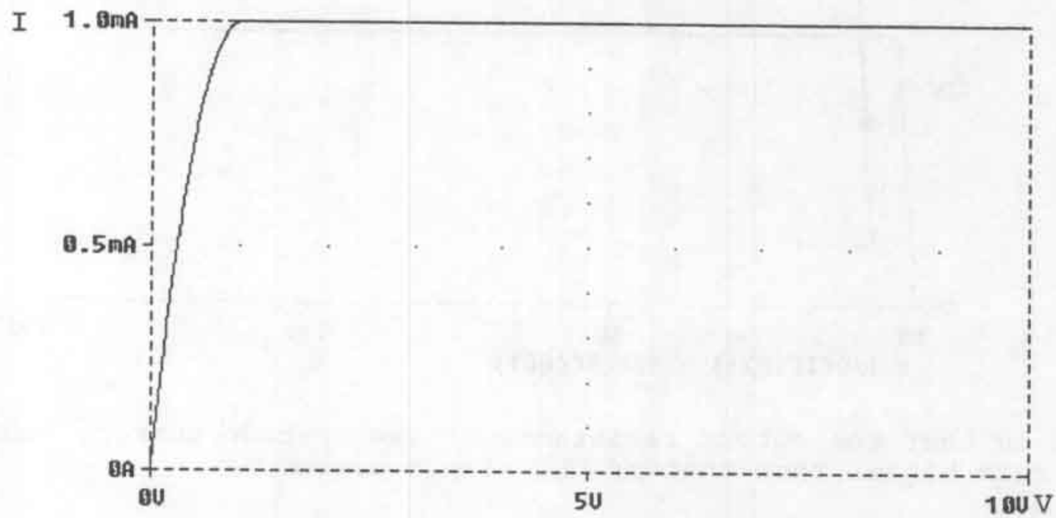
Problem 7.29

See Figures 7.15 and 7.16 in the book. In general the mirror has the larger compliance range, and the Wilson source has the higher output resistance.

Problem 7.30

A "constant-current diode" consists of a JFET with the gate connected to the source as shown below. The Schematic file is P7_30.





Problem 7.31

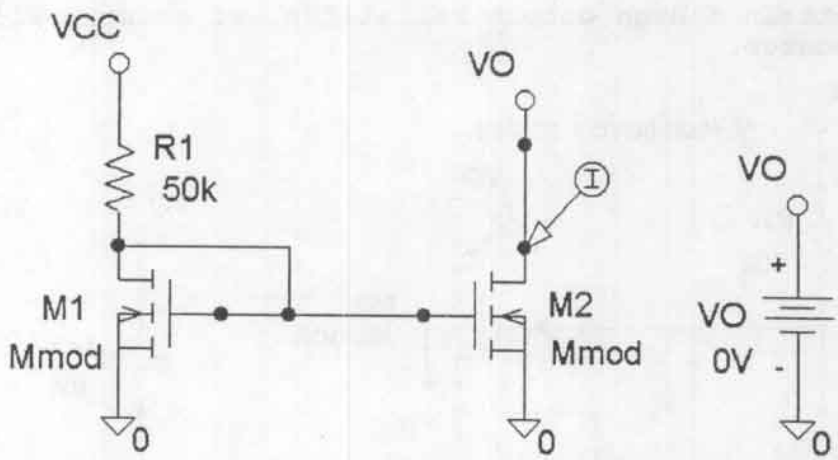
(a) $$i_{D3} = \frac{(W_3/L_3)}{(W_1/L_1)} \times i_{D1} = 3 \times 0.5 \text{ mA} = 1.5 \text{ mA}$$

$$i_{D2} = \frac{(W_2/L_2)}{(W_1/L_1)} \times i_{D1} = 2 \times 0.5 \text{ mA} = 1 \text{ mA}$$

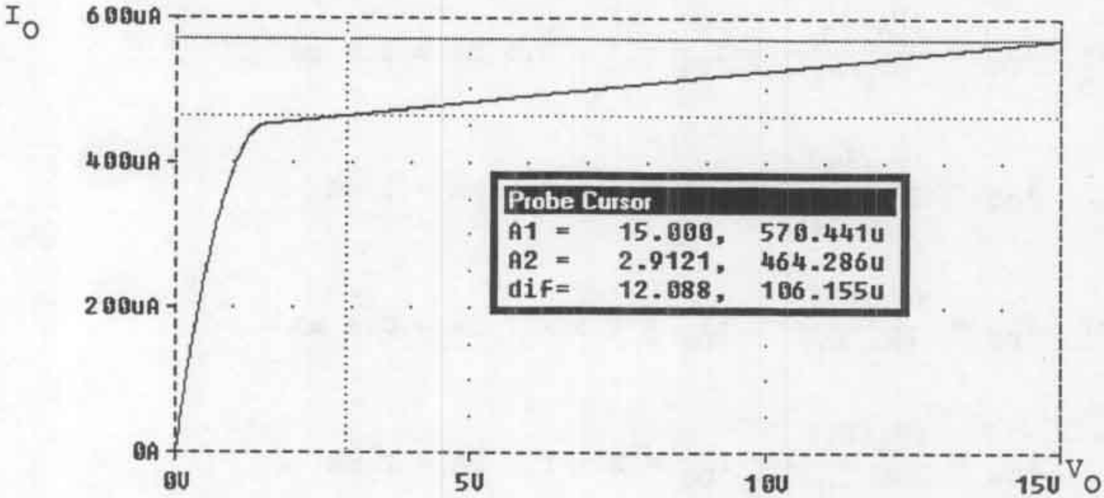
(b) $$i_{D5} = \frac{(W_5/L_5)}{(W_1/L_1)} \times i_{D4} = 0.5 \times 1 \text{ mA} = 0.5 \text{ mA}$$

$$i_{D6} = \frac{(W_6/L_6)}{(W_1/L_1)} \times i_{D4} = 2 \times 1.0 \text{ mA} = 2 \text{ mA}$$

Problem 7.32

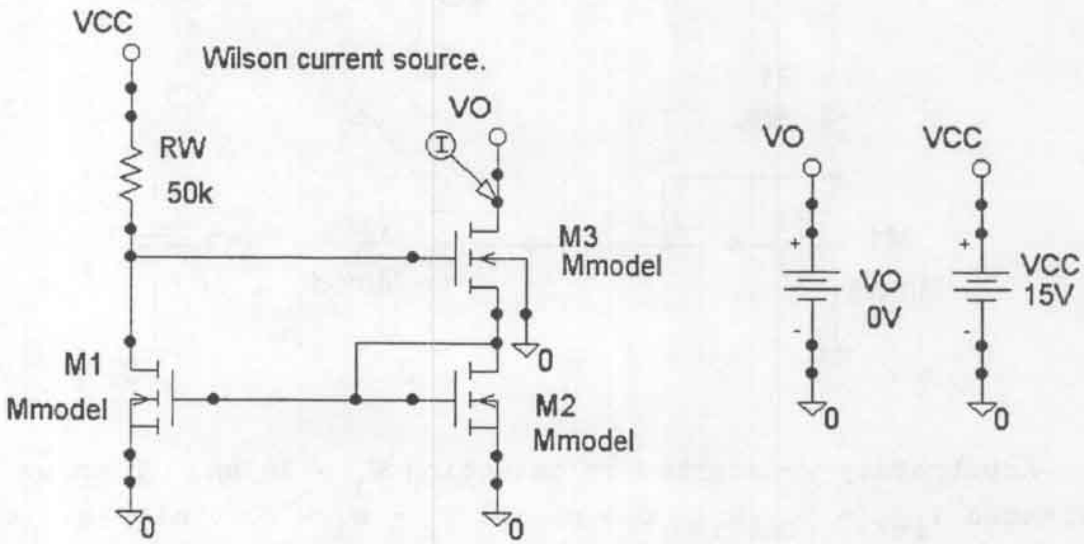


Arbitrarily we started by selecting W_1 = 20 μm. Then we estimated $I_{ref} = V_{CC}/R_1$ = 0.3 mA and $W_2 = W_1 \times$ (0.5 mA)/(0.3 mA) = 33.3 μm. Next we simulated the circuit and adjusted W_2 to attain I_O = 0.5 mA in the center of the compliance range. The plot of I_O versus V_O is shown on the next page. The compliance range extends from about 1.5 to 15 V. (If desired, the widths of the transistors could be reduced to save space. This would raise the lower end of the compliance range.) Using the cursor we found two points on the plot and computed the output resistance to be 114 kΩ.



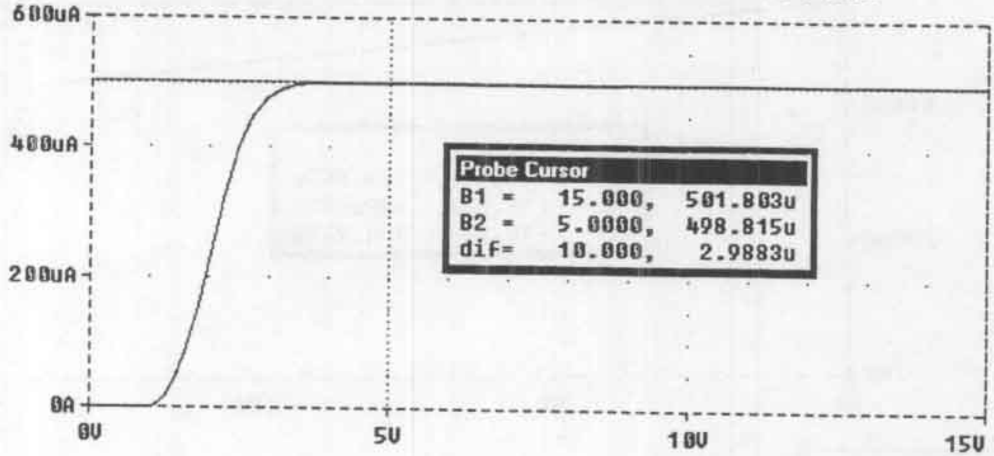
Problem 7.33

To attain a high output resistance, we chose a Wilson current source.

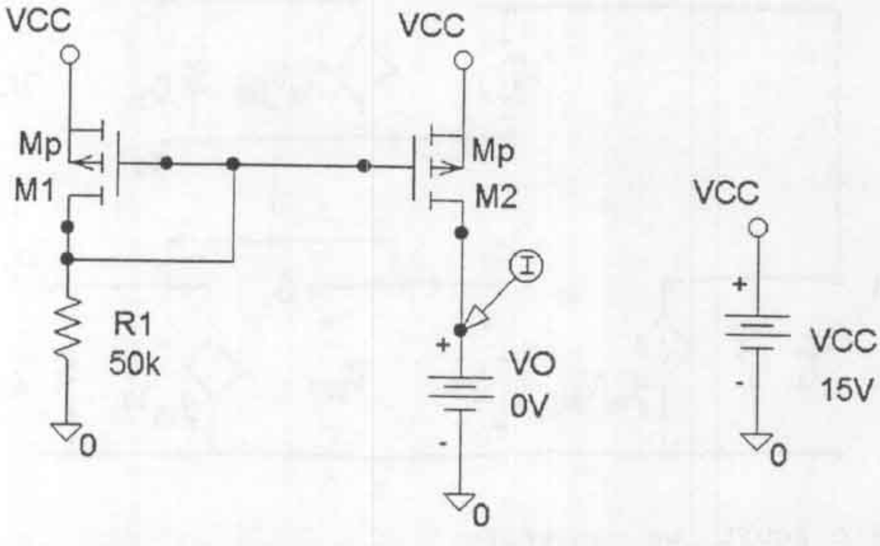


Arbitrarily, we started by selecting W_1 = 20 μm. Then we estimated $I_{ref} = V_{CC}/R_1$ = 0.3 mA and $W_2 = W_1 \times$ (0.5 mA)/(0.3 mA) = 33.3 μm. Next we simulated the circuit and adjusted W_2 to attain I_O = 0.5 mA in the center of the compliance range. This required W_2 = 50 μm. We selected $W_3 = W_2$. The plot of I_O versus

V_O is shown below. The compliance range extends from about 3.0 to 15 V. (If desired, the widths of the transistors could be reduced to save space. This would raise the lower end of the compliance range.) Using the cursor we found two points on the plot and computed the output resistance to be 3.34 MΩ.

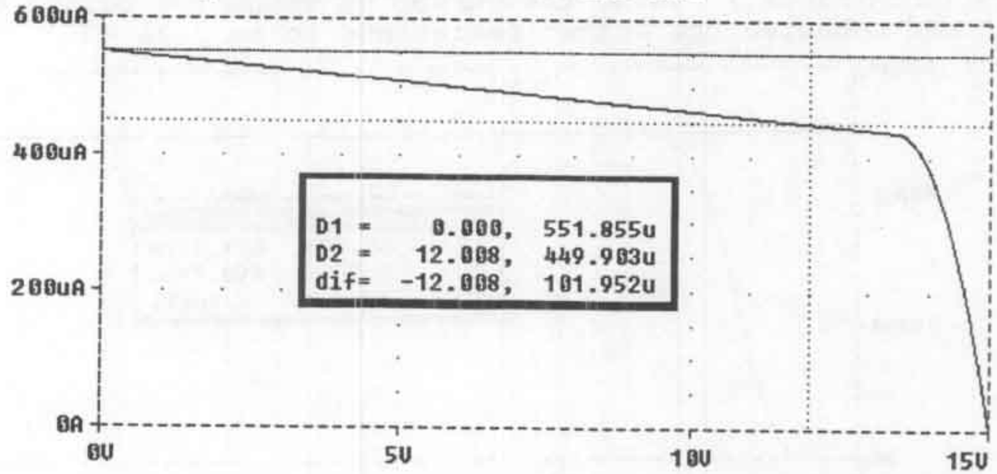


Problem 7.34

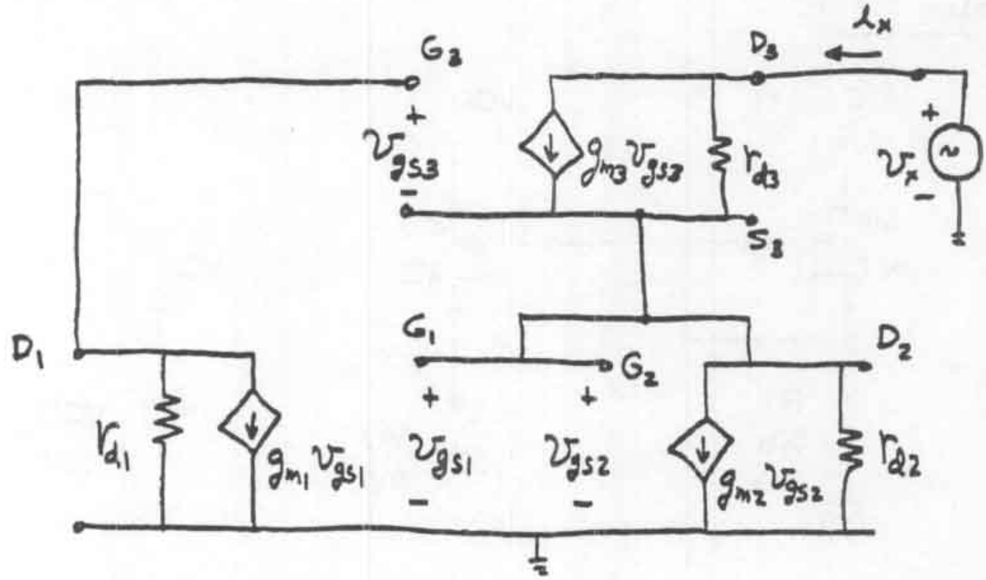


Arbitrarily, we started by selecting W_1 = 40 μm. Then we estimated $I_{ref} = V_{CC}/R_1$ = 0.3 mA and $W_2 = W_1 \times$ (0.5 mA)/(0.3 mA) = 66.6 μm. Next we simulated the circuit and adjusted W_2 to attain I_O = 0.5 mA in the center of the compliance range, settling on W_2 = 71.6 μm. The plot of I_O versus V_O is shown on the next page. The compliance range extends from about 0 to 13.5

V. (If desired, the widths of the transistors could be reduced to save space. This would lower the upper end of the compliance range.) Using the cursor we found two points on the plot and computed the output resistance to be 118 kΩ.



Problem 7.35



From the circuit, we can write

$$v_{gs3} = -(g_{m1}r_{d1} + 1)v_{gs1}$$

$$i_x = (v_x - v_{gs1})/r_{d3} + g_{m3}v_{gs3}$$

$$i_x = (g_{m2} + 1/r_{d2})v_{gs1}$$

Algebra eventually results in:

$$r_o = \frac{v_x}{i_x} = r_{d3}\left(1 + \frac{g_{m3}g_{m1}r_{d1} + g_{m3} + 1/r_{d3}}{g_{m2} + 1/r_{d2}}\right)$$

Problem 7.36

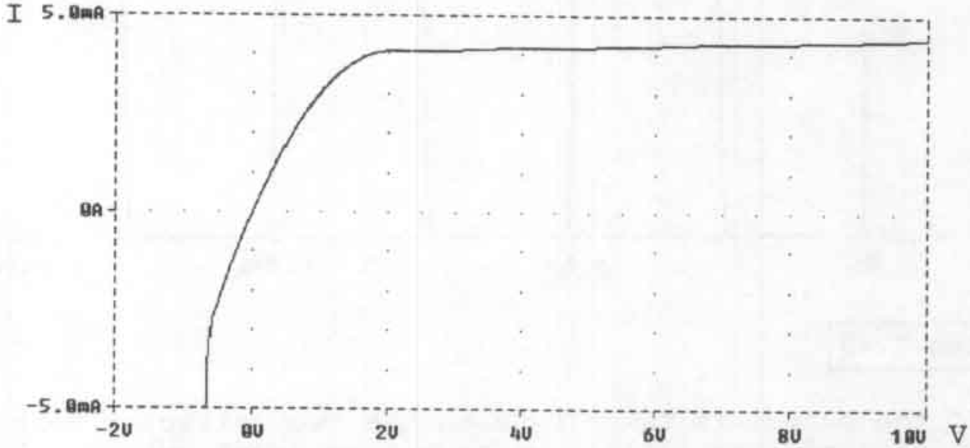
For M_1 we have $I_{D1} = \left(\frac{W_1}{L_1}\right)\frac{KP}{2}(V_{GS1} - V_{to})^2$ substituting values and solving for V_{GS1} we obtain V_{GS1} = 3 V. Then we have R = (10 - 3)/(1 mA) = 7 kΩ. Finally $I_2 = I_{D1}(W_2/W_1)$ = 0.5 mA, and $I_3 = I_{D1}(W_3/W_1)$ = 2 mA.

Problem 7.37

For M_1 we have $I_{D1} = \left(\frac{W_1}{L_1}\right)\frac{KP_p}{2}(V_{GS1} - V_{top})^2$ substituting values and solving for V_{GS1} we obtain V_{GS1} = -5 V. Similarly we obtain V_{GS3} = 5 V. Then we have R = (15 + $V_{GS1} - V_{GS3}$)/(1 mA) = 5 kΩ. Finally $I_2 = I_{D1}(W_2/W_1)$ = 1 mA, and $I_3 = I_{D1}(W_3/W_1)$ = 2 mA.

Problem 7.38

The simulation is stored in the file named P7_38.



Problem 7.39

Ideally a differential amplifier produces an output that is proportional to the differential signal and does not depend on the common-mode signal.

Problem 7.40

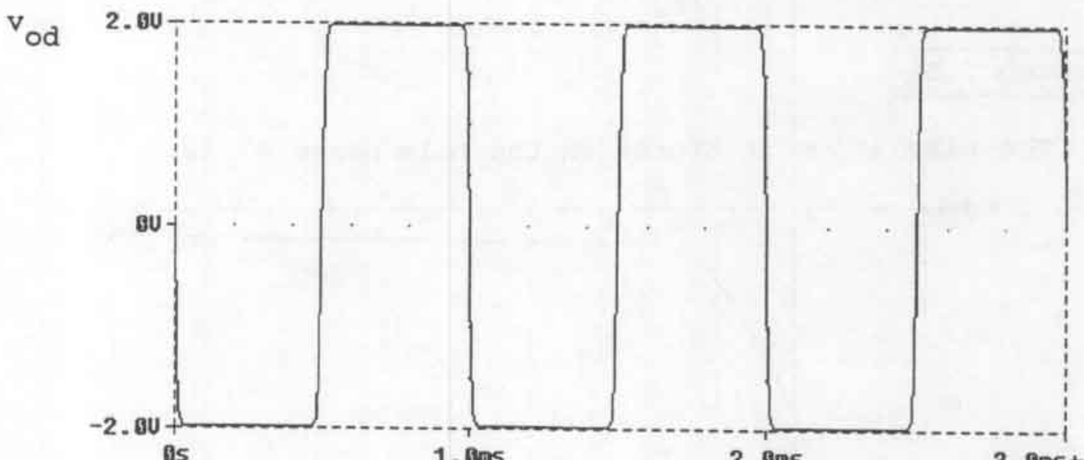
The transfer characteristic of the BJT differential amplifier is shown in Figure 7.26 on page 439 in the book. It is approximately linear for $-V_T \le v_{id} \le V_T$.

Problem 7.41

The sketch is similar to Figure 7.26 (page 439) in which the maximum value of $v_{od} = \alpha R_C I_{EE} \cong 2$ V and the minimum value of $v_{od} \cong -2$ V.

Problem 7.42

For a 1-V peak input signal, the output will display pronounced clipping. Thus the output will be a 1-kHz square wave with rounded edges. A simulation of the circuit is stored in the file named P7_42.



Problem 7.43

If the output is taken between the two collector terminals of a differential amplifier, we have a balanced output. If the output is taken from just one of the collectors, we have a single-ended output.

Problem 7.44

See Figure 7.30 on page 741 in the book.

Problem 7.45

Using Equation 7.40, we have

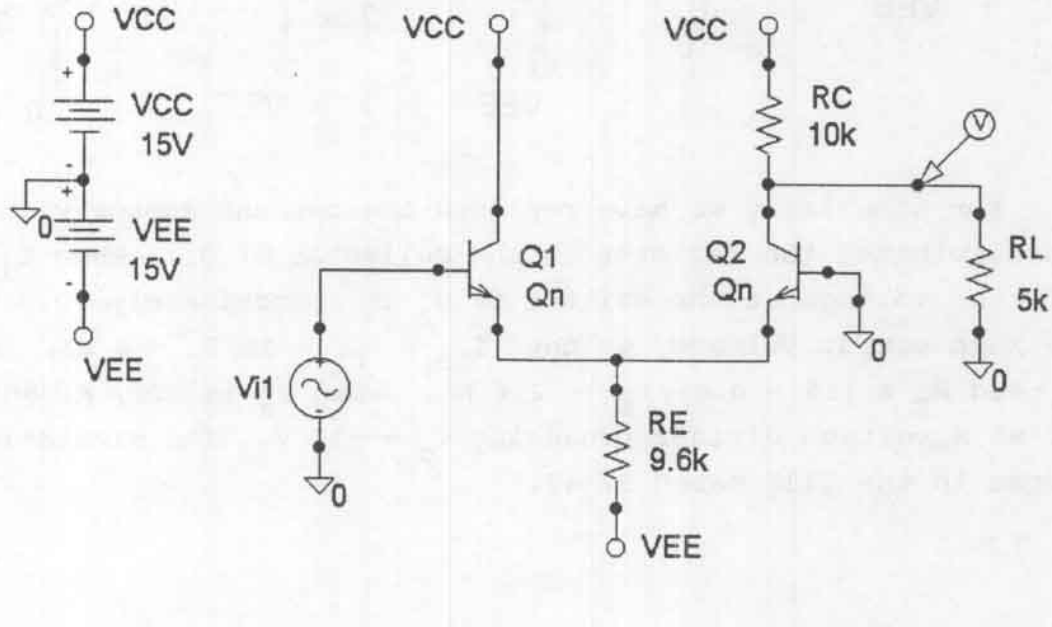
$$\frac{i_{C1}}{i_{C2}} = \exp\left(\frac{v_{id}}{V_T}\right) \quad \Rightarrow \quad v_{id} = V_T \ln(i_{C1}/i_{C2})$$

At a temperature of 300 K we have $V_T \cong 26$ mV. For 90% of the current through Q_1, we have $i_{C1}/i_{C2} = 9$.

Percentage	v_{id}
90%	57.1 mV
99%	119 mV

Problem 7.46

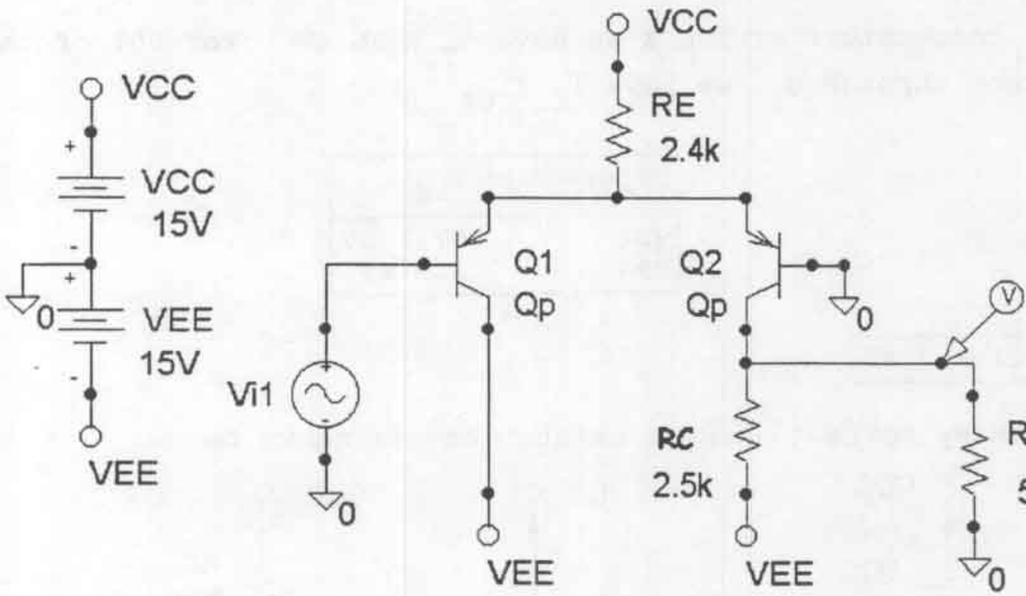
Many correct answers exist. One is shown below.



For simplicity we have replaced the current source with R_E and eliminated the resistor in the collector of Q_1. When Q_1 is off, the voltage at the emitter of Q_2 is approximately -0.6 V. For zero output voltage we need $I_{E2} \cong I_{C2} = 15/R_C = 1.5$ mA. Thus we need $R_E \cong (15 - 0.6)/I_{E2} = 9.6$ kΩ. When Q_2 is off, R_C and R_L act as a voltage divider producing $v_o = 5$ V. The simulation is stored in the file named P7_46.

Problem 7.47

Many correct answers exist. One is shown below.



For simplicity we have replaced the current source with R_E and eliminated the resistor in the collector of Q_1. When Q_1 is off, the voltage at the emitter of Q_2 is approximately +0.6 V. For zero output voltage, we need $I_{E2} \cong I_{C2} = 15/R_C = 6$ mA. Thus we need $R_E \cong (15 - 0.6)/I_{E2} = 2.4$ kΩ. When Q_2 is off, R_C and R_L act as a voltage divider producing $v_o = -10$ V. The simulation is stored in the file named P7_47.

Problem 7.48

In a small-signal equivalent circuit, an ideal dc voltage source is replaced with a short circuit because there is no change in the source voltage even if the current through it is changing. An ideal dc current source is replaced with an open circuit because there is no change in the source current even if the voltage across it changes.

Problem 7.49

By symmetry, we conclude that $I_{CQ1} = I_{CQ2} = 5$ mA. Then we have $r_{\pi 1} = r_{\pi 2} = \beta V_T / I_{CQ} = 1040\ \Omega$. Also the differential input voltage is $v_d = v_{in}$. From Table 7.2 on page 450 in the book, we have

$$A_{vds} = \frac{v_{o2}}{v_d} = \frac{v_o}{v_{in}} = \frac{R_C \beta}{2[r_\pi + (\beta + 1)R_{EF}]}$$

$$= \frac{1000 \times 200}{2[1040 + 201 \times 20]} = 19.8$$

$$R_i = R_{id} = 2[r_\pi + (\beta + 1)R_{EF}] = 10.1\ \text{k}\Omega$$

Problem 7.50

Because the 1-mA sources become open circuits in the equivalent circuit, the common-mode gain is zero, and the common-mode input impedance is infinite. Thus we can compute the input impedance and gain using the formulas for the differential signal.

Comparing Figure P7.50 to the equivalent circuit shown in Figure 7.33, we have $R_{EB} = \infty$ and $2R_{EF} = 100$. Thus $R_{EF} = 50$.

$$I_{CQ1} = I_{CQ2} = 1\ \text{mA}$$

$$r_\pi = \beta V_T / I_{CQ} = 5.2\ \text{k}\Omega$$

$$A_{vds} = \frac{v_o}{v_{in}} = \frac{v_o}{v_d} = \frac{R_C \beta}{2[r_\pi + (\beta + 1)R_{EF}]}$$

$$A_{vds} = \frac{10^4 \times 200}{2(5200 + 201 \times 50)} = 65.6$$

$$R_i = R_{id} = 2[r_\pi + (\beta + 1)R_{EF}] = 30.5\ k\Omega$$

Problem 7.51

(a) $I_{CQ1} = I_{CQ2} = (5\ mA)\beta/(\beta + 1) = 4.975\ mA$

$$r_\pi = \beta V_T/I_{CQ} = 1045\ k\Omega$$

$$A_{vds} = \frac{v_o}{v_{in}} = \frac{v_o}{v_d} = = \frac{R_C\beta}{2[r_\pi + (\beta + 1)R_{EF}]}$$

$$A_{vds} = \frac{1000 \times 200}{2(1045 + 201 \times 0)} = 95.7$$

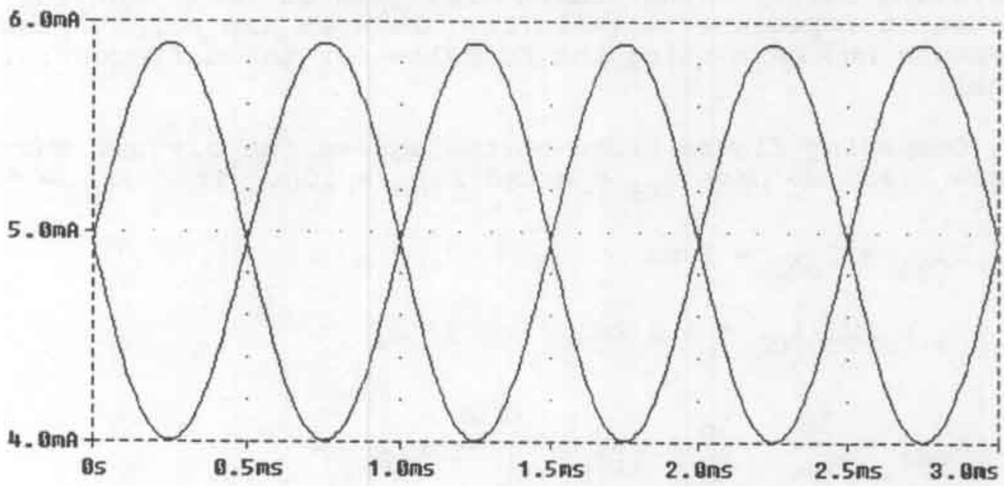
(b) and (c)

v_{i1} is a 1-kHz sine wave with peak amplitude of 10 mV.

$$i_{C1} = I_{CQ} + A_{vds}v_{i1}/R_C = 4.975 + 0.957\sin(2000\pi t)$$

$$i_{C2} = I_{CQ} - A_{vds}v_{i1}/R_C = 4.975 - 0.957\sin(2000\pi t)$$

The simulation is stored in the file named P7_51. The simulation yields the following plots of the currents.



$$v_{o1} = V_{CC} - I_{CQ1}R_C - A_{vds}v_{i1} = 10.025 - 0.957\sin(2000\pi t)$$

$$v_{o2} = V_{CC} - I_{CQ2}R_C + A_{vds}v_{i1} = 10.025 + 0.957\sin(2000\pi t)$$

The simulation results agree very well with the expressions we have given for the voltages and currents.

(d) We used the **Analysis/Setup/Transient** menu to specify a Fourier analysis of VC(Q2) for a center frequency of 1000 Hz and 9 harmonics. In the output file we find that the total harmonic distortion is 0.306%.

(e) With V_{im} = 50 mV, the output amplitude is sufficiently large that considerable distortion occurs. The simulation shows total harmonic distortion of 6.3%.

Problem 7.52

Formulas for the CMRR's are given in Table 7.2 on page 450 in the book as

$$CMRR_b = \frac{r_\pi + (\beta + 1)(R_{EF} + 2R_{EB})}{r_\pi + (\beta + 1)R_{EF}} = 2 \times CMRR_s$$

For large CMRR, we need to select $R_{EF} = 0$ and R_{EB} as large as possible.

Problem 7.53

In Table 7.2 on page 450 in the book, we find

$$R_{id} = 2[r_\pi + (\beta + 1)R_{EF}]$$

$$R_{icm} = \frac{r_\pi + (\beta + 1)R_{EF}}{2} + (\beta + 1)R_{EB}$$

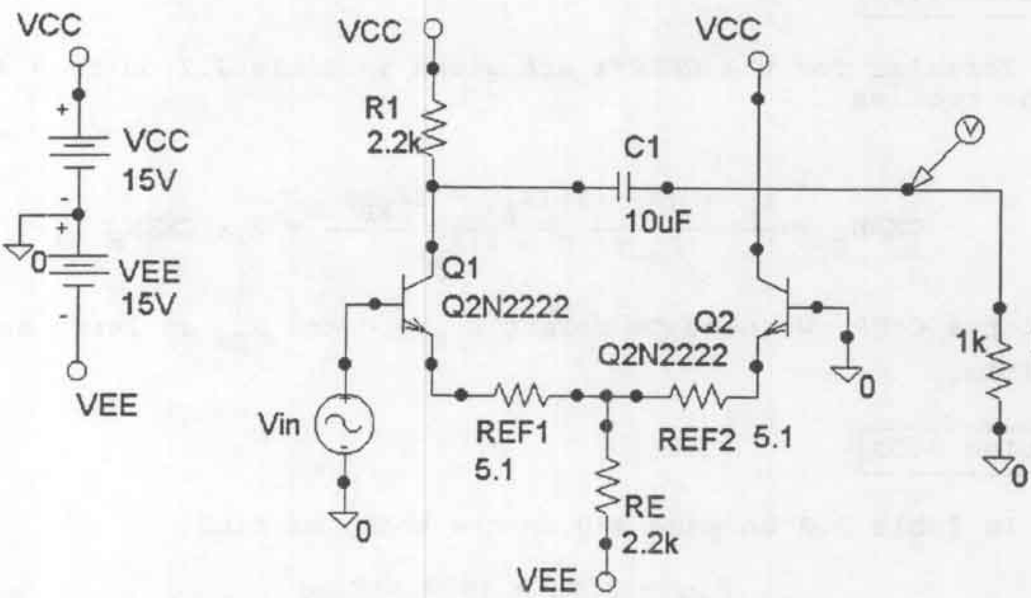
Thus to attain large values for R_{id} and R_{icm}, we need large β, small I_{CQ} (so r_π is large), and large R_{EF}. Furthermore for large R_{icm}, we need to make R_{EB} large.

Problem 7.54

To attain small distortion, we select a large value for R_{EF}. [Compare Figure 7.28 (page 440) with Figure 7.26 (page 439) and notice that the curve is straighter in Figure 7.28 which is for nonzero value of R_{EF}.] Another possibility is to drive the input terminals with current sources. (In other words increase the source impedance.) In some cases, larger values for I_{CQ} result in smaller distortion. Also for any amplifier, keeping the signal small will reduce distortion.

Problem 7.55

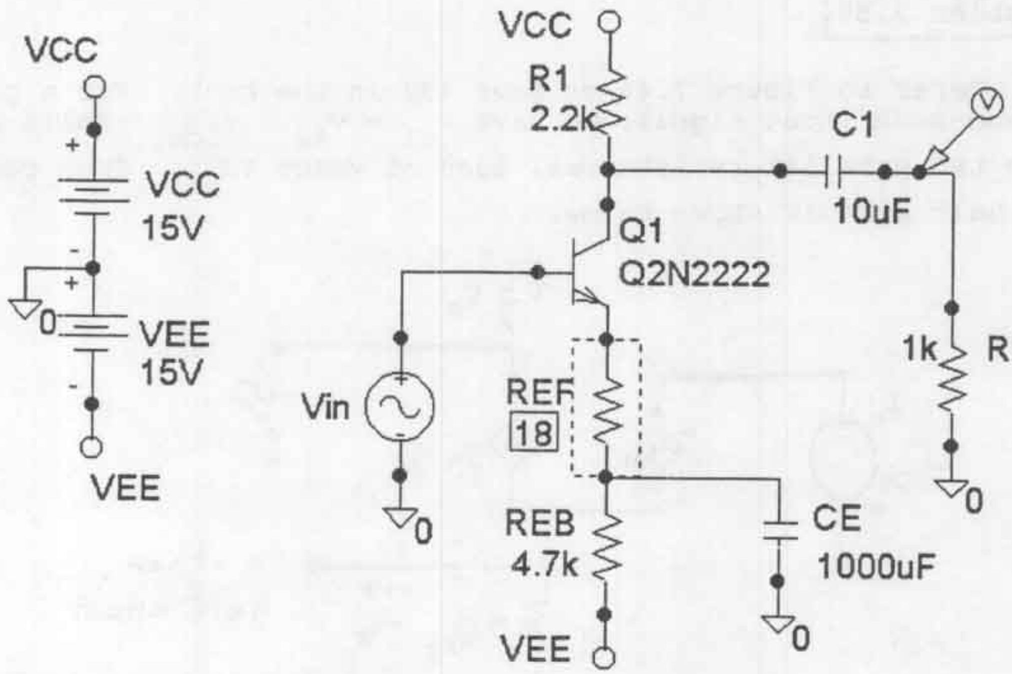
One answer is:



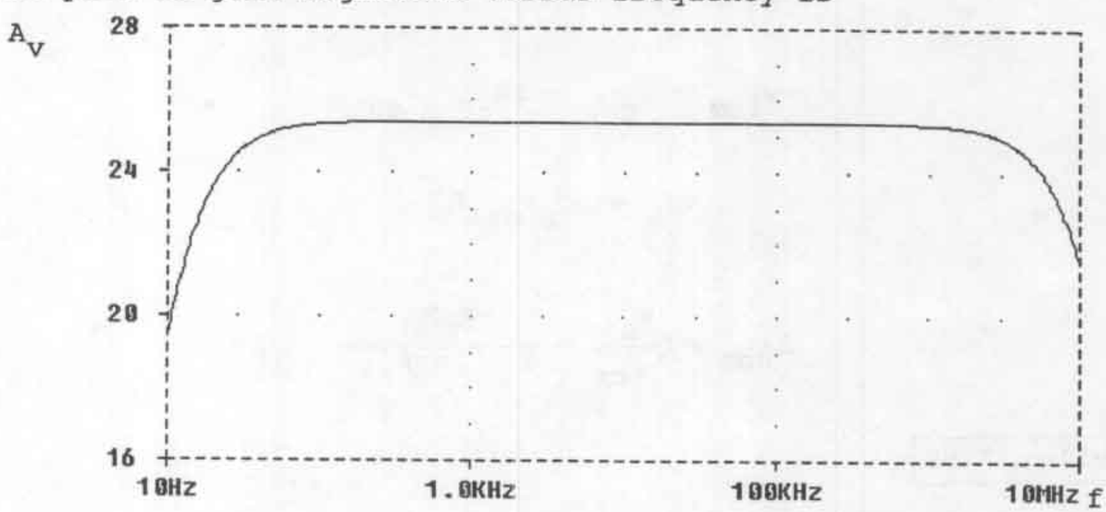
Many combinations of component values will work. We first simulated this circuit with $R_{EF1} = R_{EF2} = 0$ attaining a midband gain of about -45. Then we increased R_{EF1} and R_{EF2} by trial and error to attain a gain of -25.

Problem 7.56

Many combinations of component values will work. One possibility is shown on the next page. We increased R_{EF} by trial and error to attain a gain of -25.



The plot of gain magnitude versus frequency is

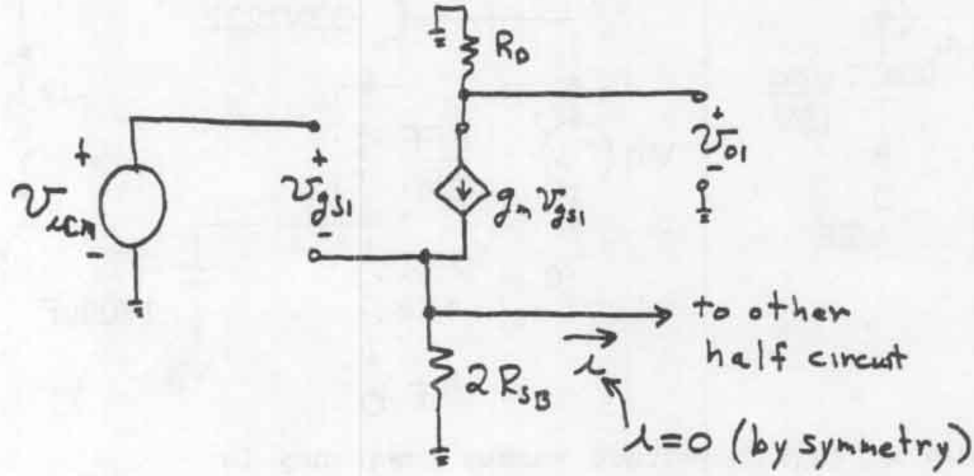


Problem 7.57

The main advantages of the source-coupled pair compared to the emitter-coupled pair are the low input bias current and nearly infinite input impedance of the JFET or MOSFET (at low frequencies). The disadvantages of the source-coupled pair compared to the emitter-coupled pair are lower gain magnitude and higher offset voltage.

Problem 7.58

Refer to Figure 7.46 on page 462 in the book. For a pure common-mode input signal, we have $v_{i1} = v_{i2} = v_{icm}$. Split R_{SB} into two parallel resistances, each of value $2R_{SB}$. Then consider the half circuit shown below.



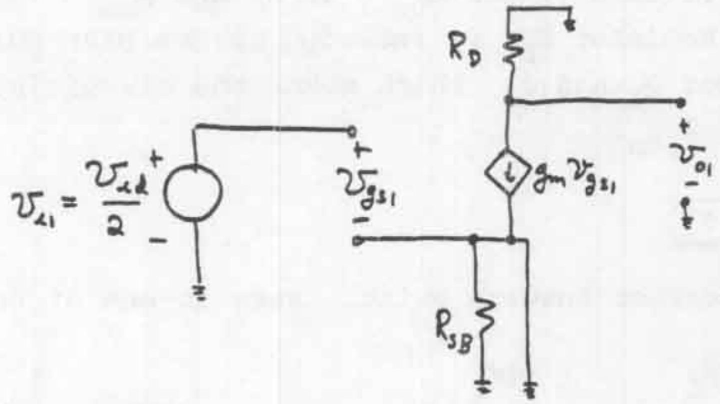
$$v_{icm} = v_{gs1} + 2R_{SB} g_m v_{gs1}$$

$$v_{o1} = -g_m v_{gs1} R_D$$

$$A_{vcm} = \frac{v_{o1}}{v_{icm}} = \frac{-g_m R_D}{1 + 2g_m R_{SB}}$$

Problem 7.59

Refer to Figure 7.46 on page 462 in the book. For a pure differential signal, we have $v_{i1} = -v_{i2} = v_{id}/2$. By symmetry, the voltage at the top end of R_{SB} is zero. Thus, we can consider the top end of R_{SB} to be grounded. The resulting half circuit is:



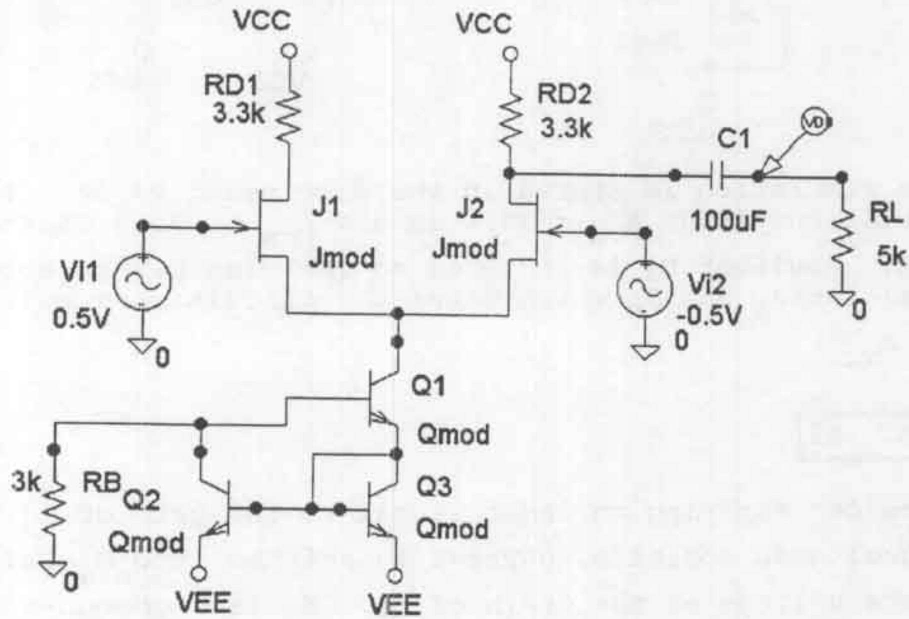
$$v_{id}/2 = v_{gs1}$$

$$v_{o1} = -g_m R_D v_{gs1}$$

$$A_{vds} = v_{o1}/v_{id} = -g_m R_D/2$$

Problem 7.60

Many correct answers can be found. Here is one example:

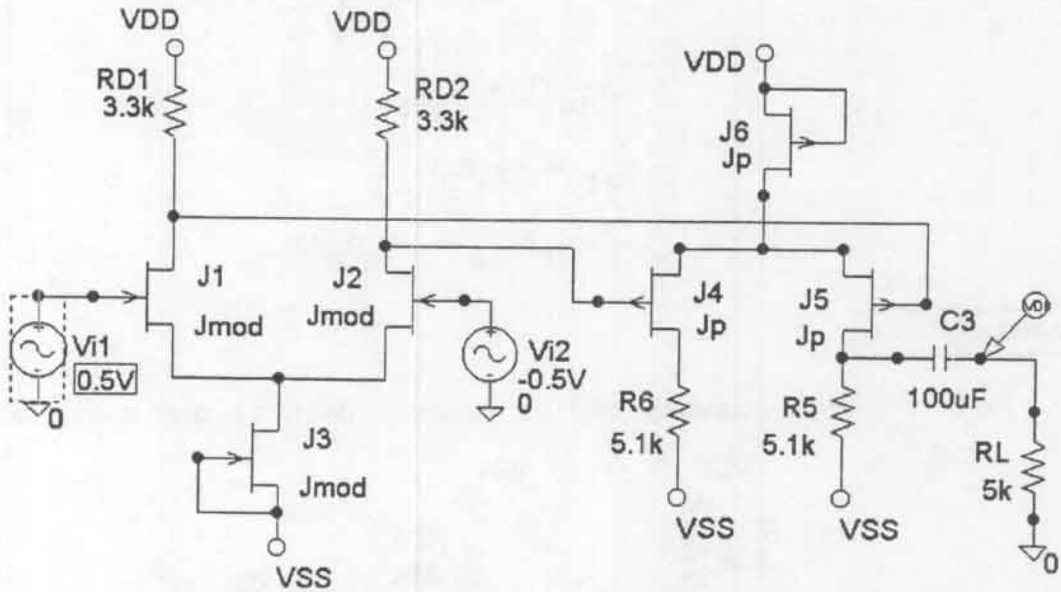


The simulation is stored in the file named P7_60. (Actually, two versions of the circuit are simulated: one for the differential gain and the other for the common-mode gain.) At 60

Hz, the simulation yields A_{vd} = 10 dB and A_{cm} = -67 dB for a CMRR of 77 dB. Resistor R_{D1} is included so the bias points are identical for J_1 and J_2, which makes the circuit more balanced and reduces A_{vcm}.

Problem 7.61

Many correct answers exist. Here is one of them:



The simulation is stored in the file named P7_61. At 60 Hz, the simulation yields A_{vd} = 38.4 dB and A_{cm} = $-35.\overline{5}$ dB for a CMRR of 74 dB. Resistor R_6 is included so the bias points are identical for J_4 and J_5 which makes the circuit more balanced and reduces A_{vcm}.

Problem 7.62

Consider applying an input signal to the gate of M_3. When this signal goes positive, current is shifted into M_4 which raises the voltage at the drain of M_4. M_7 is a common-source amplifier which is inverting. Thus we conclude that the gate of M_3 is the inverting input and the gate of M_4 is the noninverting input.

Problem 7.63

The gain of the differential stage and the transistor parameters (g_m and r_d) are the same as in the example. However because of the 1-kΩ load, the gain of the second stage (M_7) is reduced. The new value of the second-stage gain is

$$A_{v2} = -g_{m7}(r_{d7}||r_{d2}||R_L) = -3577 \times 10^{-6} \times (984\ \Omega)$$

$$= -3.52$$

The overall gain is $A_v = A_{v1} \times A_{v2} = 158 \times 3.52 = 556$. Notice that the open loop gain of the op amp is severely reduced by loading.

Problem 7.64

Consider the circuit on page 472 with $v_2 = 0$. If v_1 increases, the voltage at the collector of Q_2 increases. Then the voltage at the collector of Q_4 decreases, the voltage at the collector of Q_5 increases, and the output voltage increases. Thus the base of Q_1 is the noninverting input terminal. Similarly, the base of Q_2 is the inverting input terminal.

Problem 7.65

From Exercises 7.17, 7.18, and 7.19, we have $r_{\pi1} = r_{\pi2} = 52$ kΩ, $r_{\pi3} = r_{\pi4} = 10.4$ kΩ, $r_{\pi5} = 5.2$ kΩ, $r_{\pi6} = 520$ Ω, $R_{i2} = r_{\pi3} + r_{\pi4} = 20.8$ kΩ and the gain of the first stage consisting of Q_1 and Q_2 is $A_{v1} = 64.6$. Furthermore, $\beta = 200$ for all of the transistors.

The second stage consisting of Q_3 and Q_4 is a differential amplifier with a single-ended output. Q_5 is a common emitter amplifier with unbypassed emitter resistance. The input impedance of Q_5 is

$$R_{i5} = r_{\pi5} + (\beta + 1)R_5 = 890\ \text{k}\Omega$$

The gain of the second stage formed by Q_3 and Q_4 is

$$A_{v2} = \frac{\beta(R_4||R_{i5})}{2r_{\pi4}} = \frac{200 \times (9.89\ k\Omega)}{2 \times (10.4\ k\Omega)} = 95.1$$

The input impedance of Q_6 is

$$R_{i6} = r_{\pi6} + (\beta + 1)R_7 = 520 + 201 \times 1500 = 302\ k\Omega$$

The gain of Q_5 is

$$A_{v5} = \frac{\beta(R_6||R_{i6})}{r_{\pi5} + (\beta + 1)R_5} = \frac{200(14.8\ k\Omega)}{890\ k\Omega} = 3.33$$

The gain of Q_6 is

$$A_{v6} = \frac{(\beta + 1)R_7}{r_{\pi7} + (\beta + 1)R_7} = 0.998$$

Finally, the overall open-loop differential gain is $A_v = A_{v1}A_{v2}A_{v5}A_{v6} = 20.4 \times 10^3$.

Problem 7.66

From Exercise 7.18, we have $I_{CQ1} = I_{CQ2} = 0.1$ mA, $I_{CQ3} = I_{CQ4} = 0.5$ mA, $I_{CQ5} = 1$ mA, $I_{CQ6} = 10$ mA, $I_{CQ7} = 0.2$ mA, $I_{CQ8} = 0.2$ mA, and $I_{CQ9} = 1$ mA. We have

$$V_{CQ1} = V_{CQ2} = 15 - I_{CQ1}(100\ k\Omega) = 5\ V$$

$$V_{CQ4} = 15 - I_{CQ4}R_4 = 10\ V$$

$$V_{CQ5} = R_6 I_{CQ5} - 15 = 0.6\ V$$

$$V_o = V_{CQ5} - V_{BE6} = 0.0$$

Problem 7.67

The circuit of Figure 7.54 is a voltage follower. Thus we expect to have $v_o = v_s = 2\sin(2000\pi t)$. The voltage at the emitter of Q_1 is

$$v_{E1} = v_s - V_{BE1} = 2\sin(2000\pi t) - 0.6$$

At the collector of Q_4 we have

$$v_{C4} = V_{CQ4} + v_o/(A_{v5}A_{v6}) = 10 - 0.6\sin(2000\pi t)$$

At the collector of Q_5 we have

$$v_{C5} = v_o + V_{BEQ6} = 2\sin(2000\pi t) + 0.7$$

(We have taken V_{BEQ6} as 0.7 V because of the relatively high bias current for Q_6. On the other hand we estimated $V_{BEQ1} \cong 0.6$ because of its lower bias current.)

The schematic is stored in the file named P7_67 and the results of the simulation agree quite well with the equations given above.

Problem 7.68

The simulation is stored in the file named P7_68. We included a feedback network consisting of a 100-H inductor and a 100-F capacitor to ensure that the op amp is biased in its active region. The large inductance and capacitance prevent feedback for the ac signal. We applied a 1-V input signal and performed an ac analysis to determine the magnitude of the output voltage which is equal to the open-loop voltage gain.

With $V_A = \infty$ the open-loop gain is 11,000. With $V_A = 50$ V the open loop gain is 15,800. This is a surprising result because a lower value of V_A reduces the output impedances of the transistors. Thus the effective load impedance for each stage is reduced and we expect lower gain. However as V_A becomes smaller, the bias currents in the circuit increase, which reduces r_π. This causes the gains of the various stages to increase.

Problem 7.69

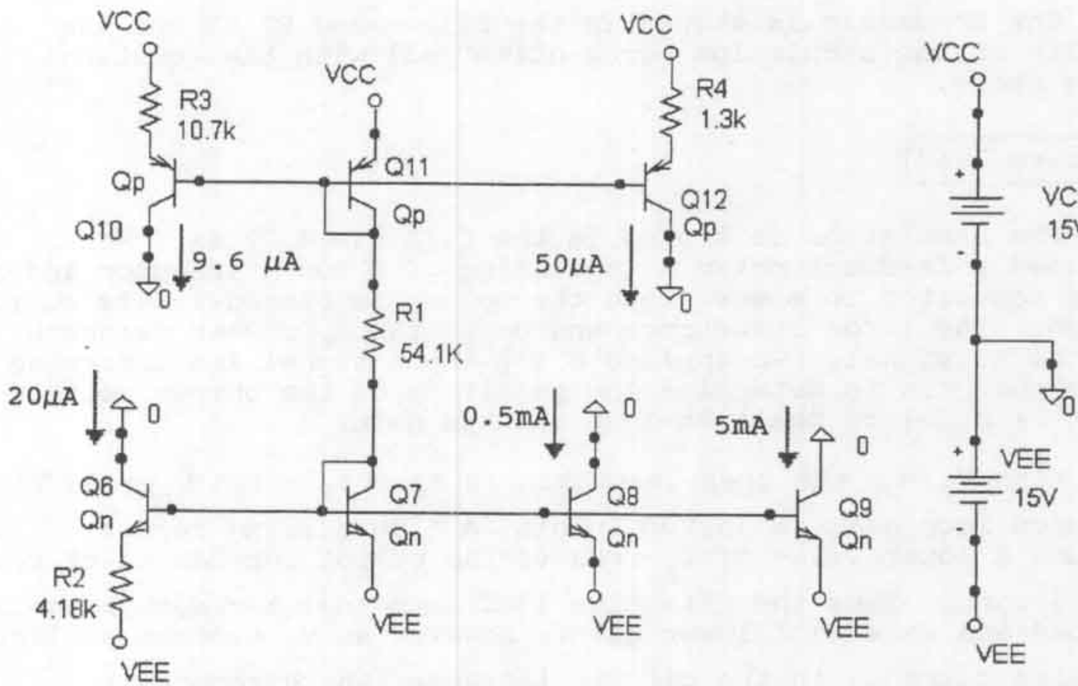
If we increase the voltage at the base of Q_1, current is steered away from Q_2 and the base voltage of Q_3 rises. This causes the voltage at the base of Q_4 to rise. In turn, the voltage at the base of Q_5 and the output voltage fall. Thus the base of Q_1 is the inverting input and the base of Q_2 is the noninverting input.

Problem 7.70

Q_1 and Q_2 form a differential amplifier with single ended output. Q_3 is an emitter follower. Q_4 is a common emitter amplifier and Q_5 is an emitter follower.

Problem 7.71

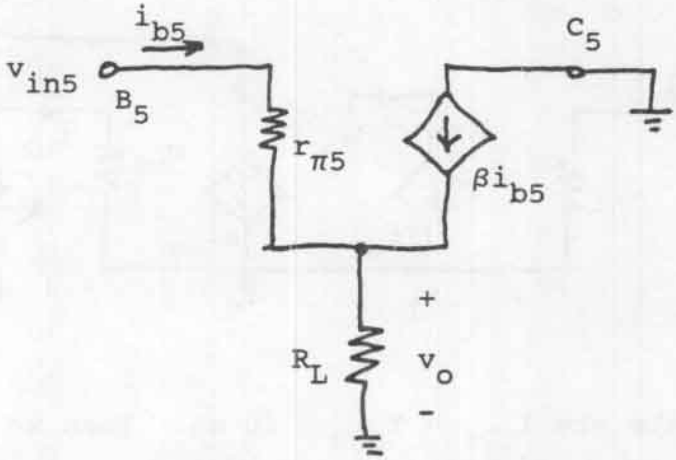
One design is shown below.



All of the transistors have unity area except Q_9 which has a relative area of 10. R_1 establishes a reference current of 0.5 mA. Q_3 is a simple mirror. Q_9 is a mirror with an area multiplier factor of 10. Q_{10}, Q_{12}, and Q_6 are Widlar sources. Initially, we estimated $R_1 = (30 - 1.2)/(0.5\ \text{mA}) = 57.6\ \text{k}\Omega$ and used Equation 7.16 to compute the emitter resistances of the Widlar sources. Then we simulated the circuit and adjusted the values to attain the desired currents.

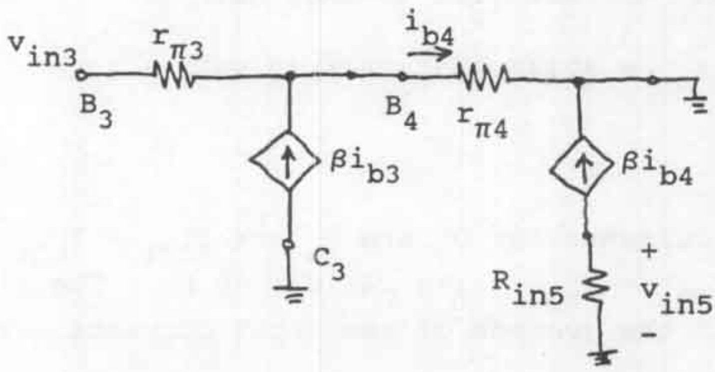
Problem 7.72

(a) The small-signal equivalent circuit for Q_5 and the load is:



The bias current for Q_5 is 5 mA and $r_{\pi 5} = \beta V_T/I_{CQ5} = 1040\ \Omega$. The input resistance is $R_{in5} = r_{\pi 5} + (\beta + 1)R_L = 202\ k\Omega$. The voltage gain is $A_{v5} = v_o/v_{in5} = (\beta + 1)R_L/[r_\pi + (\beta + 1)R_L] = 0.995$.

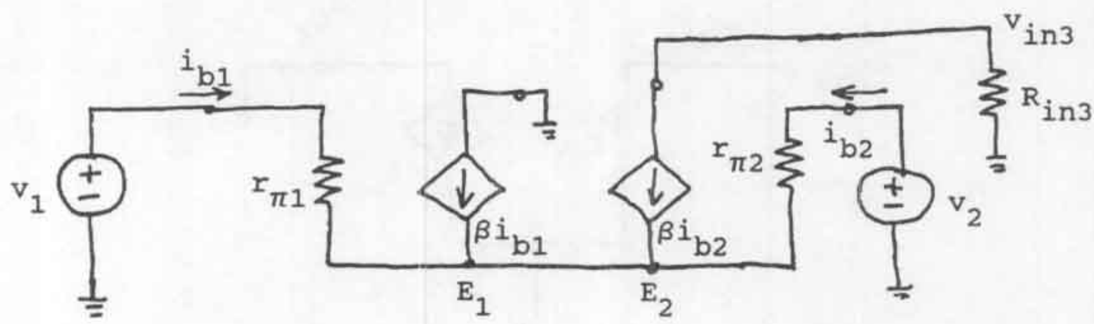
(b) and (c) The small-signal equivalent circuit for Q_3 and Q_4 is:



The bias currents are $I_{CQ3} = 50\ \mu A$ and $I_{CQ4} = 0.5$ mA. Thus $r_{\pi 3} = \beta V_T/I_{CQ3} = 104\ k\Omega$ and $r_{\pi 4} = 10.4\ k\Omega$. The input resistance is $R_{in3} = r_{\pi 3} + (\beta + 1)r_{\pi 4} = 2.19\ M\Omega$. The voltage gain of Q_3 is

$A_{v3} = (\beta + 1)r_{\pi 4}/[r_{\pi 3} + (\beta + 1)r_{\pi 4}] = 0.953$. The voltage gain of Q_4 is $A_{v4} = \beta R_{in5}/r_{\pi 4} = 3885$.

(d) The small-signal equivalent circuit for Q_1 and Q_2 is:



The bias currents are $I_{CQ1} = I_{CQ2} \cong 10\ \mu A$. Then we have $r_{\pi 1} = r_{\pi 2} = 520\ k\Omega$. If we consider the circuit for a pure differential input signal we have $v_1 = -v_2 = v_{id}/2$. Then by symmetry the voltage at E_1 (or E_2) is zero. Thus we have $i_{b1} = -i_{b2} = v_{id}/(2r_{\pi 1})$. The differential input impedance is $v_{id}/i_{b1} = 2r_{\pi 1} = 1.04\ M\Omega$. The differential voltage gain is $A_1 = v_{in3}/v_{id} = \beta R_{in3}/(2r_{\pi 1}) = 421$.

(e) The overall differential voltage gain is

$$A_{vd} = A_1 A_{v3} A_{v4} A_{v5} = 421(0.953)(3885)(0.995) = 1.55 \times 10^6$$

Problem 7.73

The bias currents for Q_1 and Q_2 are $I_{CQ1} = I_{CQ4} \cong 10\ \mu A$. Thus we have $I_{BQ1} = I_{BQ2} = (10\ \mu A)/\beta = 50$ nA. The bias current of an op amp is the average of the input currents. Thus, we have $I_B = 50$ nA.

Problem 7.74

The reference current flowing through R_3 is approximately $I_{ref} = (15 - 0.6)/(72\ k\Omega) = 200\ \mu A$. By symmetry we have $I_{CQ1} =$

$I_{CQ4} \cong 100\ \mu A$. Thus we have $I_{BQ1} = I_{BQ2} = (10\ \mu A)/\beta = 500$ nA. The bias current of an op amp is the average of the input currents thus we have $I_B = 500$ nA.

Problem 7.75

When the areas of the transistors are not equal we have: $I_{CQ1} = A_1 I_s \exp(V_{BE1}/V_T)$ and $I_{CQ2} = A_2 I_s \exp(V_{BE2}/V_T)$. Dividing the respective sides of these equations, we get

$$I_{CQ1}/I_{CQ2} = (A_1/A_2)\exp[(V_{BE1} - V_{BE2})/V_T]$$

Nominally, for zero output voltage from the op amp, we must have $I_{CQ1} = I_{CQ2}$. Thus, we have

$$1 = (A_1/A_2)\exp[(V_{BE1} - V_{BE2})/V_T]$$

The offset voltage is $V_{off} = V_{BE1} - V_{BE2}$. Hence, we have

$$1 = (A_1/A_2)\exp(V_{off}/V_T)$$

Solving, we obtain

$$A_1/A_2 = \exp(-V_{off}/V_T) = 0.953$$

Chapter 8

Exercise 8.1

The phasor for $v_{in}(t)$ is $\mathbf{V}_{in} = 5\angle -30^\circ$. Also we have $-6 = 20\log|\mathbf{V}_o/\mathbf{V}_{in}|$ which can be solved to find $|\mathbf{V}_o/\mathbf{V}_{in}| = 0.5$. Thus we have $\mathbf{V}_o/\mathbf{V}_{in} = 0.5\angle 45^\circ$. Then the phasor for the output is $\mathbf{V}_o = 5\angle -30^\circ \times 0.5\angle 45^\circ = 2.5\angle 15^\circ$. Finally we can write $v_o(t) = 2.5\cos(2000\pi t + 15^\circ)$.

Exercise 8.2

The break frequency for this circuit is given by Equation 8.6 which is $f_b = 1/(2\pi RC)$. Solving for C we have $C = 1/(2\pi f_b R)$. (a) Substituting values we find $C = 7.96\ \mu F$. (b) $C = 79.6\ \mu F$.

Exercise 8.3

(a) Refer to Figure 8.16a in the book. R_2 and C are in parallel. Furthermore R_1 and the R_2C_2 combination act as a two-element voltage divider. Thus we can write:

$$\frac{\mathbf{V}_o}{\mathbf{V}_{in}} = \frac{\dfrac{R_2(1/j\omega C)}{R_2 + (1/j\omega C)}}{R_1 + \dfrac{R_2(1/j\omega C)}{R_2 + (1/j\omega C)}} = \frac{R_2/(j\omega C)}{R_1R_2 + R_1/(j\omega C) + R_2/(j\omega C)}$$

$$= \frac{R_2/(R_1 + R_2)}{1 + j\omega CR_1R_2/(R_1 + R_2)} = \frac{R_2/(R_1 + R_2)}{1 + j(f/f_b)}$$

where $f_b = \dfrac{1}{2\pi CR_1R_2/(R_1 + R_2)}$. Substituting values we obtain $f_b = 2.12$ kHz and

$$\frac{V_o}{V_{in}} = \frac{0.25}{1 + jf/(2.12 \times 10^3)}$$

converting the constant to decibels we have $20\log(0.25) \cong -6$ dB. The Bode plots are shown in Figure 8.17(a) in the book.

(b) Here again we have a voltage divider

$$\frac{V_o}{V_{in}} = \frac{R_2}{R_2 + \dfrac{R_1(1/j\omega C)}{R_1 + (1/j\omega C)}} = \frac{R_1R_2 + R_2/(j\omega C)}{R_1R_2 + R_1/(j\omega C) + R_2/(j\omega C)}$$

$$= \frac{j\omega CR_1R_2 + R_2}{j\omega CR_1R_2 + R_1 + R_2} = \frac{R_2}{R_1 + R_2}\,\frac{1 + j\omega CR_1}{1 + j\omega CR_1R_2/(R_1 + R_2)}$$

$$= \frac{R_2}{R_1 + R_2}\,\frac{1 + j(f/f_z)}{1 + j(f/f_p)}$$

where $f_z = 1/(2\pi R_1C)$ and $f_p = \dfrac{1}{2\pi CR_1R_2(R_1 + R_2)}$. Substituting values we obtain $f_z = 1.59$ kHz, $f_p = 160.7$ kHz, and

$$\frac{V_o}{V_{in}} = (9.9 \times 10^{-3})\,\frac{1 + j(f/f_z)}{1 + j(f/f_p)}$$

The Bode plots are shown in Figure 8.17b in the book.

(c) From the circuit we can write

$$\frac{V_o}{V_{in}} = \frac{R_2}{R_1 + R_2 + j\omega L} = \frac{R_2}{R_1 + R_2}\,\frac{1}{1 + j\omega L/(R_1 + R_2)}$$

$$= \frac{R_2}{R_1 + R_2}\,\frac{1}{1 + j(f/f_p)}$$

where $f_p = (R_1 + R_2)/(2\pi L) = 477$ kHz and

$$\frac{V_o}{V_{in}} = \frac{0.6667}{1 + j(f/f_p)}$$

The Bode plots are shown in Figure 8.17c in the book.

Exercise 8.4

Equation 8.34 gives the pole frequency as

$$f_{p1} = \frac{1}{2\pi[C_{gs}R_{sig} + C_{gd}(R_{sig} + g_m R'_L R_{sig} + R'_L)]}$$

where $R'_L = \dfrac{1}{1/r_d + 1/R_{bias} + 1/R_L}$.

(a) Thus if the load resistance increases, the pole frequency decreases. (b) If the source resistance R_{sig} increases, the pole frequency decreases.

Exercise 8.5

From Example 8.3, we have R_{sig} = 10 kΩ, g_m= 4 mS, r_d = 25 kΩ, R'_L = 20 kΩ, and A_{mid} = -80.

(a) For C_{gs} = 1 pF and C_{gd} = 2 pF, we have

$$f_{p1} = \frac{1}{2\pi[C_{gs}R_{sig} + C_{gd}(R_{sig} + g_m R'_L R_{sig} + R'_L)]} = 95.3 \text{ kHz}$$

(b) For C_{gs} = 2 pF and C_{gd} = 1 pF, we have

$$f_{p1} = \frac{1}{2\pi[C_{gs}R_{sig} + C_{gd}(R_{sig} + g_m R'_L R_{sig} + R'_L)]} = 187 \text{ kHz}$$

(c) Thus we conclude that a small value for C_{gd} is more critical than a small value for C_{gs} in attaining wide bandwidth.

Exercise 8.6

Refer to Figure 8.20 in the book. At the gate node, we can write the the current equation

$$\frac{V_{gs}(s) - V_{sig}(s)}{R_{sig}} + \frac{V_{gs}(s)}{1/(sC_{gs})} + \frac{V_{gs}(s) - V_o(s)}{1/(sC_{gd})} = 0 \qquad (1)$$

Writing a current equation the drain node, we obtain

$$\frac{V_o(s) - V_{gs}(s)}{1/(sC_{gd})} + \frac{V_o(s)}{R_L'} + g_m V_{gs}(s) = 0 \qquad (2)$$

Next, we solve Equation (2) for V_{gs}:

$$V_{gs} = \frac{(sC_{gd} + 1/R_L')V_o(s)}{sC_{gd} - g_m}$$

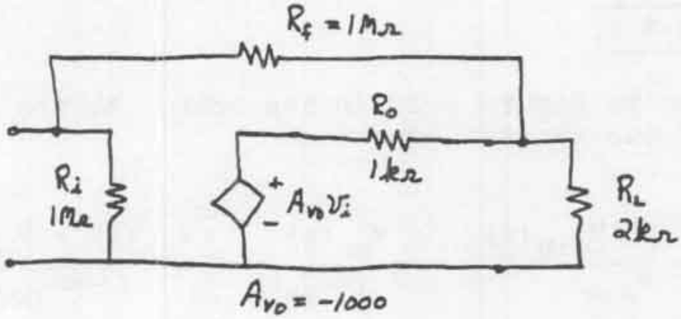
Then we substitute for V_{gs} in Equation (1) and solve for A_v.

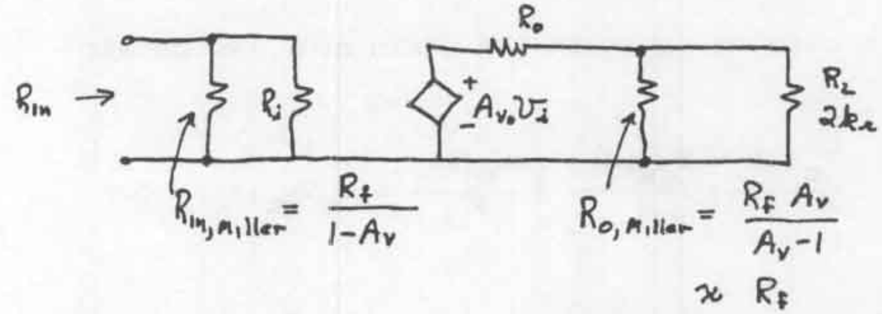
$$A_v(s) = \frac{V_o}{V_{sig}} = -g_m R_L' \times$$

$$\frac{1 - s(C_{gd}/g_m)}{1 + s[C_{gs}R_{sig} + C_{gd}(R_{sig} + g_m R_L' R_{sig} + R_L')] + s^2 C_{gs}C_{ds}R_{sig}R_L'}$$

Exercise 8.7

(a) The equivalent circuits are shown on the next page.





The loaded voltage gain is $A_v = A_{vo} \dfrac{R_L || R_{o,Miller}}{R_o + R_L || R_{o,Miller}} \cong -666$

Then we have $R_{in,Miller} = R_f/(1 - A_v) = 1499\ \Omega$ and $R_{in} = R_i || R_{in,Miller} = 1497\ \Omega$.

(b) With $R_L = \infty$, we obtain $A_v \cong -999$, $R_{in,Miller} = 1\ k\Omega$ and $R_{in} = 999\ \Omega$.

Exercise 8.8

Refer to the equivalent circuit shown in Figure 8.26b. Add the Miller output capacitance which is (approximately) C_{gd} in parallel with R'_L. Then if we write a current equation at the drain terminal we have:

$$\mathbf{V}_o/R'_L + g_m\mathbf{V}_i + j\omega C_{gd}\mathbf{V}_o = 0$$

Solving for the voltage gain, we have:

$$A_v = \frac{-g_m R'_L}{1 + j\omega R'_L C_{ds}}$$

The break frequency is $f_b = 1/(2\pi R_L' C_{ds})$. Substituting values from Examples 8.3 and 8.4 ($R_L' = 20\ k\Omega$ and $C_{ds} = 1\ pF$), we obtain $f_b = 7.96\ MHz$. Notice that the break frequency for the output circuit is much higher than that of the input circuit, so the half-power bandwidth is determined almost entirely by the input circuit.

Exercise 8.9

Equations 8.38 and 8.48 are:

$$r_\pi = \beta V_T / I_{CQ} \quad \text{and} \quad g_m = I_{CQ}/V_T$$

Solving Equation 8.44 for C_π, we have

$$C_\pi \cong \frac{\beta}{2\pi r_\pi f_t} - C_\mu$$

The plots are shown in Figure 8.32 in the book.

Exercise 8.10

Following the procedure of Example 8.7, we have $g_m = I_{CQ}/V_T = (1\ mA)/(26\ mV) = 38.5\ mS$. The range given on the data sheets for $\beta = h_{fe}$ at a bias point of $I_{CQ} = 1\ mA$ is 50 to 300. We use the average value $\beta = (300 + 50)/2 = 175$. Then we have

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{175 \times 0.026}{10^{-3}} = 4550\ \Omega$$

The data sheet gives a maximum value for h_{re} of 8×10^{-4}, which we use in computing r_μ. Equation 8.41 yields

$$r_\mu \cong \frac{r_\pi}{h_{re}} = \frac{4550}{8 \times 10^{-4}} = 5.7\ M\Omega$$

We use Equation 8.42 to find a value for $r_o \cong 1/h_{oe}$. The data sheet gives a range for h_{oe} from 5 μS to 35 μS. Thus, r_o ranges from 28.6 kΩ to 200 kΩ. We take the average value r_o =

(28.6 + 200)/2 = 114 kΩ as a typical value. As in Example 8.7 we estimate C_μ = 8 pF. Then we have:

$$C_\pi \cong \frac{\beta}{2\pi r_\pi f_t} - C_\mu = \frac{175}{2\pi \times 4550 \times 90 \times 10^6} - 8\text{ pF} = 60\text{ pF}$$

From the data sheet we have $r_x C_\mu = 150 \times 10^{-12}$. Solving for r_x and substituting the value found for C_μ, we have r_x = 19 Ω.

Exercise 8.11

$$r_\pi = \frac{\beta V_T}{I_{CQ}} \qquad C_\pi \cong \frac{\beta}{2\pi r_\pi f_t} - C_\mu$$

$$g_m = \frac{I_{CQ}}{V_T} = 0.385 \text{ for all three devices}$$

$$R'_L = R_L || R_C || r_o \qquad C_T = C_\pi + C_\mu(1 + g_m R'_L)$$

$$R'_s = r_\pi || [r_x + (R_B || R_s)] \qquad f_H = \frac{1}{2\pi R'_s C_T}$$

Device	r_π (Ω)	C_π (pF)	C_T (pF)	R'_s (Ω)	f_H (MHz)
A	260	148	638	48.6	5.13
B	260	173	369	51.8	8.33
C	130	120	316	38.5	13.1

Exercise 8.12

For $R_s = 0$, we have $R'_s = r_\pi || r_x$ = 18.4 Ω. Then we can compute $f_H = 1/(2\pi R'_s C_T) = 1/[2\pi(18.4)980 \times 10^{-12}]$ = 8.83 MHz.

Exercise 8.13

(a) $R'_s = R_s || R_E || r_\pi || (1/g_m)$ = 2.45 Ω

$$R'_L = R_C || R_L = 255\ \Omega$$

$$f_{H1} = \frac{1}{2\pi C_\pi R'_s} = \frac{1}{2\pi(196 \times 10^{-12})(2.45)} = 331\text{ MHz}$$

$$f_{H2} = \frac{1}{2\pi C_\mu R'_L} = \frac{1}{2\pi(8 \times 10^{-12})(255)} = 78\text{ MHz}$$

(b) $A_v = \beta R'_L / r_\pi = 225(255)/585 = 98.1$

$$R_{in} = R_E || [r_\pi/(\beta + 1)] = 2.58\ \Omega$$

$$A_{vs} = A_v \frac{R_{in}}{R_s + R_{in}} = 4.81$$

(c) The simulation is stored in the file named Exer8_13. It yields $f_H = 51$ MHz and $A_{vsmid} = 4.79$.

Exercise 8.14

Select R_B so the dc drop across it is small compared to V_{EE}. Since we expect $I_{BQ} = I_{CQ}/\beta = (10\text{ mA})/225 = 44\ \mu A$. Thus we should have $R_B(44\ \mu A) << 15$ V. We select $R_B = 10$ kΩ. Next we have

$$R_{E1} = \frac{V_{EE} - V_{BE} - V_{RB}}{I_{EQ}} = \frac{15 - 0.7 - 0.44}{10\text{ mA}} = 1.39\text{ k}\Omega$$

$$R_{E1} = \frac{V_{EE} - V_{BE}}{I_{EQ}} = \frac{15 - 0.7}{10\text{ mA}} = 1.43\text{ k}\Omega$$

Consequently we choose the nominal values $R_{E1} = R_{E2} = 1.3$ kΩ. The program is stored in the file named Exer8_14. It yields $f_H = 9.7$ MHz and $A_{vs} = 33.3$ dB.

Exercise 8.15

Solving Equation 8.70 we have $R_o = 1/(2\pi f_H C_L)$. Substituting values we find that the output resistance must be less than 79.6

Ω to achieve $f_H > 5$ MHz. An emitter follower would be the best choice to achieve this relatively low output resistance.

Exercise 8.16

The Bode plot is shown in Figure 8.51 in the book. The amplifier has break frequencies of 1, 10 and 100 Hz. Because the breaks at 10 Hz and 1 Hz have negligible effect at 100Hz, the half-power bandwidth is almost exactly equal to 100 Hz.

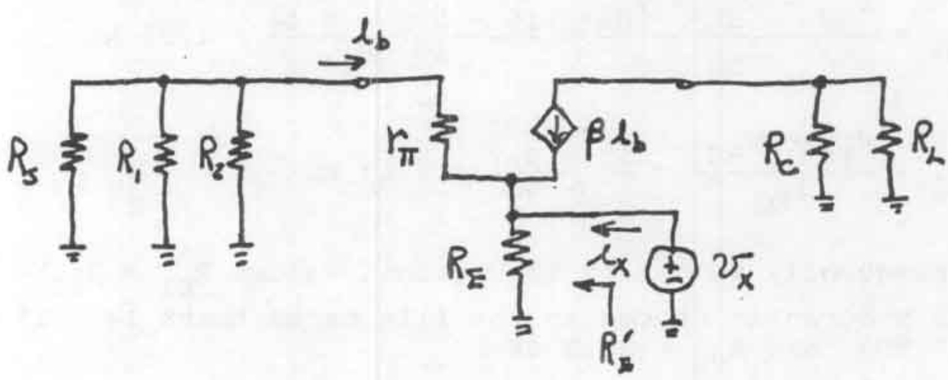
Exercise 8.17

The resistance in series with C_1 is $R_s + R_{i1} = 200$ kΩ. Thus the break frequency for C_1 is $f_1 = 1/[2\pi C_1(R_s + R_{i1})] = 0.796$ Hz. Similarly, we find $f_2 = 53.1$ Hz, and $f_3 = 15.9$ kHz. Notice that f_3 is much greater than either of the other two break frequencies. Thus to reduce the lower half-power frequency it is most important to increase the value of C_3.

Exercise 8.18

(a) See Figure 8.55 in the book for the equivalent circuit.

(b) To determine the resistance seen by C_E, we replace v_s by a short circuit and replace C_E by a test source as shown below. Then we determine the resistance $R = v_x/i_x$.



$$i_b = \frac{v_x}{r_\pi + R_1||R_2||R_s}$$

$$i_x = \frac{v_x}{R_E} + (\beta + 1)i_b = \frac{v_x}{R_E} + \frac{v_x(\beta + 1)}{r_\pi + R_1||R_2||R_s}$$

$$R'_E = \frac{v_x}{i_x} = \frac{1}{\frac{1}{R_E} + \frac{(\beta + 1)}{r_\pi + R_1||R_2||R_s}} = R_E|| \left[\frac{r_\pi + R_1||R_2||R_s}{(\beta + 1)}\right]$$

Exercise 8.19

Refer to Figure 8.53 in the book. The Thévenin resistance and voltage of the base bias circuit are

$$V_B = V_{CC}\frac{R_2}{R_1 + R_2} = 5 \text{ V} \qquad R_B = R_1||R_2 = 3.33 \text{ k}\Omega$$

Then we have

$$I_{BQ} = \frac{V_B - V_{BEQ}}{R_B + R_E(\beta + 1)} = 21.04\ \mu\text{A} \quad \text{and } I_{CQ} = \beta I_{BQ} = 4.21 \text{ mA}$$

$$r_\pi = \beta V_T/I_{CQ} = 1235\ \Omega$$

$$R'_E = R_E||\left[\frac{r_\pi + R_1||R_2||R_s}{(\beta + 1)}\right] = 9.87\ \Omega$$

$$f_1 = 1/(2\pi R'_E C_E) = 161 \text{ Hz}$$

Problem 8.1

On a logarithmic scale, the variable is multiplied by a certain factor for equal increments of length along the scale. On the other hand for a linear scale, a certain value is added to the variable for equal increments of length along the scale.

Problem 8.2

We say that f_2 is a decade higher than f_1 if $f_2/f_1 = 10$. If $f_2/f_1 = 2$, f_2 is said to be an octave higher than f_1.

Problem 8.3

A Bode magnitude plot of a network function is a plot of the magnitude of the network function in decibels versus frequency. The frequency axis is logarithmic. Assuming that the magnitude is in decibels, the vertical axis is linear. (If we were to plot the magnitude directly without converting to decibels, the vertical axis would be logarithmic.)

A Bode phase plot is a plot of phase versus frequency with a linear scale for phase and a logarithmic scale for frequency.

Problem 8.4

We assume that the network function is written as a ratio of polynomials in s. Then the poles are the roots of the denominator and the zeros are the roots of the numerator.

Problem 8.5

See Figure 8.1 in the book for the circuit diagram. Above the break frequency, the magnitude of the voltage transfer function V_o/V_{in} declines at a rate of 20 dB/decade.

Problem 8.6

$$\text{number of decades} = \log_{10}(2200/50) = 1.643$$

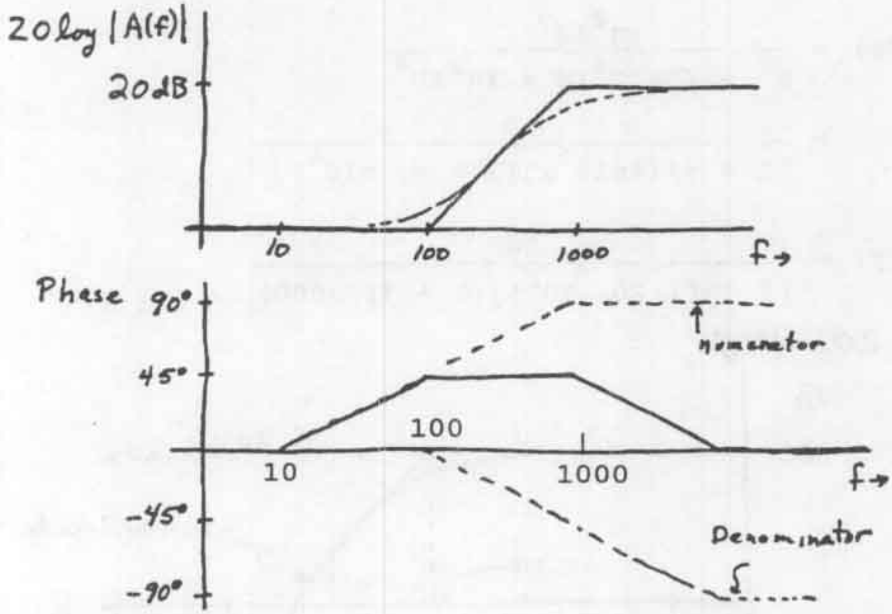
$$\text{number of octaves} = \log_2(2200/50) = \frac{\log_{10}(44)}{\log_{10}(2)} = 5.46$$

Problem 8.7

(a) $$A(s) = \frac{10(s + 200\pi)}{(s + 2000\pi)} = \frac{1 + s/200\pi}{1 + s/2000\pi}$$

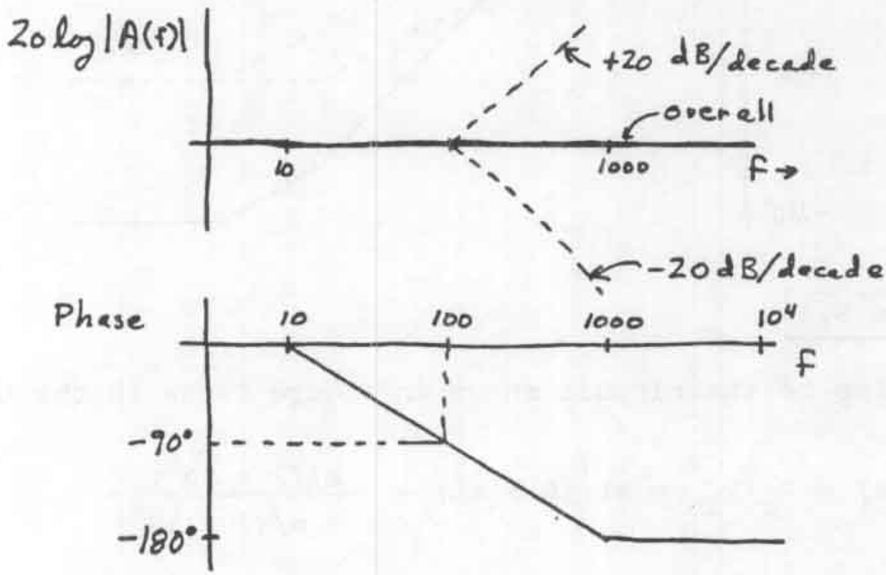
$$A(f) = \frac{1 + j(f/100)}{1 + j(f/1000)}$$

The plots are shown on the next page.



(b) $A(s) = \frac{s - 200\pi}{s + 200\pi} = \frac{1 - s/200\pi}{1 + s/200\pi}$

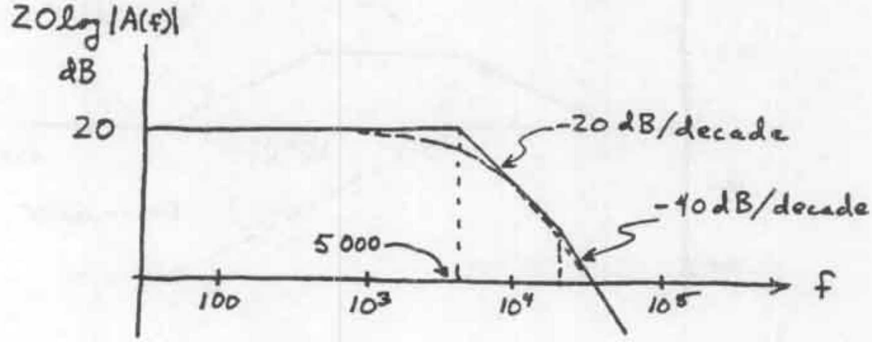
$A(f) = \frac{1 - j(f/100)}{1 + j(f/100)}$

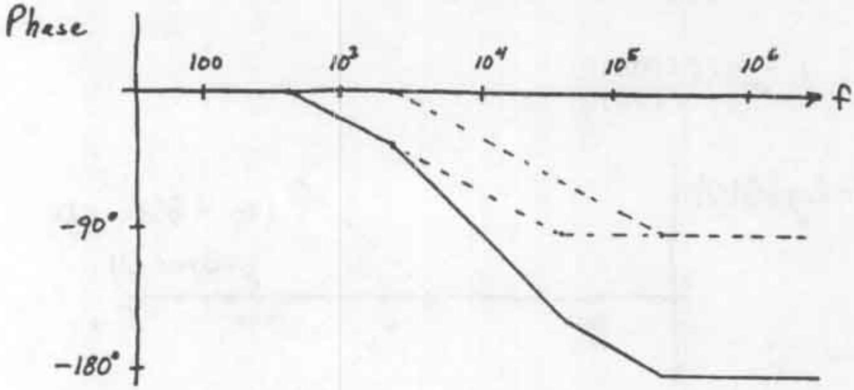


(c) $$A(s) = \frac{4\pi^2 10^9}{s^2 + (5\pi 10^4)s + 4\pi^2 10^8}$$

$$= \frac{10}{[1 + s/(4\pi 10^4)][1 + s/(\pi 10^4)]}$$

$$A(f) = \frac{10}{[1 + jf/(20\times 10^3)](1 + jf/5000)}$$





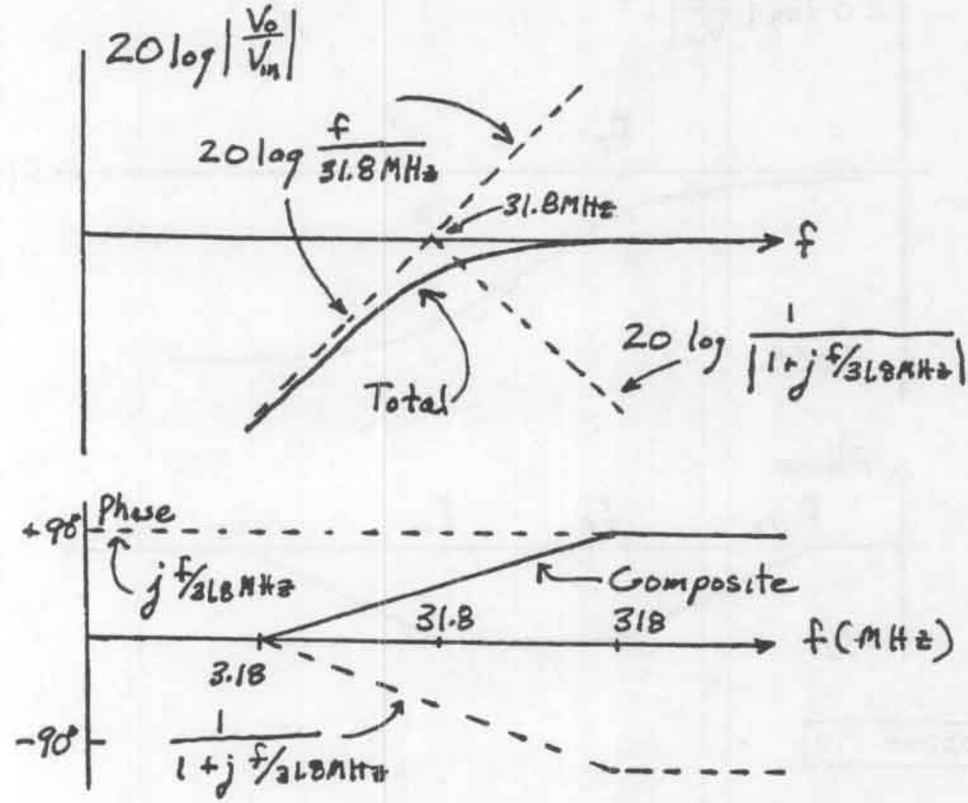
Problem 8.8

(a) Refer to the circuit shown in Figure P8.8a in the book.

$$A(s) = V_o/V_{in} = sL/(R + sL) = \frac{s/(2\times 10^8)}{1 + s/(2\times 10^8)}$$

$$A(f) = \frac{jf/(31.8\times 10^6)}{1 + jf/(31.8\times 10^6)}$$

Sketches of the magnitude and phase of A(f) are:



(b) Refer to the circuit shown in Figure P8.8b in the book.

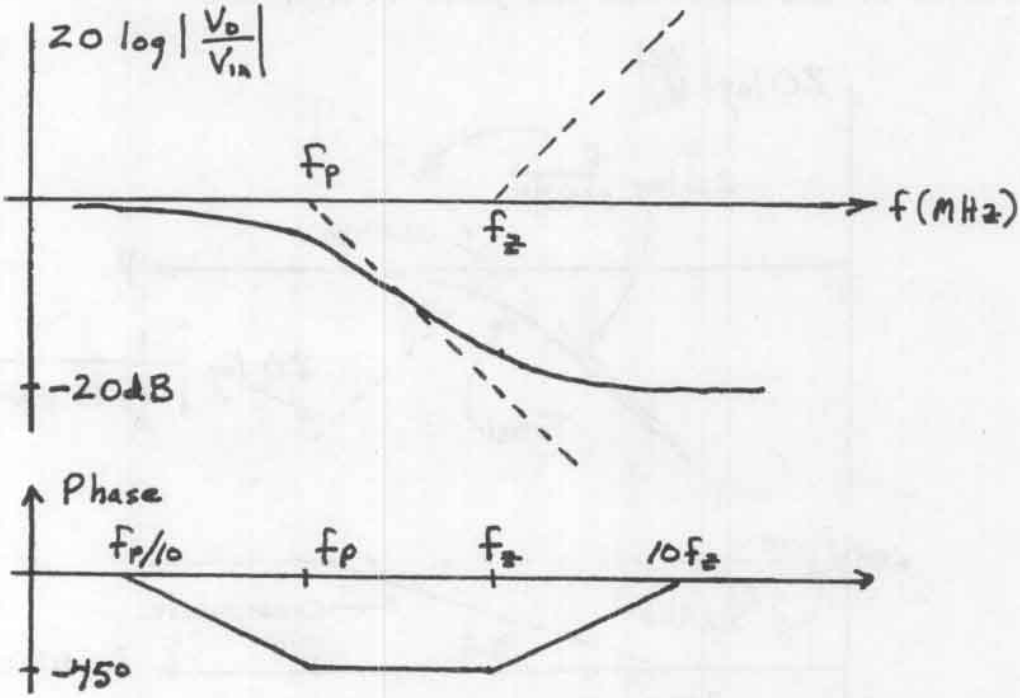
$$A(s) = V_o/V_{in} = \frac{R_2}{R_2 + sLR_1/(sL + R_1)}$$

$$= \frac{sL/R_1 + 1}{sL(R_1 + R_2)/R_1R_2 + 1}$$

$$A(f) = \frac{1 + j(f/f_z)}{1 + j(f/f_p)}$$

in which $f_z = R_1/(2\pi L) = 143.2$ MHz and $f_p = R_1R_2/[2\pi L(R_1 + R_2)] =$ 14.32 MHz

Sketches of the magnitude and phase of A(f) are shown on the next page.



Problem 8.9

(a) Refer to Figure P8.9 in the book. Writing a current equation at the output node, we obtain

$$sC(V_o - A_v V_{in}) + (V_o - V_{in})/R = 0$$

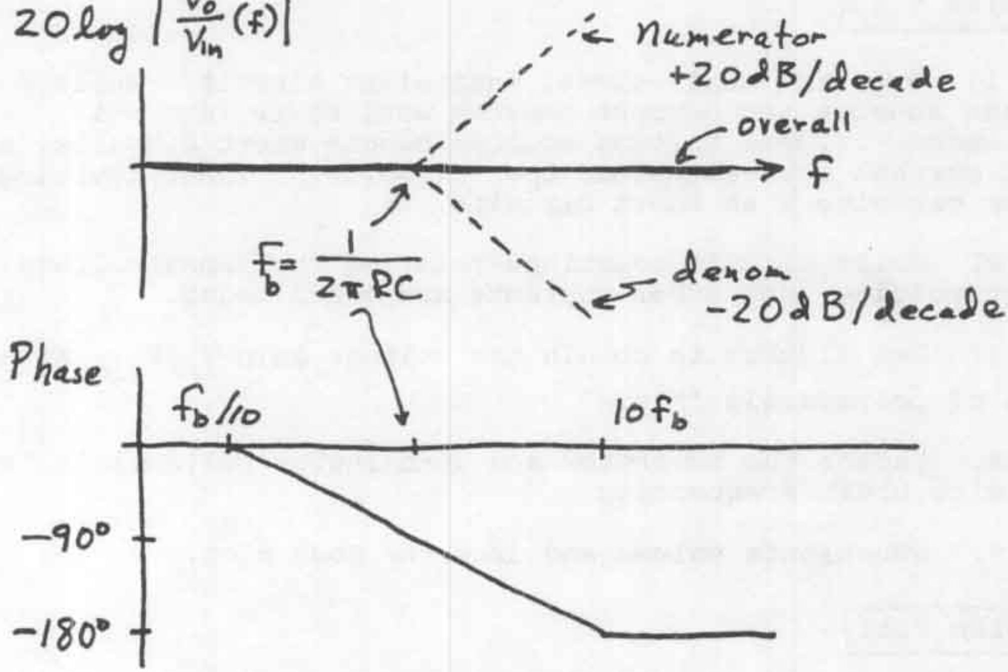
Solving for the gain we obtain:

$$A(s) = \frac{V_o}{V_{in}} = \frac{1 - RCs}{1 + RCs}$$

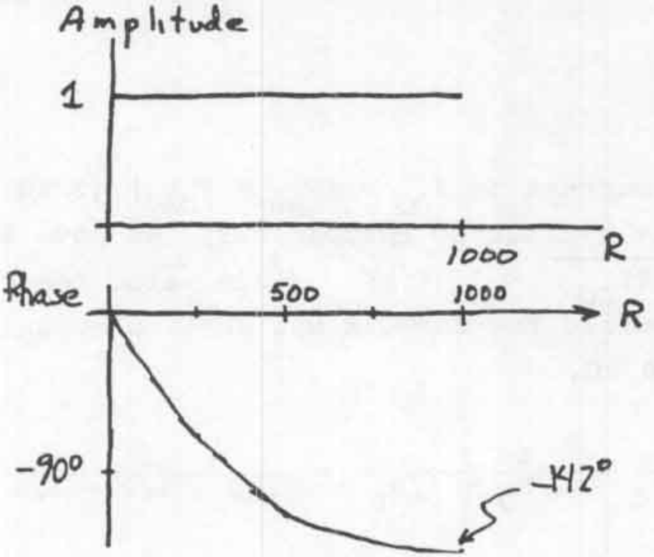
(b) We have a pole at $s = -1/(RC)$ and a zero at $s = 1/(RC)$.

(c) $A(f) = \dfrac{1 - j(f/f_b)}{1 + j(f/f_b)}$ in which $f_b = 1/(2\pi RC)$.

The magnitude and phase plots are shown on the next page.



(d) As R ranges from 0 to 1 kΩ, f_b ranges from ∞ to 339 kHz. The phase is given by $-2\tan^{-1}(f/f_b)$. The gain is unity at all frequencies for all values of R.



Problem 8.10

1. Draw the small-signal equivalent circuit. Replace dc voltage sources and current sources with their internal impedances. (Ideal voltage sources become short circuits, and ideal current sources become open circuits.) Treat coupling or bypass capacitors as short circuits.

2. Write circuit equations relating the input voltage, output voltage, and other currents and/or voltages.

3. Use algebra to obtain the voltage gain V_o/V_{sig} as a ratio of polynomials in s.

4. Factor the numerator and denominator polynomials to determine break frequencies.

5. Substitute values and draw the Bode plot.

Problem 8.11

1. Reduce the device capacitances C_{gs} and C_{gd}. (Reducing C_{gd} is more important than reducing C_{gs}.)

2. Reduce the source resistance R_{sig}.

3. Reduce the load resistance R_L which reduces the gain magnitude.

Problem 8.12

The bias current is $I_{DQ} = (V_{DD} - V_{DSQ})/(2\ \text{k}\Omega) = 2.5$ mA. This problem is similar to Example 8.3. We have $K = KP(W/L)/2 = 10^{-3}$. $g_m = 2\sqrt{KI_{DQ}} = 3.16$ mS. (This value for g_m is approximate because the formula was derived assuming $\lambda = 0$.) $r_d \cong 1/(\lambda I_{DQ}) = 40\ \text{k}\Omega$.

$$R'_L = \frac{1}{1/r_d + 1/R_D + 1/R_L} = \frac{1}{1/40 + 1/2 + 1/1} = 656\ \Omega$$

$$A_{mid} = -g_m R'_L = -(3.16 \times 10^{-3}) \times 656 = -2.07$$

The frequencies associated with the zero and the poles are

$$f_z = \frac{g_m}{2\pi C_{gd}} = 1 \text{ GHz}$$

$$f_{p1} = \frac{1}{2\pi[C_{gs}R_{sig} + C_{gd}(R_{sig} + g_m R_L' R_{sig} + R_L')]} = 15.1 \text{ MHz}$$

$$f_{p2} = \frac{C_{gs}R_{sig} + C_{gd}(R_{sig} + g_m R_L' R_{sig} + R_L')}{2\pi C_{gs} C_{ds} R_L' R_{sig}} = 2.03 \text{ GHz}$$

Because f_{p1} is much lower than the other two break frequencies, the upper half-power frequency is approximately equal to f_{p1}.

For the simulation we need to know the value of V_{bias}. The equation for the drain current is

$$I_{DQ} = K(V_{bias} - V_{to})^2(1 + \lambda V_{DSQ})$$

$$2.5 \times 10^{-3} = 10^{-3}(V_{bias} - 1)^2(1 + 0.01 \times 10)$$

Solving, we determine that $V_{bias} = 2.507$ V. The simulation is stored in the file named P8_12. The simulation yields $A_{mid} =$ 2.18 and $f_{3dB} = 14.8$ MHz. These values are in good agreement with our calculations. (The discrepancy is due to the fact that we assumed $\lambda = 0$ in computing g_m.)

Problem 8.13

The bias current is $I_{DQ} = (V_{DD} - V_{DSQ})/(2\ \text{k}\Omega) = 2.5$ mA. This problem is similar to Example 8.3. We have $K = KP(W/L)/2 = 10^{-3}$. $g_m = 2\sqrt{KI_{DQ}} = 3.16$ mS. (This value for g_m is approximate because the formula was derived assuming $\lambda = 0$.) $r_d \cong 1/(\lambda I_{DQ}) = 40\ \text{k}\Omega$.

$$R_L' = \frac{1}{1/r_d + 1/R_D + 1/R_L} = \frac{1}{1/40 + 1/2 + 1/1} = 656\ \Omega$$

$$A_{mid} = -g_m R'_L = -(3.16 \times 10^{-3}) \times 656 = -2.07$$

The frequencies associated with the zero and the poles are

$$f_z = \frac{g_m}{2\pi C_{gd}} = 1 \text{ GHz}$$

$$f_{p1} = \frac{1}{2\pi[C_{gs}R_{sig} + C_{gd}(R_{sig} + g_m R'_L R_{sig} + R'_L)]} = 485 \text{ MHz}$$

$$f_{p2} = \frac{C_{gs}R_{sig} + C_{gd}(R_{sig} + g_m R'_L R_{sig} + R'_L)}{2\pi C_{gs} C_{ds} R'_L R_{sig}} = \infty$$

Because f_z is not significantly higher than f_{p1}, we expect the upper half power frequency to be a bit higher than f_{p1} (due to the effect of the zero).

For the simulation we need to know the value of V_{bias}. The equation for the drain current is

$$I_{DQ} = K(V_{bias} - V_{to})^2(1 + \lambda V_{DSQ})$$

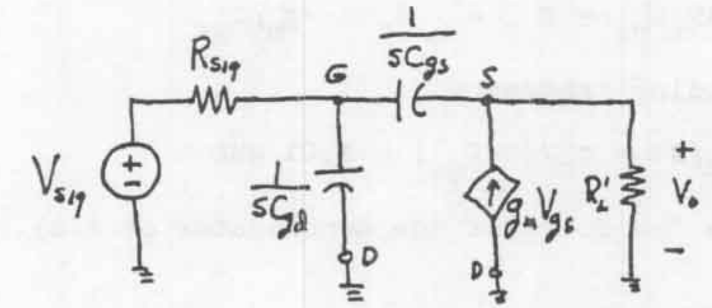
$$2.5 \times 10^{-3} = 10^{-3}(V_{bias} - 1)^2(1 + 0.01 \times 10)$$

Solving we determine that $V_{bias} = 2.507$ V. The simulation is stored in the file named P8_13. The simulation yields A_{mid} = 2.18 and f_{3dB} = 636 MHz. These values are in good agreement with our calculations. The discrepancy is due to the fact that we assumed $\lambda = 0$ in computing g_m.

Comparing the answers to Problems 8.12 and 8.13 we see that the bandwidth is much wider with $R_{sig} = 0$ than for $R_{sig} = 5$ kΩ.

Problem 8.14

(a) The small-signal equivalent circuit is shown on the next page.



(b) Writing current equations at the gate and drain we obtain:

$$\frac{V_g - V_{sig}}{R_{sig}} + sC_{gd}V_g + sC_{gs}(V_g - V_o) = 0 \qquad (1)$$

$$(V_g - V_o)(g_m + sC_{gs}) = V_o/R_L' \qquad (2)$$

Solving Equation (2) for V_g, substituting into Equation (1), and solving for the gain, we eventually obtain:

$$A(s) = \frac{V_o}{V_{sig}} = \frac{g_m R_L' + sR_L' C_{gs}}{1 + g_m R_L' + Bs + As^2}$$

in which

$$B = R_{sig}(1 + g_m R_L')(C_{gd} + C_{gs}) + C_{gs}R_L' - g_m R_{sig} R_L' C_{gs}$$

and

$$A = R_{sig}R_L' C_{gs}(C_{gd} + C_{gs}) - R_{sig}R_L' C_{gs}^{\ 2}$$

(c) Evaluating the gain expression for s = 0, we obtain the midband gain.

$$A_{mid} = \frac{g_m R_L'}{1 + g_m R_L'}$$

(d) We have $K = KP(W/L)/2 = 10^{-3}$; $g_m = 2\sqrt{KI_{DQ}} = 3.16$ mS; $r_d = \infty$ (because $\lambda = 0$); $R_L' = R_{bias}||R_L = 1$ kΩ; and $A_{mid} = 0.760$ which is equivalent to -2.39 dB.

The zero is the root of the numerator of the gain expression.

$$g_m R'_L + sR'_L C_{gs} = 0 \quad \Rightarrow \quad s_z = -g_m / C_{gs}$$

The corresponding frequency is

$$f_z = -s_z/2\pi = g_m/(2\pi C_{gs}) = 1.01 \text{ GHz}$$

The poles are the roots of the denominator of A(s). Evaluating we obtain

$$1 + g_m R'_L = 4.16$$

$$B = 26.3 \times 10^{-9}$$

$$A = 2.5 \times 10^{-18}$$

$$s_{p1} = -161 \times 10^6 \text{ and } s_{p2} = -10.3 \times 10^9$$

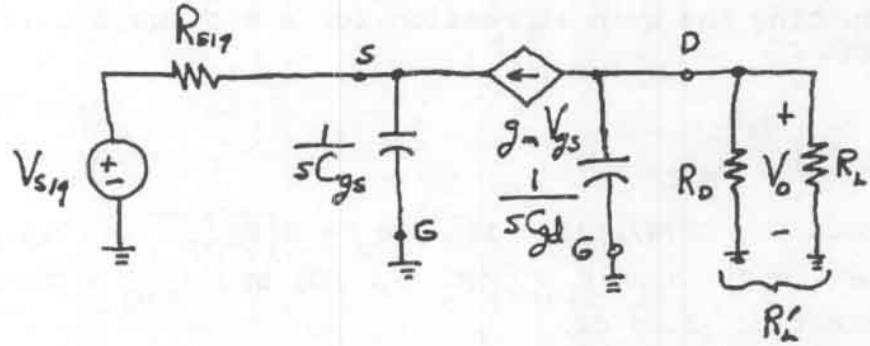
$$f_{p1} = 25.6 \text{ MHz and } f_{p2} = 1.65 \text{ GHz}$$

Because f_z and f_{p2} are much larger than f_{p1} we expect the half-power frequency to be very nearly equal to f_{p1}. Thus $f_{3dB} \cong 25.6$ MHz.

(e) The program is stored in the file named P8_14. The midband gain and half-power bandwidth agree very well with the values computed in part (d).

Problem 8.15

(a) The small-signal equivalent circuit is:



(b) Notice that $V_{gs} = -V_s$. Writing a current equation at the source node we obtain:

$$\frac{V_s - V_{sig}}{R_{sig}} + sC_{gs}V_s + g_m V_s = 0$$

Solving for V_s we obtain

$$V_s = V_{sig}\frac{1}{sC_{gs}R_{sig} + 1 + g_m R_{sig}} \qquad (1)$$

Writing a current equation at the drain node we have

$$g_m V_s = sC_{gd}V_o + V_o/R'_L$$

Solving for V_o we obtain

$$V_o = V_s\frac{g_m R'_L}{sC_{gd}R'_L + 1} \qquad (2)$$

Using Equation (1) to substitute for V_s in Equation (2) and dividing both sides by V_{sig} we have

$$A(s) = \frac{V_o}{V_{sig}}$$

$$= \frac{g_m R'_L}{(sC_{gs}R_{sig} + 1 + g_m R_{sig})(sC_{gd}R'_L + 1)}$$

(c) The poles are the roots of the denominator of A(s).

$$s_{p1} = -(1 + g_m R_{sig})/(C_{gs}R_{sig}) \quad \text{and} \quad s_{p2} = -1/(C_{gd}R'_L)$$

The break frequencies associated with these poles are

$$f_{p1} = (1 + g_m R_{sig})/(2\pi C_{gs}R_{sig}) \quad \text{and} \quad f_{p2} = 1/(2\pi C_{gd}R'_L)$$

(d) The midband gain is obtained by evaluating A(s) for s = 0.

$$A_{mid} = \frac{g_m R'_L}{1 + g_m R_{sig}}$$

(e) We have $K = KP(W/L)/2 = 10^{-3}$; $g_m = 2\sqrt{KI_{DQ}} = 3.16$ mS; $r_d = \infty$ (because $\lambda = 0$); $R'_L = R_D || R_L = 1\ k\Omega$; and $A_{mid} = 2.40$ which is equivalent to 7.6 dB. The break frequencies are $f_{p1} = 4.19$ GHz and $f_{p2} = 318$ MHz. Because f_{p1} is considerably greater than f_{p2}, the upper half-power frequency is approximately equal to f_{p2}.

(f) The program is stored in the file named P8_15. The simulation results match the hand calculations.

Problem 8.16

The pole and zero frequencies are given by Equations 8.33, 8.34 and 8.35. Usually f_z and f_{p2} are much higher than f_{p1}. Therefore the upper half-power frequency approximately equals f_{p1} which is given by

$$f_{p1} = \frac{1}{2\pi[C_{gs}R_{sig} + C_{gd}(R_{sig} + g_m R'_L R_{sig} + R'_L)]}$$

Substituting values, we have

$$10^6 = \frac{1}{18.84 \times 10^{-9} + (32 \times 10^{-12})R'_L}$$

Solving we find that $R'_L = 30.6$ kΩ. The midband gain is $A_{mid} = -g_m R'_L = -153$. Also we have

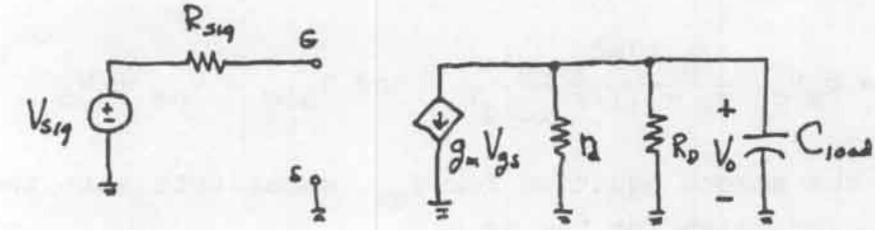
$$R'_L = \frac{1}{1/r_d + 1/R_{bias} + 1/R_L} = 30.6 \times 10^3 = \frac{1}{1/10^5 + 1/R_L}$$

from which we find $R_L = 44.1$ kΩ.

As a check we compute $f_z = 7.95$ GHz and $f_{p2} = 4.11$ GHz. Since these frequencies are much higher than f_{p1}, our initial assumption is justified.

Problem 8.17

(a) The small-signal equivalent circuit is:



(b) Notice that $V_{gs} = V_{sig}$. The output voltage is the current times the impedance of R'_L in parallel with $1/(sC_{load})$.

$$V_o = -g_m V_{sig} \frac{R'_L/(sC_{load})}{R'_L + 1/(sC_{load})}$$

from which we obtain

$$A(s) = \frac{V_o}{V_{sig}} = \frac{-g_m R'_L}{sC_{load}R'_L + 1}$$

(c) The pole is $s_p = -1/(C_{load}R'_L)$ and the corresponding break frequency is $f_p = 1/(2\pi C_{load}R'_L)$.

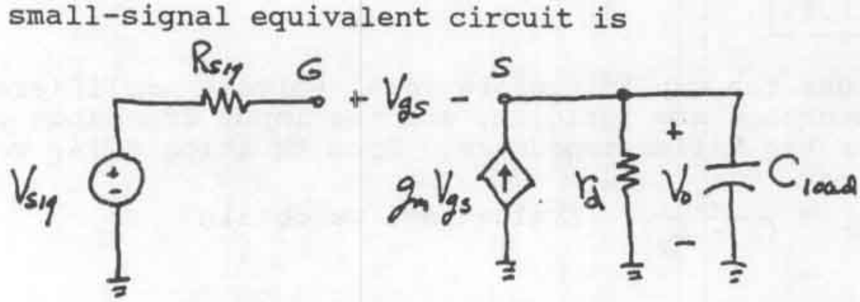
(d) $A_{mid} = A(s)|_{s=0} = -g_m R'_L$

(e) We have $K = KP(W/L)/2 = 10^{-3}$; $g_m = 2\sqrt{KI_{DQ}} = 3.16$ mS; $r_d = \infty$ (because $\lambda = 0$); $R'_L = R_D = 2$ kΩ; and $A_{mid} = -6.32$ which is equivalent to 16.0 dB. The break frequency is $f_{p1} = 39.8$ kHz.

(f) The program is stored in the file named P8_17. The simulation results match the hand calculations.

Problem 8.18

(a) The small-signal equivalent circuit is



(b) From the equivalent circuit we can write

$$V_o = g_m V_{gs} \frac{r_d (1/sC_{load})}{r_d + (1/sC_{load})} \quad \text{and } V_{sig} = V_{gs} + V_o$$

We solve the second equation for V_{gs}, substitute into the first equation, and solve for the gain.

$$A(s) = \frac{V_o}{V_{sig}} = \frac{g_m r_d}{1 + g_m r_d + sC_{load} r_d}$$

(c) The pole is the root of the denominator polynomial which is $s_p = -(1 + g_m r_d)/(C_{load} r_d)$. The corresponding break frequency is $f_p = (1 + g_m r_d)/(2\pi C_{load} r_d)$.

(d) The midband gain can be found by setting s = 0 in the expression for A(s).

$$A_{mid} = g_m r_d/(1 + g_m r_d)$$

(e) We have $K = KP(W/L)/2 = 10^{-3}$; $g_m = 2\sqrt{KI_{DQ}} = 3.16$ mS; $r_d = \infty$ (because $\lambda = 0$); and $A_{mid} = 1$ which is equivalent to 0 dB. For $r_d = \infty$, the break frequency is $f_p = g_m/2\pi C_{load} = 251$ kHz.

(f) The program is stored in the file named P8_18. The simulation results match the hand calculations.

Problem 8.19

First we determine the midband gain. Then we use this gain to determine the Miller capacitances. Finally we analyze the simplified circuit to determine the break frequencies. (Usually the analysis is much easier after applying Miller's Theorem.)

Problem 8.20

Because the amplifiers are ideal voltage amplifiers, their input impedances are infinite, and the input impedance of each circuit is the Miller impedance. From Equation 8.36, we have

$Z_{in,Miller} = \frac{Z_f}{(1 - A_v)}$. Evaluating, we obtain

(a) $Z_{in} = 909\ \Omega$ (b) $Z_{in} = 99.0\ \Omega$

(c) $Z_{in} = \infty$ (d) $Z_{in} = -10\ k\Omega$

Problem 8.21

Because the amplifiers are ideal voltage amplifiers, their input impedances are infinite, and the input capacitance of each circuit is the Miller capacitance. From Equation 8.36 we have

$$Z_{in,Miller} = \frac{Z_f}{(1 - A_v)} = \frac{1/(j\omega C_f)}{1 - A_v} = 1/[j\omega C_f(1 - A_v)]$$

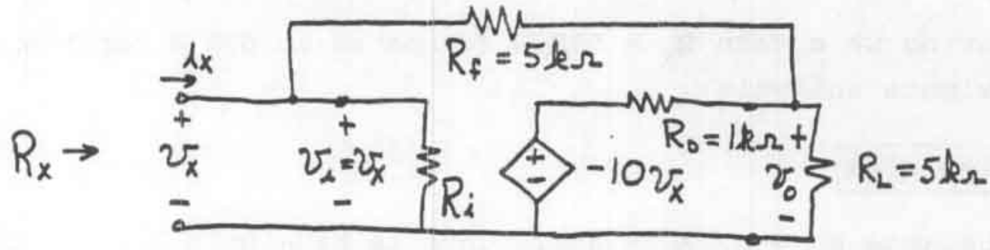
Thus the input capacitance is $C_{in} = C_f(1 - A_v)$. Evaluating we obtain

(a) $C_{in} = 1010\ pF$ (b) $C_{in} = 20\ pF$

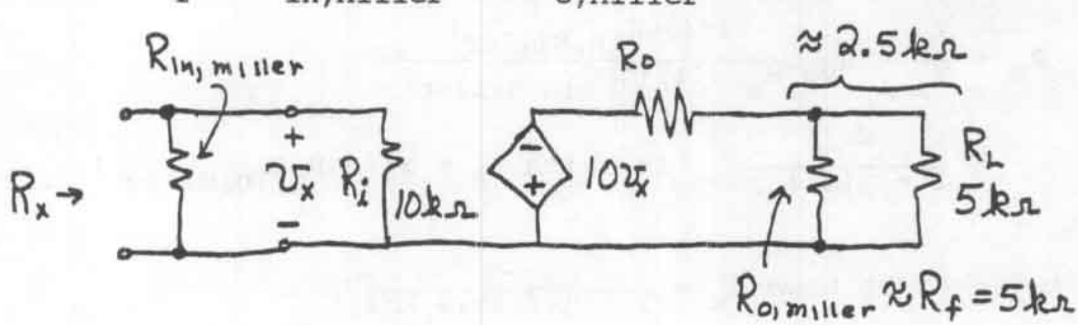
(c) $C_{in} = 0$ (d) $C_{in} = -90\ pF$

Problem 8.22

The equivalent circuit is



First for the approximate analysis we use the Miller effect to replace R_f by $R_{in,Miller}$ and $R_{o,Miller}$ as shown below.



$$A_v = -10\frac{(2.5\ k\Omega)}{(1\ k\Omega) + (2.5\ k\Omega)} = -7.14$$

$$R_{in,Miller} = \frac{R_f}{1 - A_v} = 614\ \Omega$$

$$R_x = R_i || R_{in,Miller} = 579\ \Omega$$

For the exact analysis, we refer to the original equivalent circuit and write these circuit equations:

$$i_x = \frac{v_x}{R_i} + \frac{v_x - v_o}{R_f} \qquad (1)$$

$$\frac{v_o}{R_L} + \frac{v_o - v_x}{R_f} + \frac{v_o - A_{vo}v_x}{R_o} = 0 \qquad (2)$$

We solve Equation (2) for v_o, substitute into Equation (1), and solve for R_x.

$$R_x = \frac{v_x}{i_x} = \frac{1}{\dfrac{1}{R_i} + \dfrac{1}{R_f} - \dfrac{1/R_f + A_{vo}/R_o}{1 + R_f/R_L + R_f/R_o}}$$

Evaluating we obtain $R_x = 588\ \Omega$ (compared to $579\ \Omega$ for the approximate analysis).

Problem 8.23

Because $R_o = 0$, $A_v = A_{vo}$. Thus we have $C_{in,Miller} = C(1 - A_v)$.

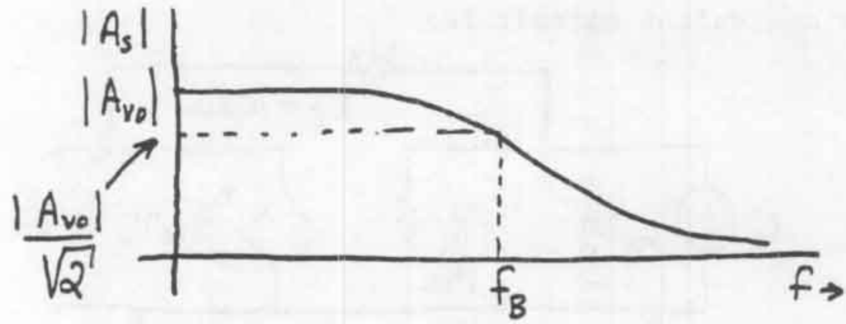
$$A_s = \frac{v_o}{v_s} = A_{vo}\frac{1/(j\omega C_{in,Miller})}{R_s + 1/(j\omega C_{in,Miller})}$$

$$= \frac{A_{vo}}{1 + j(f/f_B)} \quad \text{in which } f_B = 1/(2\pi R_s C_{in,Miller})$$

For $A_{vo} = -9$ we have $A_s = \dfrac{-9}{1 + jf/(15.9\text{ kHz})}$

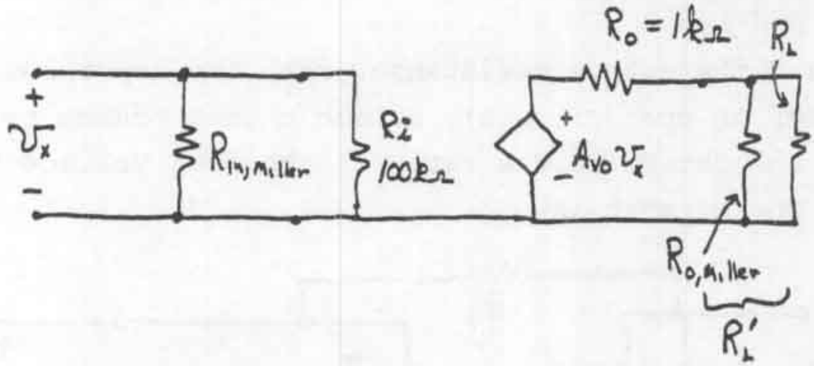
For $A_{vo} = -99$ we have $A_s = \dfrac{-99}{1 + jf/(1.59\text{ kHz})}$

The sketch of $|A_s|$ is



Problem 8.24

Because $|A_{vo}| >> 1$, we use an approximate analysis in which we assume that $R_{o,Miller} \cong R_f$. Then the equivalent circuit is:



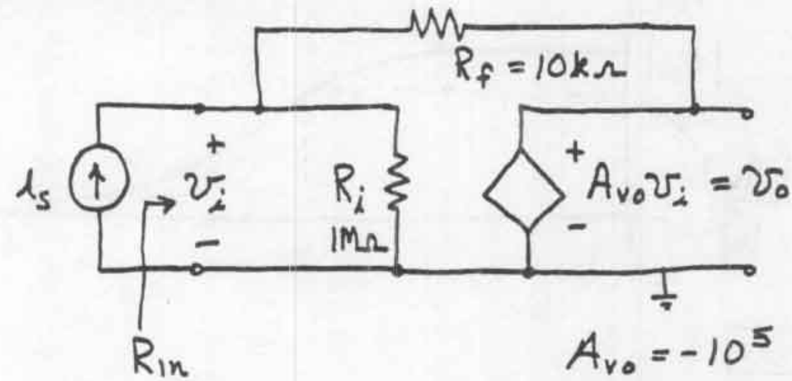
$R'_L = R_{o,Miller}||R_L \cong R_f||R_L$ $\qquad$ $A_v = A_{vo}R'_L/(R_o + R'_L)$

$R_{in,Miller} = R_f/(1 - A_v)$ $\qquad$ $R_x = R_i||R_{in,Miller}$

R_L	1 kΩ	10 kΩ
R'_L	995 Ω	9.52 kΩ
A_v	-49.9	-90.5
$R_{in,Miller}$	3.93 kΩ	2.19 kΩ
R_x	3.78 kΩ	2.14 kΩ

Problem 8.25

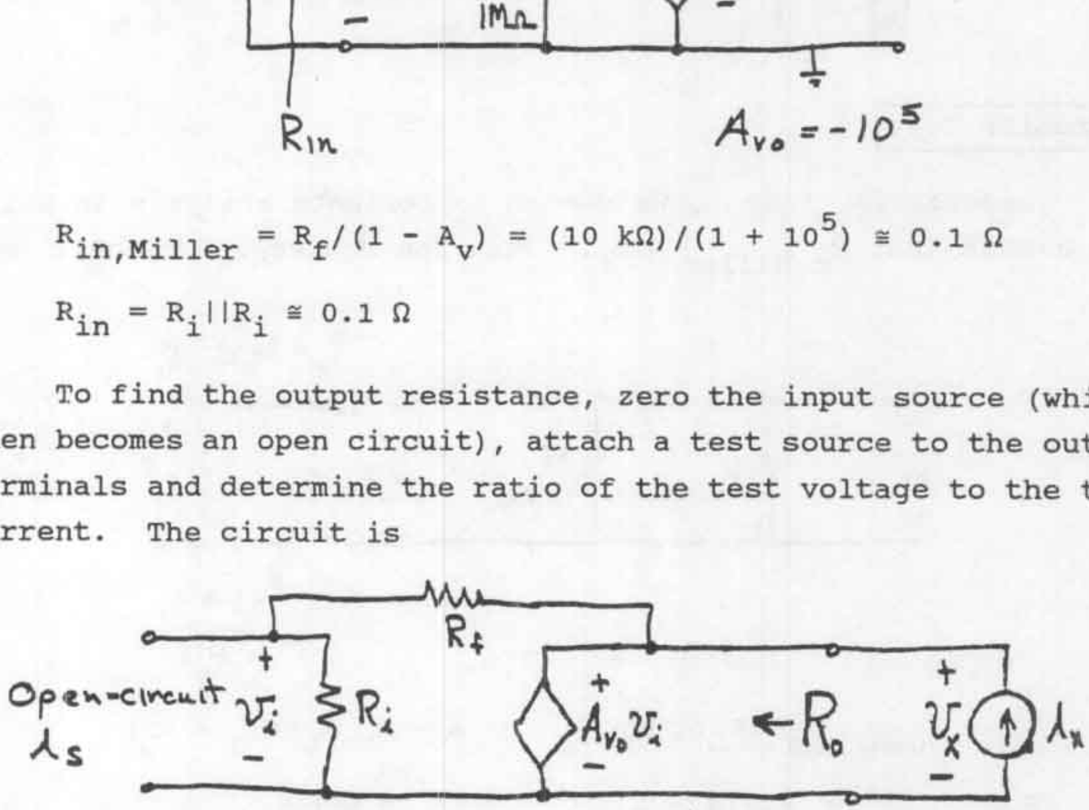
The equivalent circuit is:



$R_{in,Miller} = R_f/(1 - A_v) = (10\ k\Omega)/(1 + 10^5) \cong 0.1\ \Omega$

$R_{in} = R_i || R_i \cong 0.1\ \Omega$

To find the output resistance, zero the input source (which then becomes an open circuit), attach a test source to the output terminals and determine the ratio of the test voltage to the test current. The circuit is



Notice that we chose to use a current source for the test source. If we chose a voltage source, we would have two voltage sources in parallel forming an indeterminate circuit. We write a current equation at the top end of R_i:

$v_i/R_i + (v_i - A_{vo}v_i) = 0$

from which we have $v_i = 0$. Thus $v_x = A_{vo}v_i = 0$. Then the output resistance is $R_o = v_x/i_x = 0$. Because $R_o = 0$ and R_{in} is very small, we have a nearly ideal transresistance amplifier.

The transresistance gain is $R_m = v_o/i_s = A_{vo}v_i/(v_i/R_{in}) = A_{vo}R_{in} = -10^5(0.1\ \Omega) \cong -10\ k\Omega = -R_f$.

Problem 8.26

The equivalent circuits are shown in Figure 8.26 in the book, except that for the circuit under consideration we have $R'_L = R_D||r_d||R_L$. The midband voltage gain is $A_{mid} = -g_m R'_L$.

The bias current is $I_{DQ} = (V_{DD} - V_{DSQ})/(2\ k\Omega) = 2.5$ mA. We have $K = KP(W/L)/2 = 10^{-3}$. $g_m = 2\sqrt{KI_{DQ}} = 3.16$ mS. (This value for g_m is approximate because the formula was derived assuming $\lambda = 0$.) Also we have $r_d \cong 1/(\lambda I_{DQ}) = 40\ k\Omega$.

$$R'_L = \frac{1}{1/r_d + 1/R_D + 1/R_L} = \frac{1}{1/40 + 1/2 + 1/1} = 656\ \Omega$$

$$A_{mid} = -g_m R'_L = -(3.16 \times 10^{-3}) \times 656 = -2.07$$

Then the Miller capacitance is

$$C_{Miller} = C_{gd}(1 - A_{mid}) = (0.5\ pF)(1 + 2.07) = 1.54\ pF$$

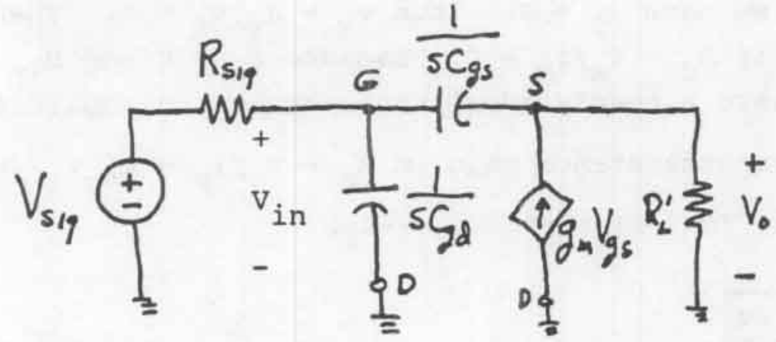
$$C_{total} = C_{gs} + C_{Miller} = 2.04\ pF$$

$$f_b = \frac{1}{2\pi R_{sig} C_{total}} = 15.6\ MHz$$

In Problem 8.12 we did an exact analysis of this circuit and obtained $f_b = 15.1$ MHz. (The simulation yielded $f_b = 14.8$ MHz.)

Problem 8.27

(a) The equivalent circuit is shown on the next page.



(b) In the midband, we have $V_{sig} = V_{in}$. Also, we have

$$V_{in} = V_{gs} + V_o \qquad \text{and} \qquad V_o = g_m V_{gs} R_L'$$

From which we have

$$A_{vs} = \frac{V_o}{V_{sig}} = A_v = \frac{V_o}{V_{in}} = \frac{g_m R_L'}{1 + g_m R_L'}$$

(c) $C_{Miller,in} = C_{gs}(1 - A_v)$

$$C_{total} = C_{gd} + C_{Miller,in}$$

$$f_b = 1/(2\pi R_{sig} C_{total})$$

(d) We have $K = KP(W/L)/2 = 10^{-3}$; $g_m = 2\sqrt{KI_{DQ}} = 3.16$ mS; $r_d = \infty$ (because $\lambda = 0$); $R_L' = R_{bias}||R_L = 1$ kΩ; and $A_v = 0.760$ which is equivalent to -2.39 dB. $C_{Miller,in} = C_{gs}(1 - A_v) = (0.5 \text{ pF})(1 - 0.760) = 0.120$ pF. $C_{total} = C_{gd} + C_{Miller,in} = 0.620$ pF. $f_b = 1/(2\pi R_{sig} C_{total}) = 25.7$ MHz.

In Problem 8.14, we did an exact analysis and determined that $f_{3-dB} = 25.6$ MHz. Thus, the Miller approximation is very accurate in this case.

Problem 8.28

See Figure 8.29 in the book.

Problem 8.29

For infinite Early voltage, r_o is infinite. Then neglecting the currents through r_μ and C_μ, the collector current is independent of changes in v_{CE} (within the active region). Thus from Equation 8.42, we have $h_{oe} \cong 1/r_o$, so h_{oe} is zero. (Keep in mind that h_{oe} is a conductance.)

Problem 8.30

Equations 8.41 and 8.42 are

$$r_o \cong 1/h_{oe} \quad \text{and} \quad r_o \cong \frac{V_A}{I_{CQ}}$$

I_{CQ} (mA)	r_o	h_{oe}
0.1	1 MΩ	1 μS
1	100 kΩ	10 μS
10	10 kΩ	100 μS

Problem 8.31

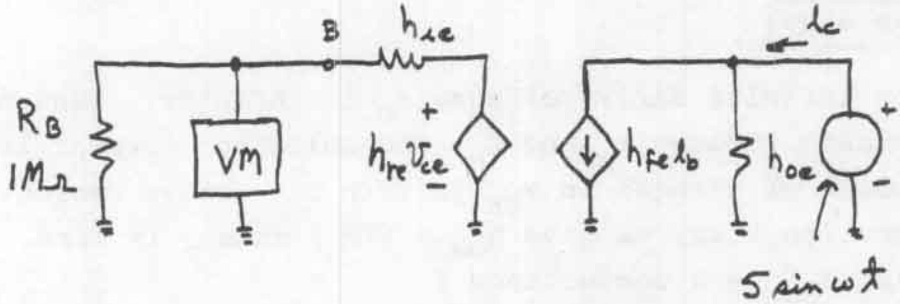
We have $h_{fe} \cong \beta$ and $h_{ie} \cong r_\pi$. Since $r_\pi = \beta V_T/I_{CQ}$, we have $h_{ie} \cong h_{fe}V_T/I_{CQ}$. At 300 K, $V_T \cong 26$ mV.

I_{CQ}	0.1 mA	1 mA	10 mA
h_{ie}	52 kΩ	5.2 kΩ	520 Ω

Problem 8.32

Using the hybrid-parameter equivalent for the BJT, the small-signal equivalent circuit is shown on the next page.

Because of the high value of R_B and the high impedance of the voltmeter compared to h_{ie}, we have $i_b \cong 0$. Thus, the voltmeter reads $h_{re}V_{ce,rms} = 10^{-4} \times 5/\sqrt{2} = 354\ \mu V$ rms.



Problem 8.33

Refer to the equivalent circuit shown in the solution to Problem 8.33. Because we assume that $i_b \cong 0$, we have $i_c \cong h_{oe}v_{ce} = 10^{-4} \times 5\sin(2000\pi t) = 50\sin(2000\pi t)$ μA. Thus, $I_{c,rms} = 35.4$ μA.

Problem 8.34

Refer to Figure P8.32 in the book and the equivalent circuit shown in the solution to Problem 8.32.

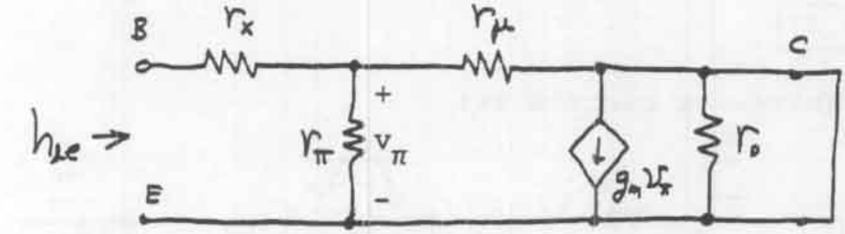
The dc base current is $I_{BQ} = (15 - V_{BEQ})/R_B = 14.35$ μA. Then we have $h_{fe} \cong \beta = I_{CQ}/I_{BQ} = (5\text{ mA})/(14.35\ \mu\text{A}) = 348$. Because of the high value of R_B and the high voltmeter impedance, the ac base current is negligible. Thus $i_c \cong h_{oe}v_{ce}$ which implies that $h_{oe} = I_{c,rms}/V_{ce,rms} = (0.1\text{ mA})/(5/\sqrt{2}) = 28.3\ \mu\text{S}$. Also $h_{re} \cong V_{be,rms}/V_{ce,rms} = (1\text{ mV})/(5/\sqrt{2}) = 2.83 \times 10^{-4}$. Finally $h_{ie} \cong r_\pi = \beta V_T/I_{CQ} = 348(0.026)/0.005 = 1810\ \Omega$.

Problem 8.35

Refer to the equivalent circuit on the next page.

$$h_{ie} = r_x + \frac{1}{1/r_\pi + 1/r_\mu}$$

$$= 19 + \frac{1}{1/585 + 1/(1.5 \times 10^6)} = 604\ \Omega$$



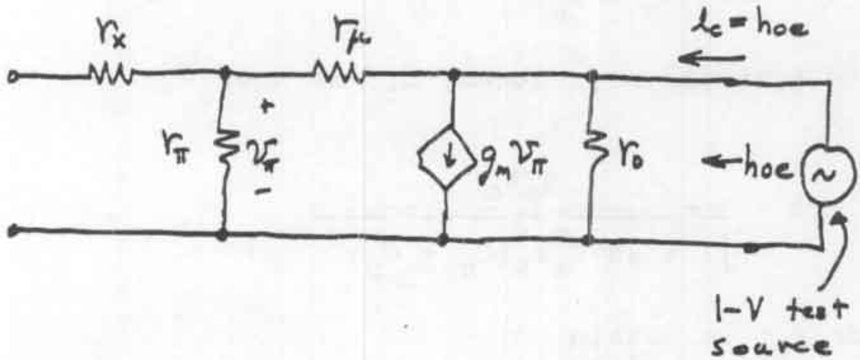
If we use the approximation $h_{ie} = r_\pi = 585\ \Omega$, the error is 3.1%, which is insignificant in view of the fact that β may vary from unit to unit by a ratio of 3 to 1.

Problem 8.36

From Equation 8.40, we have

$$h_{oe} = \left.\frac{i_c}{v_{ce}}\right|_{i_b=0}$$

Thus, h_{oe} is the conductance seen from the collector-emitter terminals with the base open circuited. The equivalent circuit is



Because we have used a 1-V test source

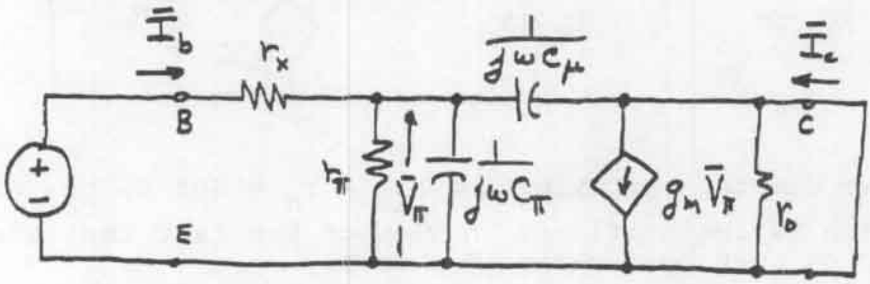
$$h_{oe} = i_c = \frac{1}{r_o} + g_m \frac{r_\pi}{r_\pi + r_\mu}$$

$$= \frac{1}{22.5 \times 10^3} + 0.385 \frac{585}{585 + 1.5 \times 10^6}$$

$$= 195\ \mu S$$

Problem 8.37

(a) The equivalent circuit is:



$$V_\pi = I_b \frac{1}{(1/r_\pi) + j\omega(C_\pi + C_\mu)}$$

Neglecting the current flowing through C_μ, we have

$$I_c = g_m V_\pi$$

Solving, we obtain

$$\frac{I_c}{I_b} = \frac{g_m r_\pi}{1 + j\omega r_\pi (C_\pi + C_\mu)}$$

(b) At the transition frequency f_t, we have

$$\left|\frac{I_c}{I_b}\right| = 1 = \frac{g_m r_\pi}{\sqrt{1 + 4\pi^2 f_t^2 r_\pi^2 (C_\pi + C_\mu)^2}}$$

Solving for f_t, we obtain

$$f_t = \frac{\sqrt{(g_m r_\pi)^2 - 1}}{2\pi r_\pi (C_\pi + C_\mu)}$$

However, rearranging Equation 8.47, we have $g_m r_\pi = \beta$. Thus, we have

$$f_t = \frac{\sqrt{\beta^2 - 1}}{2\pi r_\pi (C_\pi + C_\mu)} \cong \frac{\beta}{2\pi r_\pi (C_\pi + C_\mu)}$$

Problem 8.38

First, we use Equation 8.48 to compute the transconductance.

$$g_m = I_{CQ}/V_T = 1\text{mA}/26\text{mV} = 38.5 \text{ mS}$$

$$\beta = h_{fe} = 500$$

Then using Equation 8.38, we have

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{500 \times 0.026}{0.001} = 13 \text{ k}\Omega$$

Equation 8.41 yields

$$r_\mu \cong \frac{r_\pi}{h_{re}} = \frac{13 \times 10^3}{10^{-5}} = 1300 \text{ M}\Omega$$

We can use Equation 8.42 to find a value for r_o.

$$r_o \cong 1/h_{oe} = 50 \text{ k}\Omega$$

$$C_\mu = 2 \text{ pF}$$

$$C_\pi \cong \frac{\beta}{2\pi r_\pi f_t} - C_\mu = \frac{500}{2\pi \times 13 \times 10^3 \times 400 \times 10^6} - 2 \text{ pF}$$

$$C_\pi \cong 13.3 \text{ pF}$$

$$r_x C_\mu = 20 \times 10^{-12}$$

$$r_x = 10 \ \Omega$$

Problem 8.39

Equations 8.49 through 8.55 are:

$$R'_L = R_L || R_C || r_o \qquad R_B = R_1 || R_2 \qquad R'_s = r_\pi || [r_x + (R_B || R_s)]$$

$$A_{vb'} = V_o/V_\pi = -g_m R_L' \qquad C_T = C_\pi + C_\mu(1 + g_m R_L')$$

$$f_H = \frac{1}{2\pi R_s' C_T}$$

Thus, we see that increasing R_L increases R_L', does not effect R_s', increases the gain $A_{vb'}$, increases C_T, and ultimately decreases the half-power frequency f_H.

Problem 8.40

(a) $I_{BQ} = I_{CQ}/\beta = 100 = 10\ \mu A \quad R_B = (V_{CC} - V_{BEQ})/I_{BQ} = 1.43\ M\Omega$

$R_C = (V_{CC} - V_{CEQ})/I_{CQ} = 7\ k\Omega$

(b) $r_\pi = \beta V_T/I_{CQ} = 2600\ \Omega \qquad R_L' = R_L||R_C||r_o = 838\ \Omega$

$R_s' = r_\pi||[r_x + (R_B||R_s)] = 142\ \Omega$

$C_\pi \cong \dfrac{\beta}{2\pi r_\pi f_t} - C_\mu = 7.24\ pF \qquad g_m = \beta/r_\pi = 38.5\ mS$

$C_T = C_\pi + C_\mu(1 + g_m R_L') = 173\ pF$

$f_H = \dfrac{1}{2\pi R_s' C_T} = 6.48\ MHz$

In the midband, we have $R_{in} = R_B||r_\pi = 2.6\ k\Omega$, $A_v = -\beta R_L'/r_\pi = -32.2$, and $A_{vs} = A_v R_{in}/(R_s + R_{in}) = -31.0$.

Problem 8.41

(a) $I_{BQ} = I_{CQ}/\beta = 1.43\ \mu A$

$R_B = (V_{CC} - V_{BEQ})/I_{BQ} = 10.0\ M\Omega$

$R_C = (V_{CC} - V_{CEQ})/I_{CQ} = 7\ k\Omega$

(b) $r_\pi = \beta V_T/I_{CQ} = 18.2\ k\Omega \quad r_o \cong V_A/I_{CQ} = 50\ k\Omega$

$R'_L = R_L || R_C || r_o = 860\ \Omega$

$R'_s = r_\pi || [r_x + (R_B || R_s)] = 149\ \Omega$

$C_\pi \cong \dfrac{\beta}{2\pi r_\pi f_t} - C_\mu = 99\ \text{pF} \qquad g_m = \beta / r_\pi = 38.5\ \text{mS}$

$C_T = C_\pi + C_\mu(1 + g_m R'_L) = 201\ \text{pF}$

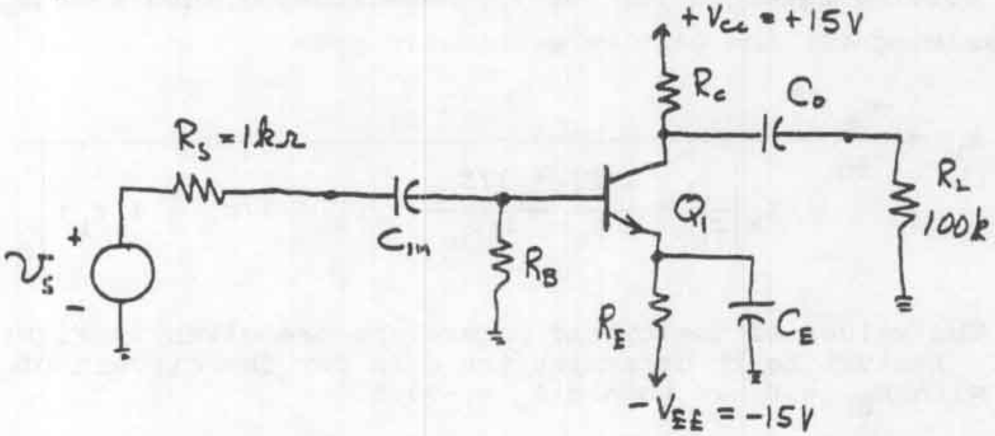
$f_H = \dfrac{1}{2\pi R'_s C_T} = 5.3\ \text{MHz}$

In the midband, we have $R_{in} = R_B || r_\pi = 18.2\ \text{k}\Omega$, $A_v = -\beta R'_L / r_\pi = -33.2$, and $A_{vs} = A_v R_{in}/(R_s + R_{in}) = -33.0 = 30.3$ dB.

(c) The simulation is stored in the file named P8_41 and yields A_{vs} = 29.4 dB and f_H = 5.9 MHz.

Problem 8.42

Many correct answers exist. We show an example.



The simulations of the two circuits are stored in the files named P8_42a and P8_42b. The resistance values and resulting midband gain in bandwidth are shown on the following page. Notice that the gain-bandwidth product is smaller for the high-impedance version of the circuit.

	$I_{CQ} \cong 1$ mA	$I_{CQ} = 10$ μA
R_B	200 kΩ	20 MΩ
R_C	6.8 kΩ	680 kΩ
R_E	13 kΩ	1.3 mΩ
A_{vsmid}	-184	-31.0
f_H	105 kHz	182 kHz

Problem 8.43

(a) Refer to the small-signal equivalent circuit shown in Figure 8.33 in the book. Replace the capacitances with open circuits. Then we can write voltage equations at nodes b′ and c.

$$\frac{v_\pi}{r_\pi} + \frac{v_\pi - v_{in}}{r_x} + \frac{v_\pi - v_o}{r_\mu} = 0 \qquad (1)$$

$$\frac{v_o}{R'_L} + g_m v_\pi + \frac{v_o - v_\pi}{r_\mu} = 0 \qquad (2)$$

Solving Equation (2) for v_o, substituting into Equation (1), and solving for the gain we eventually get

$$A_v = \frac{v_o}{v_{in}} = \frac{-1}{r_x\left[\frac{1}{r_\mu} + \frac{1/R'_L + 1/r_\mu}{g_m - 1/r_\mu}(1/r_\pi + 1/r_x + 1/r_\mu)\right]}$$

(b) The values of the hybrid parameters are given in Figure 8.31. Evaluating to determine the gain for the circuit of Figure 8.37 with $R_{EF} = 0$, we obtain $A_v = -93.9$.

(c) For the parameters shown in Figure 8.31 we have $\beta = 225$ and $r_\pi = 585$ Ω. Equations (4.44) and (4.47) yield

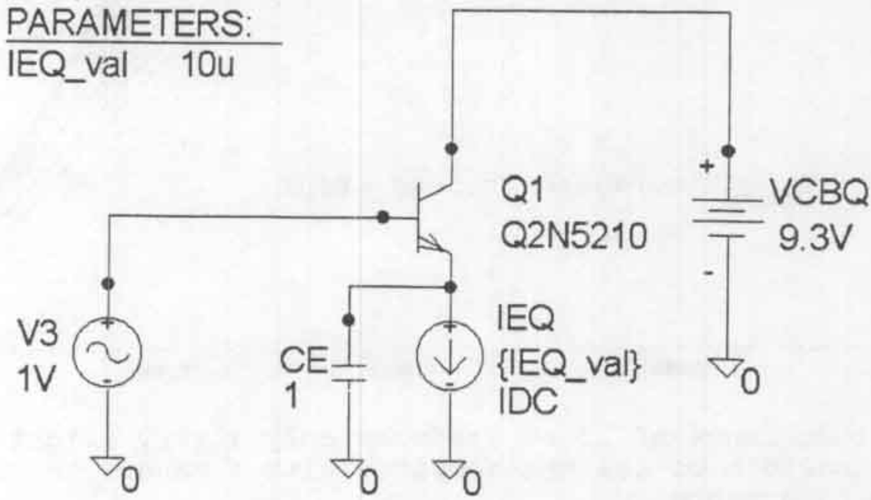
$$R'_L = R_L || R_C = \frac{1}{1/R_L + 1/R_C} = 255\ \Omega$$

$$A_v = \frac{v_o}{v_{in}} = -\frac{\beta R'_L}{r_\pi + (\beta + 1)R_{E1}} = \frac{225(255)}{585 + (226) \times 0} = -98.1$$

Considering that β may vary by a ratio of 3 to 1 from unit to unit and resistance tolerances, the difference between the two values for A_v are not significant.

Problem 8.44

The circuit diagram is:



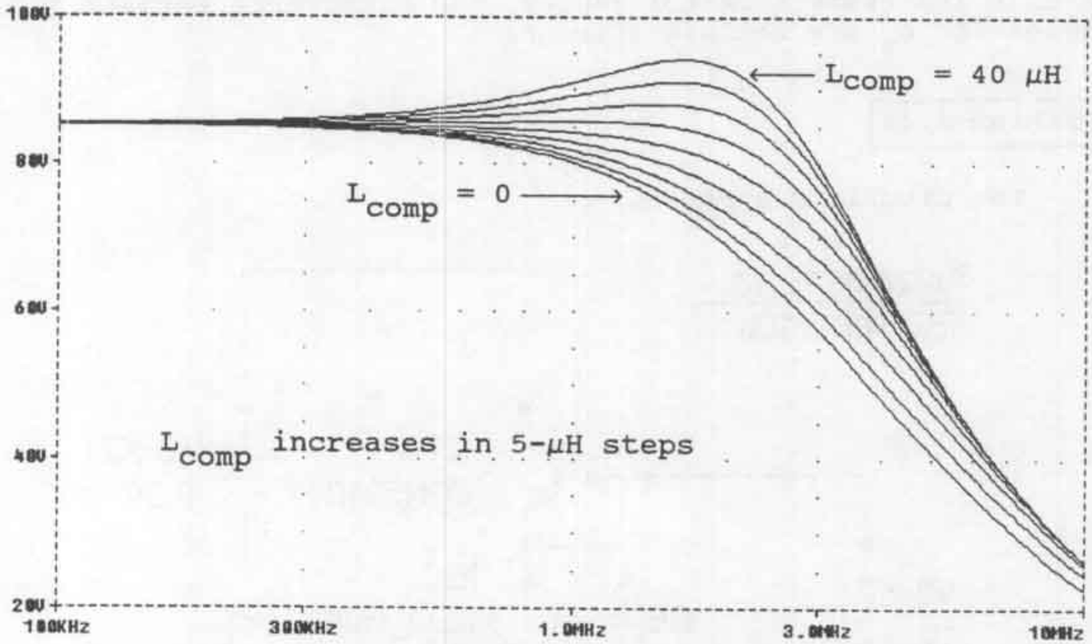
We have assumed that $I_{CQ} \cong I_{EQ}$ and that $V_{BEQ} \cong 0.7$ V. The simulation is stored in the file named P8_44. A parametric sweep is used to vary IEQ_val over the desired values and an ac sweep analysis is carried out for each bias current. Then we plot the current gain in dB and determine the frequency at which the current gain crosses 0 db.

I_{CQ}	f_t for 2N2222A	f_t for 2N5210
10 μA	1.6 MHz	3.1 MHz
100 μA	15 MHz	27 MHz
1 mA	110 MHz	150 MHz
10 mA	290 MHz	300 MHz

Results will vary depending on the models used for the transistors and on how precisely the bias points are established.

Problem 8.45

The simulation is stored in the file named P8_45. Plots of voltage gain magnitude versus frequency are shown below.



An inductance of 25 μH produces only a very slight peak and a 3-dB bandwidth of 4.2 MHz compared with a bandwidth of 2.7 MHz for zero inductance.

Problem 8.46

The common-base amplifier tends to have the lowest input resistance. The common-emitter and cascode amplifiers are inverting. To minimize feedback capacitance, we usually want to apply the input to the first transistor and take the output from the second transistor in an emitter-coupled pair, in which case this amplifier is noninverting. The common-base amplifier and emitter follower are noninverting. The frequency response of the common-emitter amplifier is limited to the greatest degree by the Miller effect.

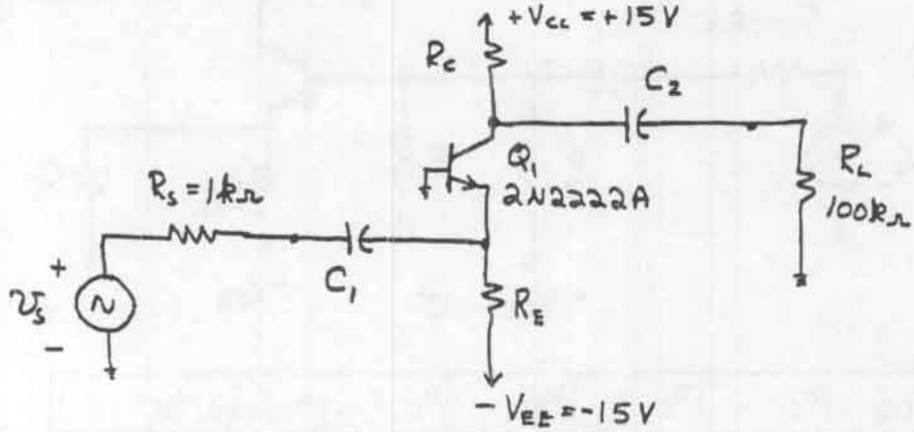
Problem 8.47

Usually, a common-base amplifier is unsuitable with a source with a high internal impedance because the input impedance of the common-base amplifier tends to be low and loading effects would be extreme.

Problem 8.48

See Figure 8.40 in the book.

Problem 8.49



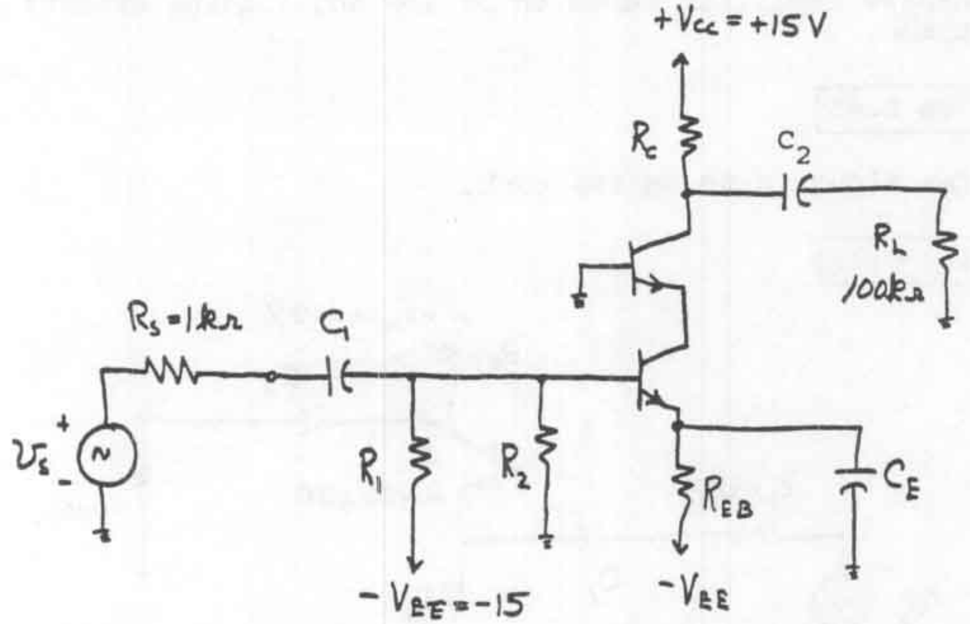
Many correct choices exist for component values. We used 1 μF for each of the coupling capacitors, because the low-frequency region is not of interest in this problem. The following table gives choices of component values and results of the PSpice simulations for both Q points.

I_{CQ}	R_E	R_C	A_{vsmid}	f_H
1 mA	15 kΩ	5.6 kΩ	+5.1	3.9 MHz
10 μA	1.5 MΩ	560 kΩ	+22.6	248 kHz

The simulations are stored in P8_49a and P8_49b. The model for the 2N2222A is stored in the Device.lib file. Results will vary depending on the model used.

Problem 8.50

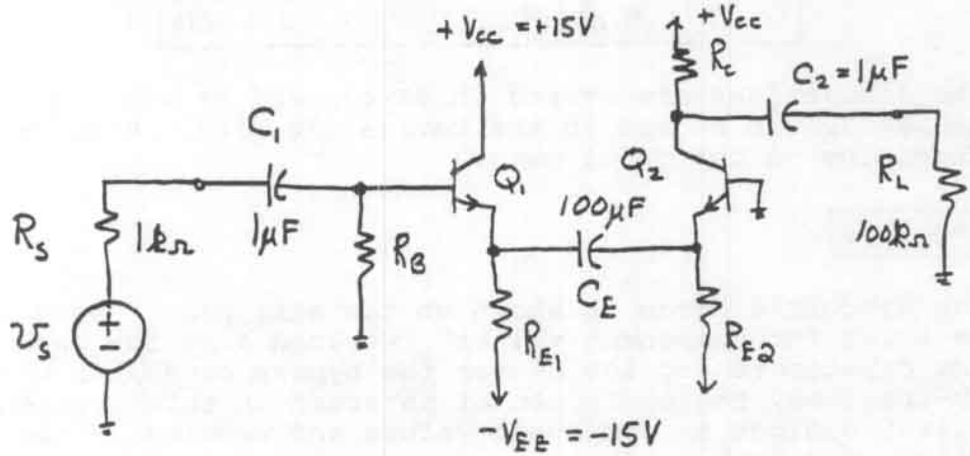
The circuit diagram is shown on the next page. Many correct choices exist for component values. We used 1 μF for each of the coupling capacitors and 100 μF for the bypass capacitor because the low-frequency region is not of interest in this problem. The table gives choices of component values and results of the PSpice simulations for both Q points.



I_{CQ}	R_1	R_2	R_{EB}	R_C	A_{vsmid}	f_H
1 mA	51 kΩ	100 kΩ	4.3 kΩ	5.6 kΩ	-157	2.2 MHz
10 μA	5.1 MΩ	10 MΩ	430 kΩ	560 kΩ	-31	240 kHz

The simulations are stored in P8_50a and P8_50b. The model for the 2N2222A is stored in the Device.lib file. Results will vary depending on the model used.

Problem 8.51



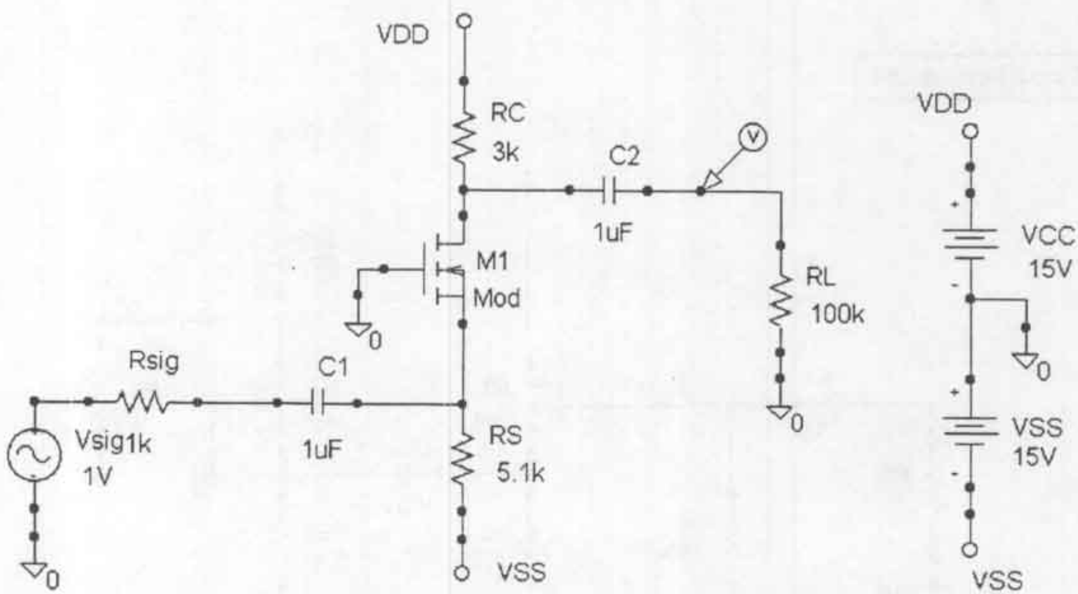
Many correct choices exist for component values. We used $C_1 = C_2 = 1\ \mu F$ and $C_E = 100\ \mu F$ because the low-frequency region is not of interest in this problem. The following table gives choices of component values and results of the PSpice simulations for both Q points.

I_{CQ}	R_B	R_{E1}, R_{E2}	R_C	A_{vsmid}	f_H
1 mA	150 kΩ	15 kΩ	5.6 kΩ	+83	2.4 MHz
10 μA	15 MΩ	1.5 MΩ	560 kΩ	+14.7	250 kHz

The simulations are stored in P8_51a and P8_51b. The model for the 2N2222A is stored in the Device.lib file. Results will vary depending on the model used.

Problem 8.52

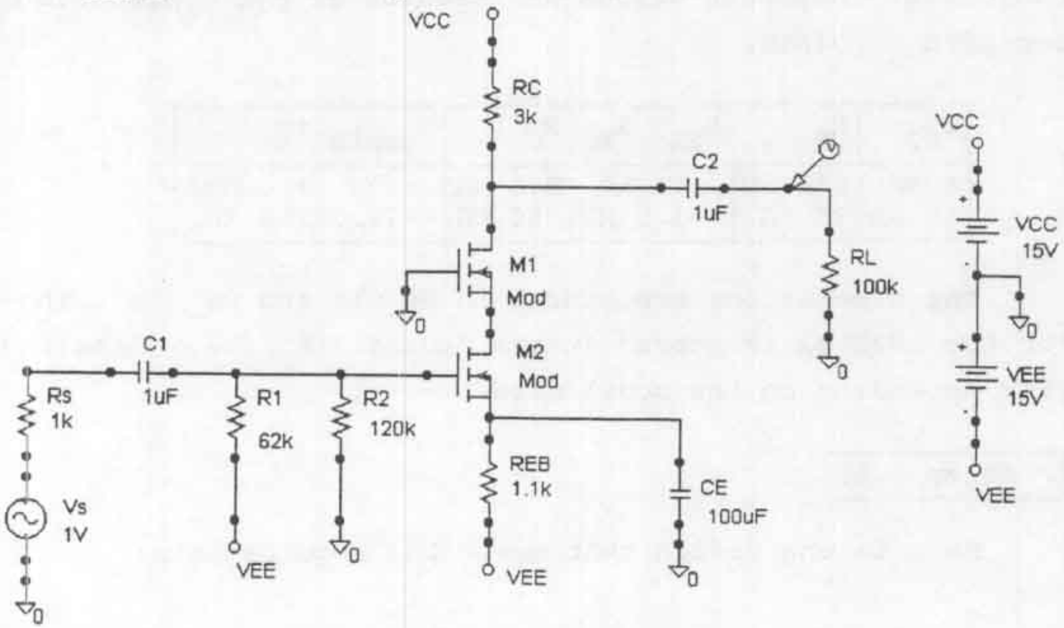
Here is one design that meets the requirements:



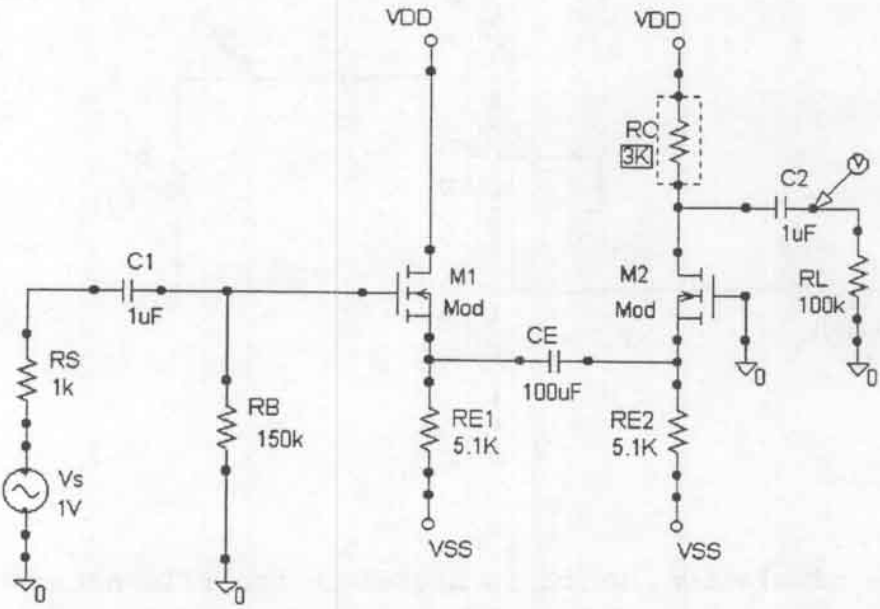
The simulation, which is stored in the file named P8_52, yields $A_{vsmid} = 2.1$ and $f_H = 110$ MHz.

Problem 8.53

The simulation, which is stored in the file named P8_53, yields $A_{vsmid} = 9.2$ and $f_H = 65$ MHz.



Problem 8.54



The simulation, which is stored in the file named P8_54, yields $A_{vsmid} = 4.4$ and $f_H = 93$ MHz.

Problem 8.55

In the midband, the input current to the amplifier is $i_{in} = v_s/(R_s + R_i)$ in which R_s is the internal source resistance (500 Ω) and R_i is the input resistance of the amplifier. The output current is $i_o = v_o/R_L$. Thus the current gain is required to be

$$A_i = i_o/i_{in} = A_v(R_s + R_i)/R_L$$

$$= 10(500 + R_i)/500 = 10 + R_i/50$$

Thus the most suitable configurations are those that can achieve current and voltage gains that are both large compared to unity. Furthermore, to achieve wide bandwidth, configurations that minimize feedback capacitance are more suitable than those configurations that have substantial feedback capacitance.

(a) The common-base stage has a very low input impedance (tens of ohms for bias currents on the order of one mA). Furthermore, its current gain is less than unity. Thus, a common-base stage will have difficulty meeting the desired specifications.

(b) The common-emitter amplifier is suitable from the standpoint of the gains required, because it can achieve high voltage and current gains (compared to unity). However, its bandwidth is adversely affected by the Miller effect.

(c) The differential amplifier is suitable, because it can achieve high voltage and current gains (compared to unity). Furthermore this configuration minimizes feedback capacitance.

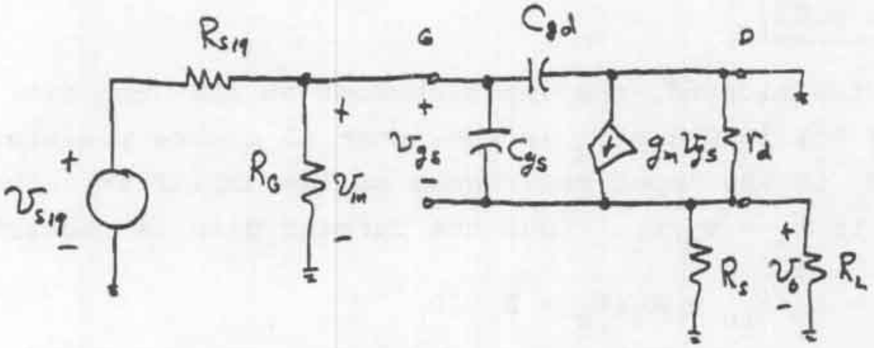
(d) The cascode amplifier is suitable because it can achieve high voltage and current gains (compared to unity). Furthermore this configuration minimizes feedback capacitance.

(e) The emitter follower is not suitable because its voltage gain is less than unity.

(f) An emitter follower cascaded with a common-emitter amplifier is a good choice because it can achieve large current and voltage gain and has very small feedback capacitance.

Problem 8.56

The high-frequency equivalent circuit is shown on the next page.

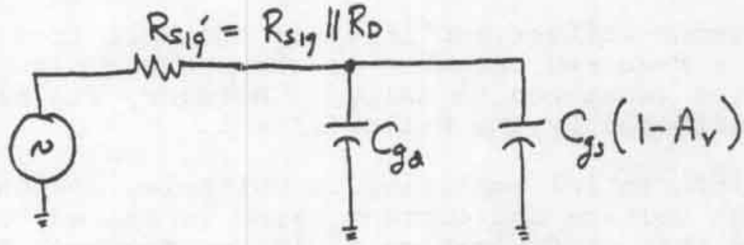


Equation 5.48 in the book gives the midband voltage gain as

$$A_v = \frac{v_o}{v_{in}} = \frac{g_m R_L'}{1 + g_m R_L'} \quad \text{where } R_L' = r_d || R_S || R_L$$

However $A_{vs} = A_v R_G/(R_{sig} + R_G)$.

Using the Miller effect and replacing v_{sig}, R_{sig}, and R_G with a Thévenin equivalent, we obtain the following equivalent input circuit.



This is a first-order lowpass filter having

$$f_H = \frac{1}{2\pi R_{sig}'[C_{gd} + C_{gs}(1 - A_v)]}$$

Evaluating for the parameters given in the problem we obtain

$R_L' = 1333\ \Omega$ $\qquad R_{sig}' = 4.98\ \text{k}\Omega$

$A_v \cong A_{vs} \cong 0.87$ $\qquad f_H = 56.5\ \text{MHz}$

Problem 8.57

This problem is similar to Example 8.10.

$I_{CQ} \cong I_{EQ} = 1$ mA $\quad r_\pi = \beta V_T/I_{CQ} = 150(0.026)/10^{-3} = 3900\ \Omega$

$$f_t \cong \frac{\beta}{2\pi r_\pi (C_\mu + C_\pi)} \quad \Rightarrow \quad C_\pi = 7.2 \text{ pF}$$

$$R_L' = r_o || R_L = 990\ \Omega \qquad A_v = \frac{(\beta + 1)\ R_L'}{r_\pi + (\beta + 1)\ R_L'} = 0.975$$

$$R_{in} = R_B || [r_\pi + (\beta + 1) R_L'] = 60.5 \text{ k}\Omega$$

$$A_{vs} = \frac{v_o}{v_s} = A_v \frac{R_{in}}{R_s + R_{in}} = 0.367$$

$$g_m = I_{CQ}/V_T = 38.5 \text{ mS} \qquad C_T = C_\mu + \frac{C_\pi}{1 + g_m R_L'} = 5.18 \text{ pF}$$

$$R_T = [r_x + (R_s || R_B)] || [r_\pi (1 + g_m R_L')] = 37.7 \text{ k}\Omega$$

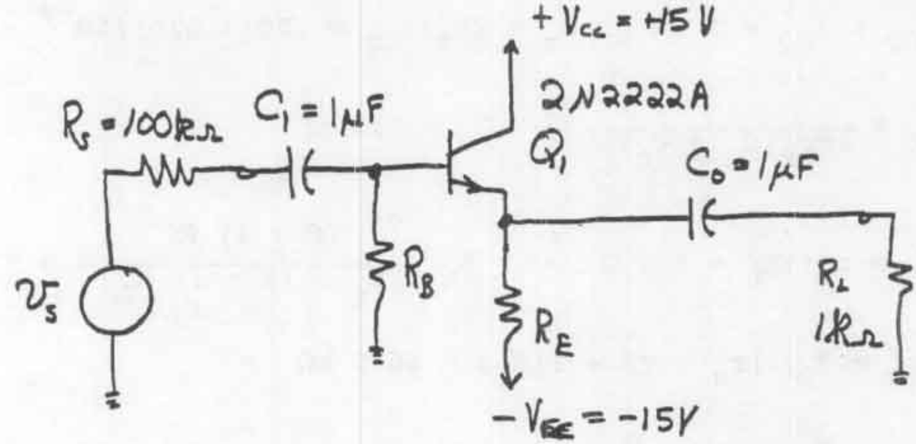
$f_H = \dfrac{1}{2\pi R_T C_T} = 815$ kHz This the upper half-power frequency for A_{vs}. For A_v we assume $R_s = 0$ and recompute R_T and f_H. The upper half-power frequency for A_v is $f_H = 1.02$ GHz.

Problem 8.58

See the circuit diagram on the next page. Many correct choices exist for component values. We used 1 μF for each of the coupling capacitors because the low-frequency region is not of interest in this problem. The following table gives choices of component values and results of the PSpice simulations for both Q points.

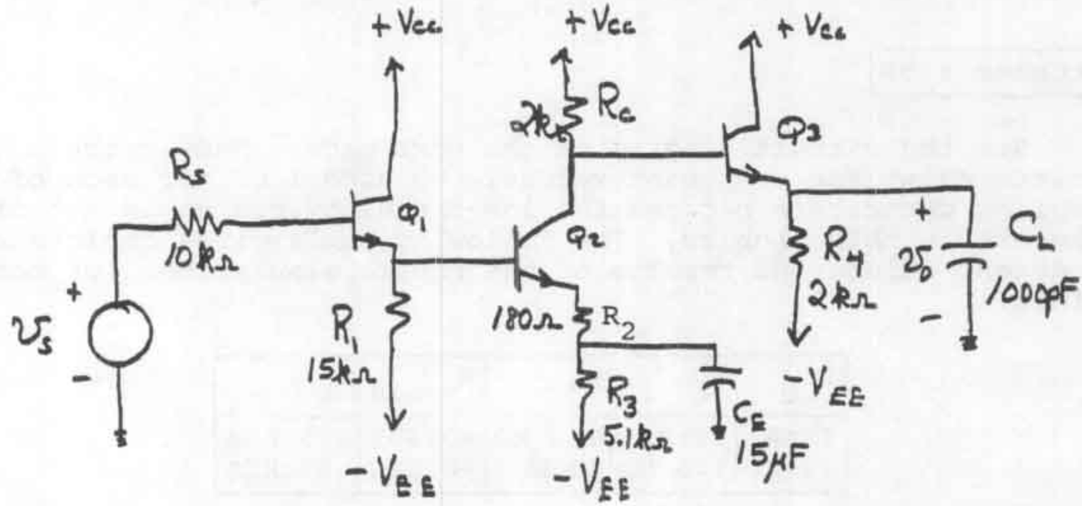
I_{CQ}	R_E	R_B	A_{vsmid}	f_H
1 mA	13 kΩ	150 kΩ	+0.435	455 kHz
10 μA	1.3 MΩ	13 MΩ	+0.22	69 kHz

The simulations are stored in P8_58a and P8_58b. The model for the 2N2222A is stored in the Device.lib file. Results will vary depending on the model used.



Problem 8.59

We elected to cascade three stages. First an emitter-follower to provide high input impedance and low source impedance for the second stage. The second stage is a common-emitter with a partially unbypassed emitter resistor to provide the desired voltage gain. The final stage is an emitter follower providing the low output impedance needed to drive the load capacitance at high frequencies. To reduce the number of components required we use direct coupling. The circuit is:



Simulations (stored in the file named P8_59) show that this circuit meets the desired specifications.

Problem 8.60

Coupling capacitors are used to isolate the dc bias points of cascaded stages, prevent dc components in the signal source from affecting the bias point of the first stage, and to prevent dc from being applied to the load.

Bypass capacitors are used to ground points in a circuit for ac signals but not for dc signals.

Coupling and bypass capacitors are common in discrete circuits but usually are not practical in integrated circuits.

Problem 8.61

The break frequency for each capacitor is $f_{break} = 1/(2\pi RC)$ where R is the total equivalent resistance in series with the capacitor.

Problem 8.62

Each coupling capacitor in an RC-coupled amplifier contributes a 20 dB/decade decline in gain at low frequencies.

Problem 8.63

1. Eliminate any capacitors that are not essential.

2. Determine the resistance in series with each coupling capacitor and the resistance seen by each bypass capacitor. Treat all of the other capacitors as short circuits in determining the resistances. The break frequencies, capacitances values and resistances are related by $f_{break} = 1/(2\pi RC)$ where R is the resistance in series with the capacitance. If practical, redesign the circuit to increase the resistances so smaller capacitances can be used.

3. Decide how to budget the desired lower half-power frequency between the various break frequencies using the approximation that the lower half-power frequency equals the sum of the break frequencies.

4. Use the resistances found in Step 2 and the break frequencies selected in Step 3 to compute capacitance values.

5. Select standard capacitance values sufficiently large to allow for component tolerances.

Problem 8.64

Assuming that the other capacitors are short circuits the resistance in series with C_1 is $R_s + R_{in}$ in which $R_{in} = r_\pi || R_B$ is the midband input resistance of the amplifier. In Example 8.8 we found that $R_{in} = 553\ \Omega$. Thus we have:

$$f_{B1} = 1/[2\pi C_1(R_s + R_{in})] = 264 \text{ Hz}$$

The output resistance of the amplifier is

$$R_o = r_o || R_C = (22.5 \text{ k}\Omega)||(510\ \Omega) = 499\ \Omega$$

$$f_{B2} = 1/[2\pi C_2(R_o + R_L)] = 160 \text{ Hz}$$

The midband resistance seen by the bypass capacitor is

$$R'_E = R_{E2} || \left[\frac{r_\pi + R_B || R_s}{(\beta + 1)}\right] = 1300 || \left[\frac{585 + 10^4 || 50}{(225 + 1)}\right] \cong 2.8\ \Omega$$

$$f_E = 1/(2\pi C_E R'_E) = 567 \text{ Hz}$$

Now we estimate the lower half-power frequency as

$$f_L = f_1 + f_2 + f_E = 991 \text{ Hz}$$

The file for simulating this circuit is P8_64. The results of the simulation yield $f_L = 848$ Hz. This is good agreement given the uncertainty about transistor parameters such as β.

Problem 8.65

Assuming that the other capacitors act as short circuits, the resistance in series with C_1 is

$$R_s + r_{\pi 1} || R_1 || R_2 = 50 + 585 || (6.8 \text{ k}\Omega) || (10 \text{ k}\Omega) = 561\ \Omega$$

Then for a break frequency of 10 Hz we have

$$C_1 = 1/(2\pi f_1 561) = 1/(2\pi 10 \times 561) = 28.4\ \mu\text{F}$$

Similarly,

$$C_2 = 1/[2\pi f_2(R_C + R_L)] = 1/(2\pi 10 \times 1020) = 15.6\ \mu F$$

Looking back from C_E, Q_1 acts as an emitter follower. The resistance seen by C_E is

$$R'_E = R_E || \left[\frac{r_\pi + R_1||R_2||R_s}{(\beta + 1)}\right] = 2.79\ \Omega$$

$$C_E = 1/(2\pi f_3 R'_E) = 5700\ \mu F$$

We estimate the lower half-power frequency as $f_L = f_1 + f_2 + f_3 = 30$ Hz. The simulation file is P8_65. The simulation gives $f_L = 23.6$ Hz. Actually, the assumption that $f_L = f_1 + f_2 + f_3$ is an approximation that gives a value higher than the true value. Thus, the capacitances computed using this assumption are too high. However, considering component tolerances, the approximate results are sufficiently accurate.

Problem 8.66

First, we consider the break frequency due to C_1, assuming that the other capacitances are short circuits. We need to find the resistance in series with C_1. We have $r_{\pi 1} = r_{\pi 2} = \beta V_T/I_{CQ} = 585\ \Omega$. The resistance seen looking into the emitter of Q_2 is $r_{e2} = r_{\pi 2}/(\beta_2 + 1) = 2.59\ \Omega$. This resistance in parallel with R_{E1} and R_{E2} acts as an unbypassed emitter resistance for Q_1. Thus, the input resistance of the amplifier is

$$R_{in} = R_B || r_{\pi 1} + (\beta + 1)(R_{E1} || R_{E2} || r_{e2}) = 1168\ \Omega$$

$$C_1 = 1/(2\pi f_1 1168) = 1/(2\pi 10 \times 1168) = 13.6\ \mu F$$

The resistance in series with C_2 is $R_C + R_L = 1020\ \Omega$. Thus we have

$$C_2 = 1/(2\pi f_2 1168) = 1/(2\pi 10 \times 1020) = 15.6\ \mu F$$

The resistance in series with C_E is the sum of the resistances seen looking to the right and to the left from the respective terminals of C_E. Looking to the right, the resistance is $R_{E2}||r_{e2} = 1300||2.59 = 2.58\ \Omega$. Looking to the left, Q_1 has the configuration of an emitter follower and its output resistance is $R_{E2}||[(r_\pi + R_s||R_B)/(\beta + 1)] = 2.80\ \Omega$. Thus the total resistance in series with C_E is $2.58 + 2.80 = 5.38\ \Omega$. The required capacitance is

$$C_E = 1/(2\pi f_3 5.38) = 1/(2\pi 10 \times 5.38) = 2960\ \mu F$$

We estimate the lower half-power frequency as $f_L = f_1 + f_2 + f_3 = 30$ Hz. The simulation file is P8_66. The simulation gives $f_L = 25$ Hz. Actually, the assumption that $f_L = f_1 + f_2 + f_3$ is an approximation that gives a result higher than the true value. Thus, the capacitances computed using this assumption are too high. However, considering component tolerances, the approximate results are sufficiently accurate.

Problem 8.67

In Example 8.10, we established that $r_\pi = 585\ \Omega$ and $\beta = 225$. The midband input impedance of the emitter follower is given by Equations (4.59) and (4.60).

$$R'_L = R_E||R_L = 48.15\ \Omega$$

$$Z_{it} = \frac{v_{in}}{i_b} = r_\pi + (1 + \beta)R'_L = 11.47\ k\Omega$$

$$Z_i = \frac{1}{1/R_B + 1/Z_{it}} = 5.342\ k\Omega$$

The resistance in series with C_1 is $R_{series1} = R_s + Z_i = 5.852\ k\Omega$. Thus the break frequency associated with C_1 is

$$f_1 = 1/(2\pi C_1 R_{series1}) = 27.2\ Hz$$

The output resistance is given by Equations (4.63) and (4.65) with $R_B = R_1 || R_2$.

$$R'_s = R_s || R_B = 485\ \Omega$$

$$R_o = \frac{v_x}{i_x} = \frac{1}{\dfrac{1+\beta}{R'_s + r_\pi} + \dfrac{1}{R_E}} = 4.72\ \Omega$$

The resistance in series with C_2 is $R_{series2} = R_o + R_L = 54.7\ \Omega$. Thus the break frequency associated with C_2 is

$$f_2 = 1/(2\pi C_2 R_{series2}) = 29.0\ \text{Hz}$$

We estimate the lower half-power frequency as $f_L = f_1 + f_2 =$ 56.2 Hz. The simulation file is P8_67. The simulation gives f_L = 49 Hz. Actually, the assumption that $f_L = f_1 + f_2$ is an approximation that gives a result higher than the true value. Thus, capacitances computed using this assumption are too high. However, considering component tolerances, the approximate results are sufficiently accurate.

Chapter 9

Exercise 9.1

$$A_f = \frac{x_o}{x_s} = \frac{A}{1 + A\beta} = \frac{10^5}{1 + 10^5 \times 0.01} = 99.9$$

$$x_o = A_f x_s = 499.5\sin(2000\pi t)$$

$$x_f = \beta x_o = 4.995 \sin(2000\pi t)$$

$$x_i = x_x - x_f = 0.005\sin(2000\pi t)$$

Exercise 9.2

Equation 9.2 states

$$\frac{dA_f}{A_f} = \frac{dA}{A} \frac{1}{(1 + A\beta)}$$

(a) We have $\left|\frac{dA}{A}\right| \cong \left|\frac{\Delta A}{A}\right| = 0.1$ (i.e., the tolerance for A is ±10%) and we want $|\Delta A_f/A_f| < 0.01$ (i.e., ±1% tolerance). Thus we need $0.01 = 0.1/(1 + A\beta_{min})$, which implies that $1 + A\beta_{min} = 10$ and the maximum closed loop gain is $A_{fmax} = A/(1 + A\beta_{min}) = 10^5/10 = 10^4$.

(b) Similarly we determine that a 0.1% tolerance for A_f requires $A_{fmax} = 10^3$.

Exercise 9.3

See Figure 9.6 on page 562 in the book.

Exercise 9.4

Recall that $A_f \cong 1/\beta$. Therefore change the values of R_1 and/or R_2 so that $\beta = R_2/(R_1 + R_2) = 1/20$. One possible combination of values is $R_1 = 19\ k\Omega$ and $R_2 = 1\ k\Omega$.

Exercise 9.5

Here the feedback ratio is $R_2/(R_1 + R_2) = 10^{-3}$ and we have $A\beta \cong 1$. The SPICE simulation (which is stored in the file named Exer9_5) shows that the output waveform is distorted. For negative feedback to be effective in reducing distortion, we must have $A\beta >> 1$.

Exercise 9.6

(a) $SNR = 20\log(V_s/V_{noise}) = 20\log(10/0.1) = 40$ dB

(b) Equation 9.17 shows that the SNR is improved by the factor A_2^2. Since we want to improve the SNR by a factor of 100 (equivalent to 20 dB) we require $A_2 = 10$.

Exercise 9.7

Refer to Figure 9.16 in the book. We can write:

$$i_s = i_i + i_f = v_s/R_i + \beta x_o \qquad x_o = Ai_i = Av_s/R_i$$

$$i_s = v_s/R_i + A\beta v_s/R_i \qquad R_{if} = v_s/i_s = R_i/(1 + A\beta)$$

Exercise 9.8

Refer to Figure 9.18 in the book.

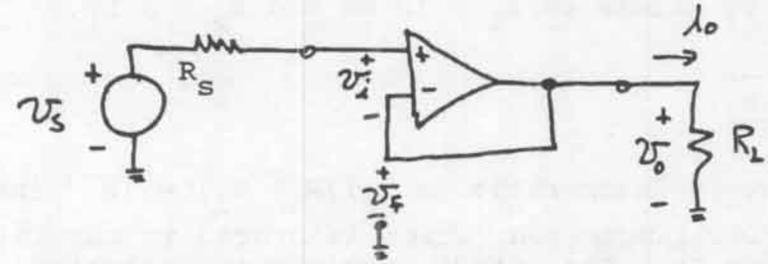
$$i_{test} = v_{test}/R_o - A_{sc}x_{in} \qquad x_{in} = \beta i_{test}$$

$$i_{test} = v_{test}/R_o - A_{sc}\beta i_{test}$$

$$R_{of} = v_{test}/i_{test} = R_o(1 + A_{sc}\beta)$$

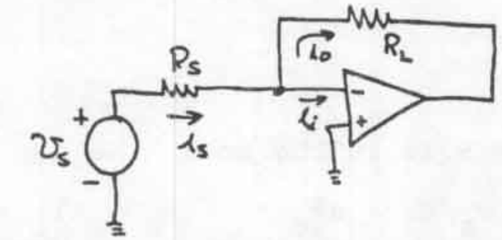
Exercise 9.9

(a) Answers: Negative series voltage feedback, $\beta = 1$, ideal voltage amplifier, $A_{vf} = 1$, $R_{if} = \infty$, and $R_{of} = 0$.



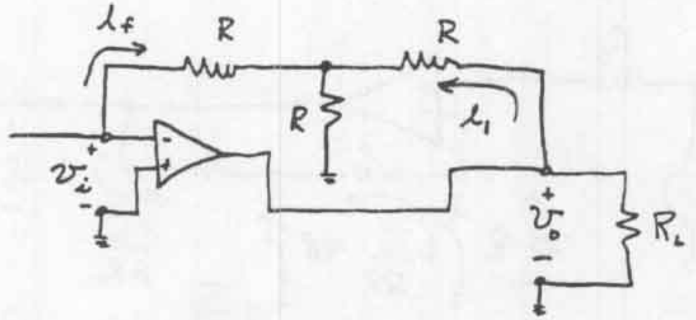
Notice that if we replace R_L with a short circuit, we have no feedback, therefore we have voltage feedback. The feedback connection is to the inverting input terminal (and the feedback network is noninverting) therefore the feedback is negative. We have $v_f = v_o$ so $\beta = 1$. We have series feedback because v_s, v_i and v_o are in series. Negative series voltage feedback tends to produce an ideal voltage amplifier with $R_{if} = \infty$, $R_{of} = 0$ and $A_{vf} = 1/\beta = 1$.

(b) Answers: Negative parallel current feedback, $\beta = 1$, ideal current amplifier, $A_{if} = 1$, $R_{if} = 0$, $R_{of} = \infty$.



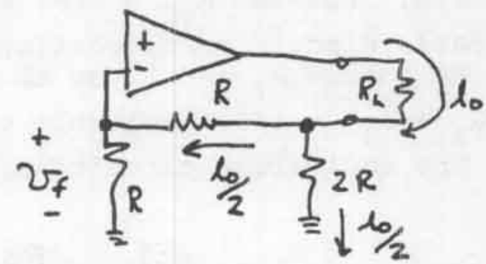
Notice that if R_L is open circuited, the feedback path is broken. Therefore, we have current feedback. Because the feedback path is connected to the inverting input terminal the feedback is negative. Notice that $i_i = i_s - i_o$ so we have $\beta = 1$. The feedback network, output terminals, the source, and the amplifier input terminals are in parallel. Negative parallel current feedback tends to produce an ideal current amplifier with $R_{if} = 0$, $R_{of} = \infty$, and $A_{if} = 1/\beta = 1$.

(c) Answers: Negative parallel voltage feedback, $\beta = -1/3R$, ideal transresistance amplifier, $R_{mf} = -3R$, $R_{if} = 0$, and $R_{of} = 0$.



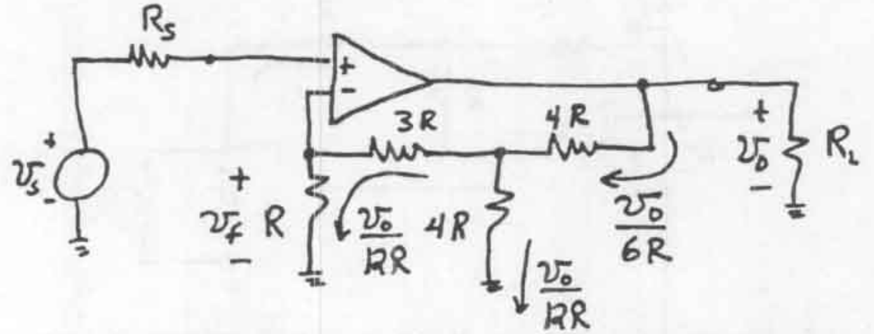
Notice that if we replace R_L with a short circuit, we have no feedback, therefore we have voltage feedback. The feedback connection is to the inverting input terminal (and the feedback network is noninverting) therefore the feedback is negative. Because the feedback output is in parallel with the amplifier input terminals and with the source, we have parallel feedback. In finding β, assume $v_i = 0$. Then $i_1 = v_o/(3R/2)$ and $i_f = -(1/2)i_1 = -v_o/(3R)$. Therefore $\beta = -1/3R$. Negative parallel voltage feedback tends to produce an ideal transresistance amplifier with $R_{if} = 0$, $R_{of} = 0$, and $R_{mf} = 1/\beta = -3R$.

(d) Answers: Negative series current feedback, $\beta = R/2$, ideal transconductance amplifier, $G_{mf} = 2/R$, $R_{if} = \infty$, and $R_{of} = \infty$.



Because the output of the feedback network is in series with the amplifier input terminals and because the feedback becomes zero for an open circuit load, we have series current feedback. Because the feedback connection is to the inverting input terminal, the feedback is negative. Assuming $i_i = 0$, we have $v_f = i_o(R/2)$, thus $\beta = R/2$. Negative series current feedback tends to produce an ideal transconductance amplifier with $R_{if} = \infty$, $R_{of} = \infty$, and $G_{mf} = 1/\beta = 2/R$.

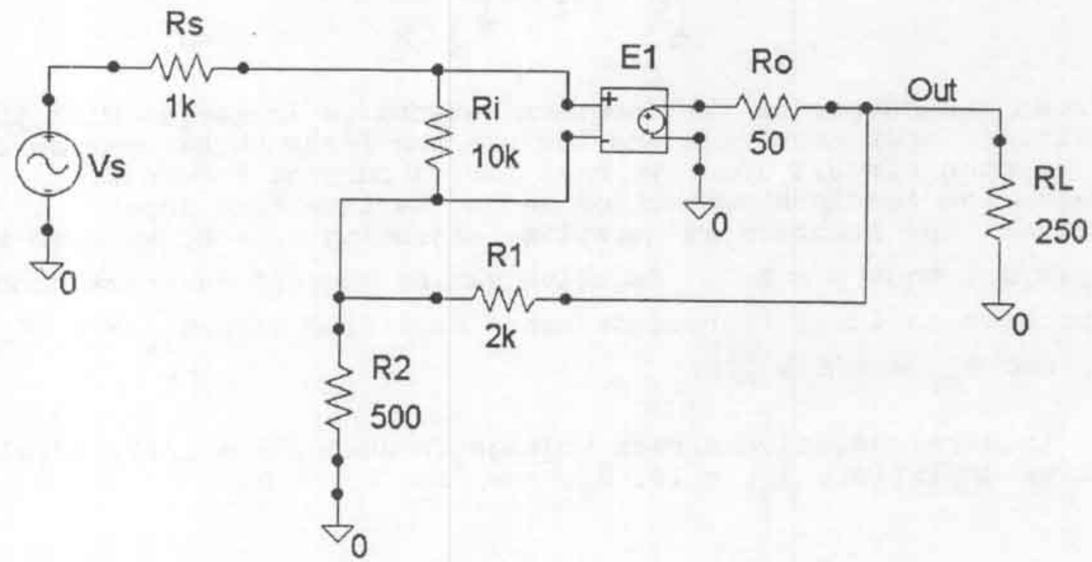
(e) Answers: Negative series voltage feedback, $\beta = 1/12$, ideal voltage amplifier, $A_{vf} = 12$, $R_{if} = \infty$, and $R_{of} = 0$.



Because the output of the feedback network is in series with the amplifier input terminals and because the feedback becomes zero for a short-circuit load, we have series voltage feedback. Because the feedback connection is to the inverting input terminal, the feedback is negative. Assuming $i_i = 0$, we have $v_f = v_o/12$, thus $\beta = 1/12$. Negative series voltage feedback tends to produce an ideal voltage amplifier with $R_{if} = \infty$, $R_{of} = 0$, and $A_{vf} = 1/\beta = 12$.

Exercise 9.10

To obtain a nearly ideal voltage amplifier, use negative series voltage feedback. Because $A_{vf} \cong 1/\beta$, we need to design for $\beta = 1/5$. A suitable circuit configuration is shown in Figure 9.19a on page 578. We choose R_1 and R_2 so that $R_2 << R_i$, $R_1 + R_2 >> R_{of}$ and $\beta = R_2/(R_1 + R_2) = 1/5$. Suitable choices are $R_1 = 2$ kΩ and $R_2 = 500$ Ω. The equivalent circuit is:



We setup a transfer function analysis with Vs as the input source and Out as the output terminal. After running the simulation we find the following in the output file:

V(Out)/V_Vs = 4.998E+00

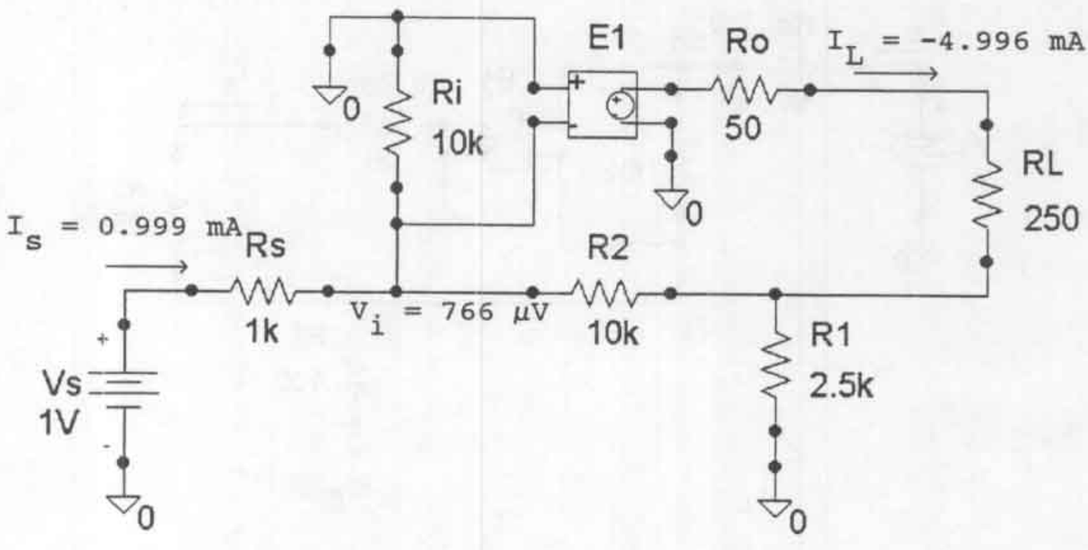
INPUT RESISTANCE AT V_Vs = 2.460E+07

OUTPUT RESISTANCE AT V(Out) = 1.899E-02

Actually the input resistance reported by PSpice is $R_s + R_{if}$ but R_s is negligible compared to R_{if}. Also the output resistance reported by PSpice is R_L in parallel with R_{of} but this is not significant because $R_{of} << R_L$.

Exercise 9.11

Use the configuration of Figure 9.19d with $R_2 = 4R_1$. To avoid excessive loading, we want to select values so that $R_2 >> R_i$ and so that $R_1 << R_o + R_L$. It is not possible to meet all of these objectives, and we must compromise. One reasonable choice is R_2 = 10 kΩ and R_1 = 2.5 kΩ. For this choice, the SPICE simulation shows that A_{if} = -5.00, R_{if} = 0.767 Ω, and R_{of} = 2.54 MΩ. The circuit configuration is:



We ran an operating point analysis and displayed the currents and voltages on the circuit diagram in Schematics some of which are shown above. (The simulation is stored in the file named Exer9_11a.) Then we computed the current gain and input impedance.

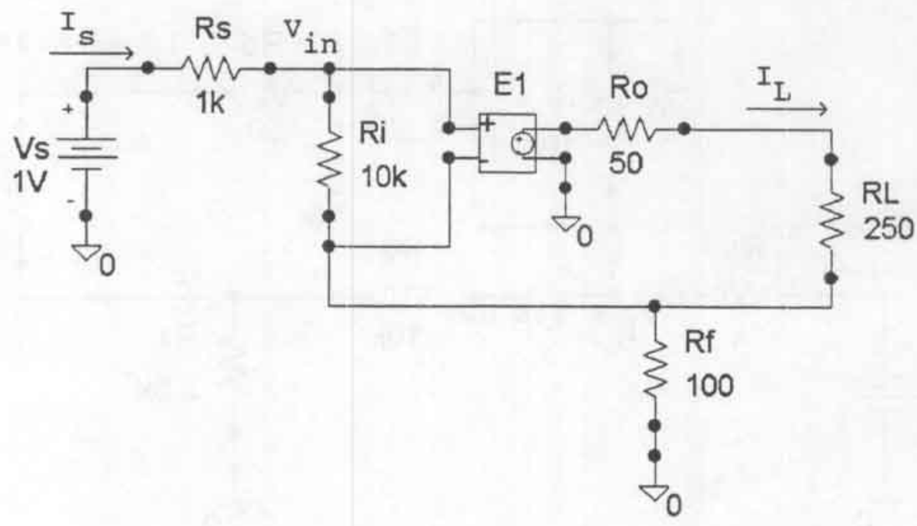
$$A_{if} = I_L/I_s = -4.996/0.999 = -5.00$$
$$R_{if} = V_i/I_s = 0.766\ \Omega$$

To determine the output resistance we set V_s = 0 and replaced R_L with a test source. The simulation is stored in the file named Exer9_11b. The results of the operating point analysis were then used to compute the output resistance as R_{of} = 2.54 MΩ

Exercise 9.12

To attain a nearly ideal transconductance amplifier, we use negative series current feedback as shown in Figure 9.19b in the book. We require $\beta = R_f = 1/G_{mf} = 100\ \Omega$. The circuit configuration is shown below. We ran an operating point analysis, displayed the voltages and currents on the circuit diagram, and calculated the gain and input impedance.

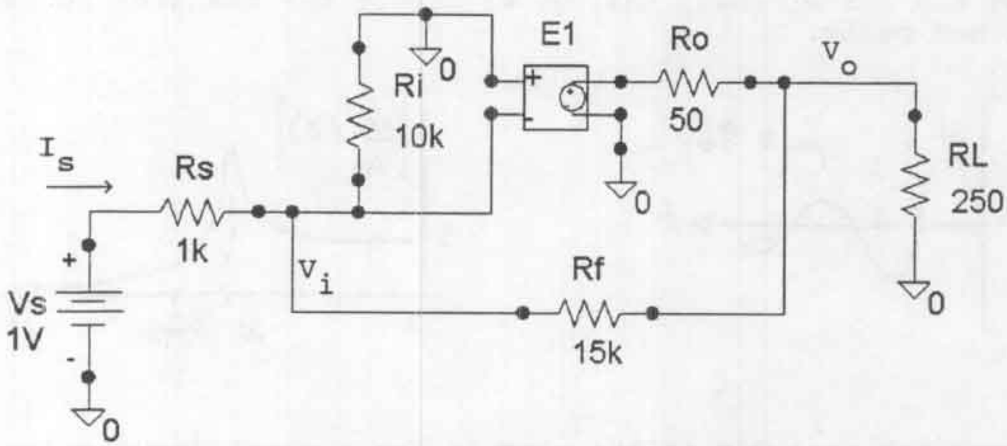
$G_{mf} = I_L/V_i = 0.01$ S $\qquad R_{if} = I_s/V_{in} = 37.5$ MΩ



Next we set $V_s = 0$, replaced R_L by a 1-V test source, ran an operating-point analysis, and used the results to compute $R_{of} = 1.35$ MΩ. The simulation files are Exer9_12a and Exer9_12b.

Exercise 9.13

To attain a nearly ideal transresistance amplifier, we use negative series current feedback as shown in Figure 9.19c in the book. We require $\beta = -1/R_f = 1/R_{mf}$. Thus we need $R_f = R_{mf} = 15$ kΩ. The circuit configuration is shown below.



We ran an operating-point analysis, displayed the voltages and currents on the circuit diagram, and calculated the gain and input impedance.

$$R_{mf} = V_o/I_s = 14.99 \text{ k}\Omega \qquad R_{if} = V_i/I_s = 1.20\ \Omega$$

Next we set $V_s = 0$, replaced R_L by a 1-V test source, ran an operating-point analysis, and used the results to compute $R_{of} = 0.0583\ \Omega$. The simulation files are Exer9_13a and Exer9_13b.

Exercise 9.14

Refer to the circuit diagrams shown in the book.

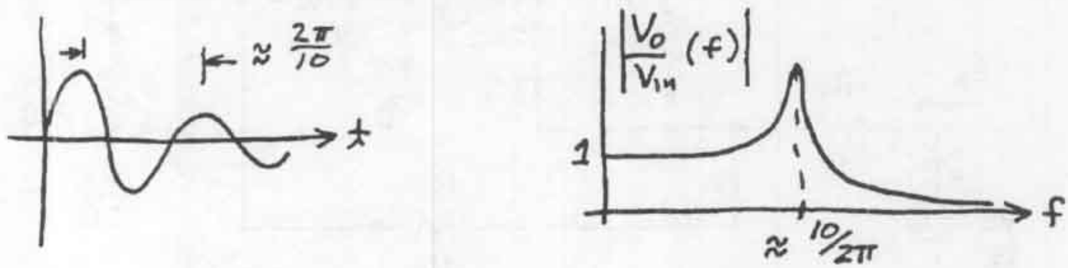
(a) The circuit is a voltage divider.

$$\frac{V_o}{V_{in}}(s) = \frac{1/sC}{sL + R + 1/sC} = \frac{1/LC}{s^2 + s(R/L) + 1/LC} = \frac{101}{s^2 + 2s + 101}$$

The poles are the roots of the denominator polynomial which are $s_p = -1 \pm j10$. There are no finite zeros. The transient response contains damped sinusoids of the form

$$\exp(-t)[A\cos(10t) + B\sin(10t)]$$

Using the rubber-sheet analogy we expect the transfer function sketched below.



A transient analysis of the circuit for a short input pulse (that approximates an impulse) and an ac sweep to plot the transfer function versus frequency is stored in the file named Exer9_14. The simulation results confirm our predictions about the circuit response.

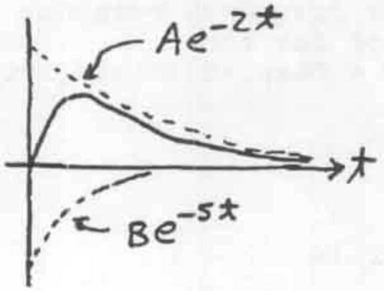
(b) The circuit is a voltage divider.

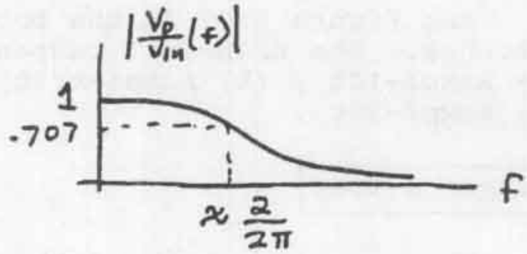
$$\frac{V_o}{V_{in}}(s) = \frac{1/sC}{sL + R + 1/sC} = \frac{1/LC}{s^2 + s(R/L) + 1/LC} = \frac{10}{s^2 + 7s + 10}$$

The poles are the roots of the denominator polynomial which are $s_{p1} = -2$ and $s_{p2} = -5$. There are no finite zeros. The transient response contains exponentials:

$$A\exp(-2t) + B\exp(-7t)$$

Using the rubber-sheet analogy we expect the transfer function sketched below.





A transient analysis of the circuit for a short input pulse (that approximates an impulse) and an ac sweep to plot the transfer function versus frequency is stored in the file named Exer9_14b. The simulation results confirm our predictions about the circuit response.

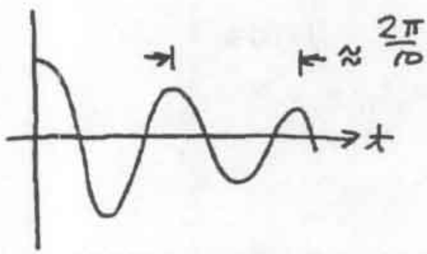
(c) The circuit is a voltage divider.

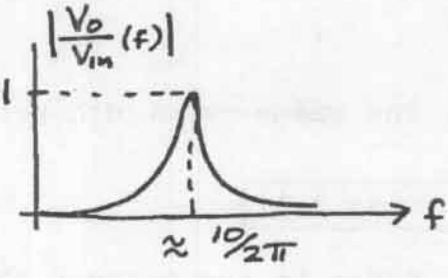
$$\frac{V_o}{V_{in}}(s) = \frac{R}{sL + R + 1/sC} = \frac{s(R/L)}{s^2 + s(R/L) + 1/LC} = \frac{2s}{s^2 + 2s + 101}$$

The poles are the roots of the denominator polynomial which are $s_p = -1 \pm j10$ There is a zero at s = 0. The transient response contains damped sinusoids of the form

$$\exp(-t)[A\cos(10t) + B\sin(10t)]$$

Using the rubber-sheet analogy we expect the transfer function sketched below.





A transient analysis of the circuit for a short input pulse (that approximates an impulse) and an ac sweep to plot the transfer function versus frequency is stored in the file named Exer9_14c. The simulation results confirm our predictions about the circuit response.

Exercise 9.15

See Figure 9.37 in the book for the frequency response sketches. The transient responses are of the form: (a) $A\exp(-10t)$; (b) $A\exp(-t/10)\cos(10t) + B\exp(-t/10)\sin(10t)$; (c) $A\exp(-10t)$.

Exercise 9.16

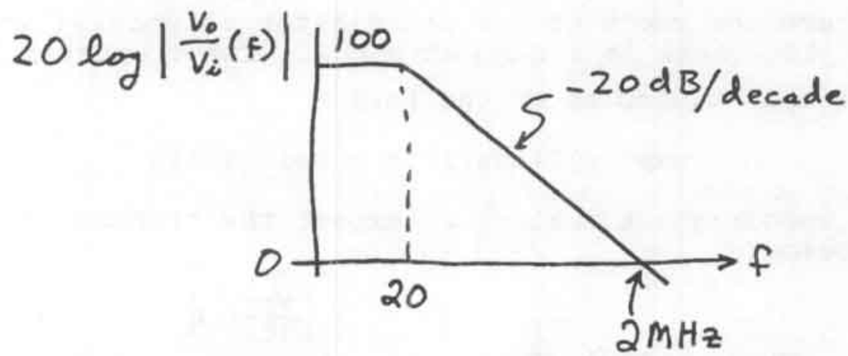
The open-loop gain of the amplifier is

$$A(s) = \frac{V_o(s)}{V_i(s)} = \frac{1/sC_P}{R_P + 1/sC_p} \times 10^5 = \frac{10^5}{sR_pC_p + 1}$$

This is of the same form as Equation (9.42) with $A_0 = 10^5$ and $f_b = 1/(2\pi R_P C_P) = 20$ Hz.

(a) The pole for $A(s)$ is located at $s_p = -1/R_P C_P = -125.6$ rad/s.

(b) The gain magnitude is 100 dB up to the corner frequency of 20 Hz. Then it falls off at 20 dB per decade.



(c) The gain--bandwidth product is $A_0 f_b = 2$ MHz.

Exercise 9.17

(a) Refer to the circuit shown in Figure 9.40b. Because $R_2 \gg R_o$ and $R_i \gg R_1$ we can neglect loading effects. This circuit has negative series voltage feedback. The feedback ratio is $\beta = R_2/(R_1 + R_2) = 0.01$. Using Equation (9.44), we have $A_{0f} = A_0/(1 + A_0\beta) = 10^5/(1 + 1000) = 99.9 \cong 100$.

(b) From Exercise 9.16 we have a gain-bandwidth product of 2 MHz. Thus we expect a closed-loop bandwidth of $f_{bf} = (2 \times 10^6)/100 = 20$ kHz.

(c) The results of the simulation are in good agreement the answers of parts a and b. The simulation is stored in the file Exer9_17.

(d) At f = 1 Hz, $Z_{in} \cong 10^9\angle -3^\circ$ which is approximately a 1 GΩ resistance. At f = 1 kHz, $Z_{in} \cong 20\times10^6\angle -86^\circ$ which is approximately the same impedance as an 8 pF capacitor.

(e) The bandwidth is approximately $f_{bf} = 780$ Hz. It is less than in part c because the low values for R_1 and R_2 load the output of the amplifier reducing the effective gain magnitude by a factor of approximately 26.

Exercise 9.18

Equation 9.50 states

$$s = -\frac{1}{2}(2\pi f_1 + 2\pi f_2) \pm \frac{1}{2}\sqrt{(2\pi f_1 + 2\pi f_2)^2 - 16\pi^2 f_1 f_2(1 + A_0\beta)}$$

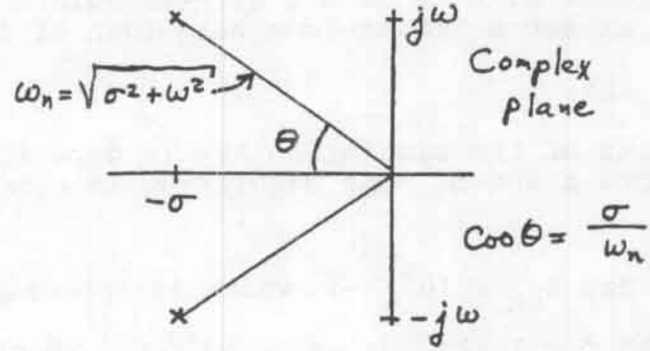
The amplifier has $f_1 = f_2 = 100$ kHz $A_0 = 10^4$ and $\beta = 0.1$. Substituting these values we obtain

$$s = 2\pi 10^5(-1 \pm j\sqrt{1000})$$

The natural frequency is $\omega_n = 2\pi 10^5\sqrt{1001}$ which corresponds to a period of 0.316 μs. This compares very well with the interval between peaks of the ringing in Figure 9.43 in the book.

Exercise 9.19

A pair of poles $s_p = -\sigma \pm j\omega$, has a natural frequency of $\omega_n = \sqrt{\sigma^2 + \omega^2}$ and a damping ratio $\delta = \frac{\sigma}{\omega_n}$. [These are Equations (9.36) and (9.37) on page 594 in the book.] The poles are shown in the complex plane on the next page. Notice that $\delta = \cos(\theta)$. Thus for $\delta = 0.707$ we have $\theta = 45^\circ$ and $\sigma = \omega$.



For a two-pole amplifier with feedback, Equation 9.50 states

$$s = -\frac{1}{2}(2\pi f_1 + 2\pi f_2) \pm \frac{1}{2}\sqrt{(2\pi f_1 + 2\pi f_2)^2 - 16\pi^2 f_1 f_2 (1 + A_0\beta)}$$

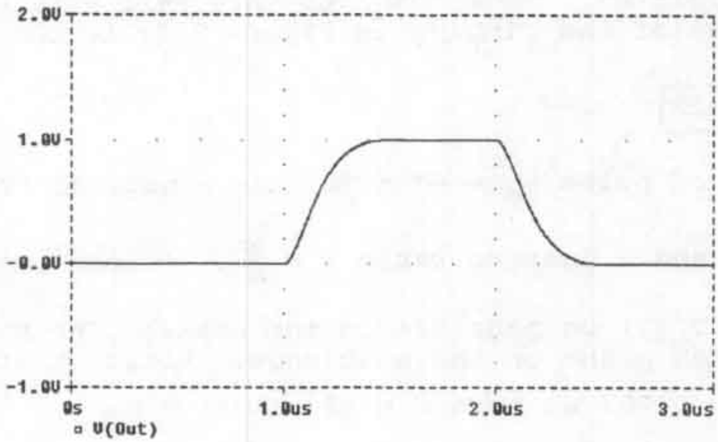
Thus we have $\sigma = \frac{1}{2}(2\pi f_1 + 2\pi f_2)$

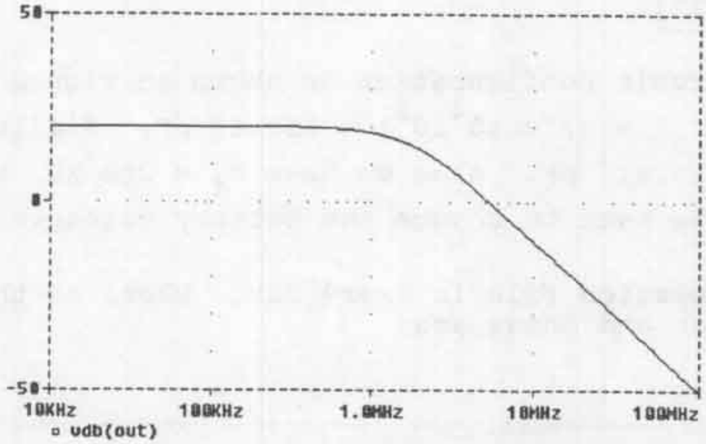
and $j\omega = \frac{1}{2}\sqrt{(2\pi f_1 + 2\pi f_2)^2 - 16\pi^2 f_1 f_2 (1 + A_0\beta)}$

Substituting $f_1 = f_2$ and simplifying, we have $\sigma = 2\pi f_1$ and $\omega = 2\pi f_1\sqrt{A_0\beta}$. Then we set $\sigma = \omega$ and solve for $\beta = 1/A_0 = 10^{-4}$. Thus to have $\delta \ge 0.707$ we must have $\beta \le 10^{-4}$ and $A_{0f} = A_0/(1 + A_0\beta) \ge 5000$.

Exercise 9.20

The simulation file is named Exer9_20. The plots corresponding to Figures 9.43 and 9.44 in the book are:





Notice that for this two-pole amplifier, feedback does not produce ringing in the transient response or peaking in the frequency response. Often this is the case in a multipole amplifier when one break frequency is much smaller than any of the others.

Exercise 9.21

As in Example 9.7, the closed-loop poles are the roots of $\beta A(s) = -1$. Thus we must solve

$$\frac{\beta 10^4}{[1 + s/(2\pi f_b)]^4} = -1$$

Taking the fourth root of each side we obtain:

$$s_1 = 2\pi f_b\left[\sqrt[4]{\beta}10\angle -45^\circ - 1\right] \qquad s_2 = 2\pi f_b\left[\sqrt[4]{\beta}10\angle 45^\circ - 1\right]$$
$$s_3 = 2\pi f_b\left[\sqrt[4]{\beta}10\angle 135^\circ - 1\right] \qquad s_4 = 2\pi f_b\left[\sqrt[4]{\beta}10\angle -135^\circ - 1\right]$$

The amplifier becomes unstable when the poles s_1 and s_2 move into the right-half plane. The real part of s_1 (or s_2) is

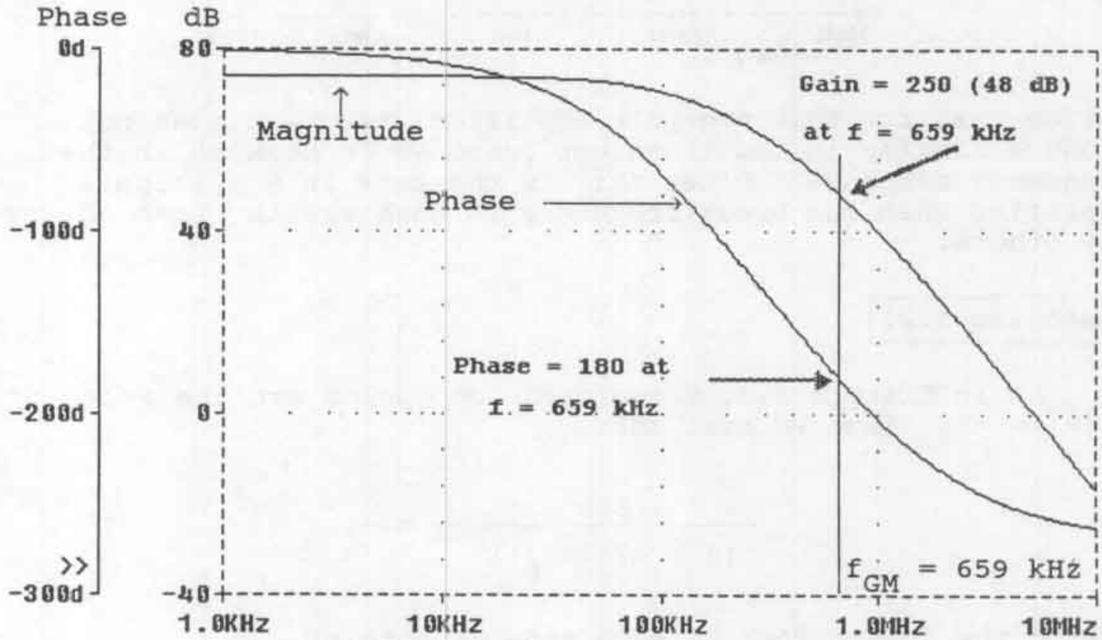
$$\mathcal{R}e(s_1) = 2\pi f_b[\sqrt[4]{\beta}10\cos(-45^\circ) - 1]$$

Setting this equal to zero and solving we obtain $\beta_u = 0.0004$. The root locus is shown in Figure 9.48 in the book.

Exercise 9.22

(a) The circuit configuration is shown in Figure 9.46. We have $C_1 = 1/(2\pi R_1 f_1) = 1/(2\pi 10^4 10^5) = 159.15$ pF. Similarly $C_2 = 53.05$ pF and $C_3 = 15.915$ pF. Also we have $R_i = 200$ kΩ, $R_o = 25$ Ω, and $A_0 = 5000$. We need to change the battery voltages to ±5 V.

(b) The simulation file is Exer9_22b. Plots of the open-loop gain magnitude and phase are:



From the magnitude and phase plots we determine that 659 kHz is the frequency (f_{GM}) for which the phase is 180°. At f_{GM} the magnitude is 250 (48 dB). Thus to avoid oscillation the maximum value of β is $\beta_{max} = 1/250 = 0.004$.

(d) For a gain margin of 10 dB (which is equivalent to a gain ratio of $10^{10/20} = 3.16$, the value of β is $0.004/3.16 = 1.26 \times 10^{-3}$, which is equivalent to -58 dB.

(e) We use the plots to determine the frequency f_{PM} at which $A\beta = 1$, or equivalently $A_{dB} + \beta_{dB} = 0$. Because we have $\beta_{dB} = -58$ dB, we are looking for the frequency at which $A_{dB} = 58$. We find f_{PM}

= 363 kHz. At this frequency we have a phase of -145°. Thus the phase margin is 45°.

(f) We require $\beta = 1.26 \times 10^{-3} = R_A/(R_A + R_B)$. One choice of resistance values (which also produce negligible loading effects) is $R_A = 1\ k\Omega$ and $R_B = 793\ k\Omega$.

(g) A simulation for the closed-loop response is stored in the file named Exer9_22g.

Exercise 9.23

Follow the procedure of Example 9.11, changing the capacitance values to $C_1 = C_2 = C_3 = 1/[2\pi(2 \times 10^6)100] = 795.8$ pF. A simulation that can be used to obtain plots of the open-loop gain magnitude and phase is stored in the file named Exer9_23a.

f_{PM} is the frequency for which the phase is -30°. From the plots of open-loop gain magnitude and phase, we find that f_{PM} = 354 kHz and that the gain magnitude at this frequency is 79.6 dB.

Thus we require $20\log(1 + f_{PM}/f_C) = -59.6$ dB. This yields $f_C = 371$ Hz. Then we have $C_C = 1/(2\pi f_C R_C) = 4.29\ \mu F$. The simulation file for the closed-loop amplifier is stored in the file named Exer9_23b.

Exercise 9.24

The circuit is shown on the next page. For the RL circuit we can write:

$$\beta = \frac{V_o}{V_{in}} = \frac{\dfrac{R(j\omega L)}{R + j\omega L}}{R + j\omega L + \dfrac{R(j\omega L)}{R + j\omega L}} =$$

$$\frac{j\omega RL}{R^2 - \omega^2 L^2 + j3\omega RL}$$

For oscillation the Barkhausen criterion requires $A_V\beta = 1$, and we have

$$\frac{j\omega RLA_V}{R^2 - \omega^2L^2 + j3\omega RL} = 1$$

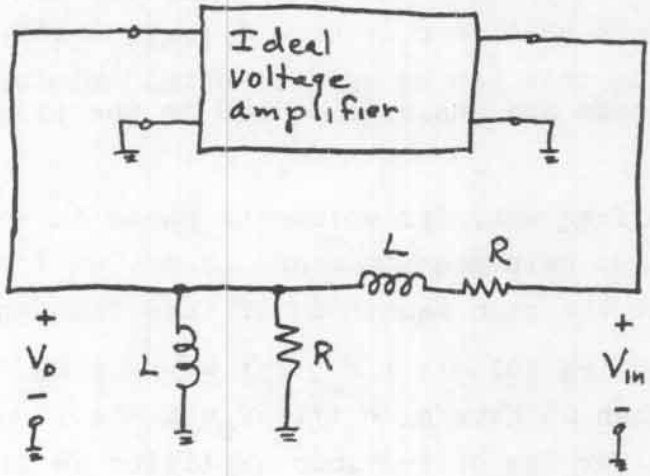
$$R^2 - \omega^2L^2 + j\omega RL(3 - A_V) = 0$$

Now we equate the real parts of both sides:

$$R^2 - \omega^2L^2 = 0 \quad \Rightarrow \quad \omega = R/L$$

Similarly equating the imaginary parts:

$$j\omega RL(3 - A_V) = 0 \quad \Rightarrow \quad A_{vmin} = 3$$



Exercise 9.25

From the circuit shown in Figure 9.72, we can write:

$$\beta = \frac{V_o}{V_{in}} = \frac{\dfrac{R_B(1/j\omega C_B)}{R_B + 1/j\omega C_B}}{R_A + 1/j\omega C_A + \dfrac{R_B(1/j\omega C_B)}{R_B + 1/j\omega C_B}} =$$

$$\frac{R_B(1/j\omega C_B)}{R_AR_B - 1/(\omega^2C_AC_B) + R_B/(j\omega C_A) + R_A/(j\omega C_B) + R_B/(j\omega C_B)} =$$

$$\beta = \frac{R_B}{R_B C_B/C_A + R_A + R_B + j(\omega C_B R_A R_B - 1/\omega C_A)}$$

For oscillation the Barkhausen criterion requires $A_v\beta = 1$, and we have

$$\frac{R_B A_v}{R_B C_B/C_A + R_A + R_B + j(\omega C_B R_A R_B - 1/\omega C_A)} = 1$$

$$R_B C_B/C_A + R_A + R_B + j(\omega C_B R_A R_B - 1/\omega C_A) = R_B A_v$$

Now we equate the real parts of both sides:

$$A_v R_B = R_B C_B/C_A + R_A + R_B \quad \Rightarrow \quad A_{vmin} = 1 + R_A/R_B + C_B/C_A$$

Similarly equating the imaginary parts:

$$j(\omega C_B R_A R_B - 1/\omega C_A) = 0 \quad \Rightarrow \quad \omega = 1/\sqrt{R_A R_B C_A C_B}$$

Exercise 9.26

One solution is simply to reduce the capacitances in the circuit of Figure 9.77 by a factor of five which will increase the frequency from 1 kHz to 5 kHz. The file Exer9_26 contains a simulation of the circuit.

Problem 9.1

Some of the potential benefits of negative feedback are:

1. Stabilization of gain. Closed-loop gain can depend almost solely on a feedback network that is constructed of relatively stable passive components (i.e., resistors and/or capacitors).

2. Reduction of nonlinear distortion.

3. Reduction of certain types of noise, such as power-supply hum.

4. Control (by the designer) of the input and output impedances.

5. Extension of bandwidth.

Problem 9.2

Some of the problems associated with positive feedback in amplifiers are:

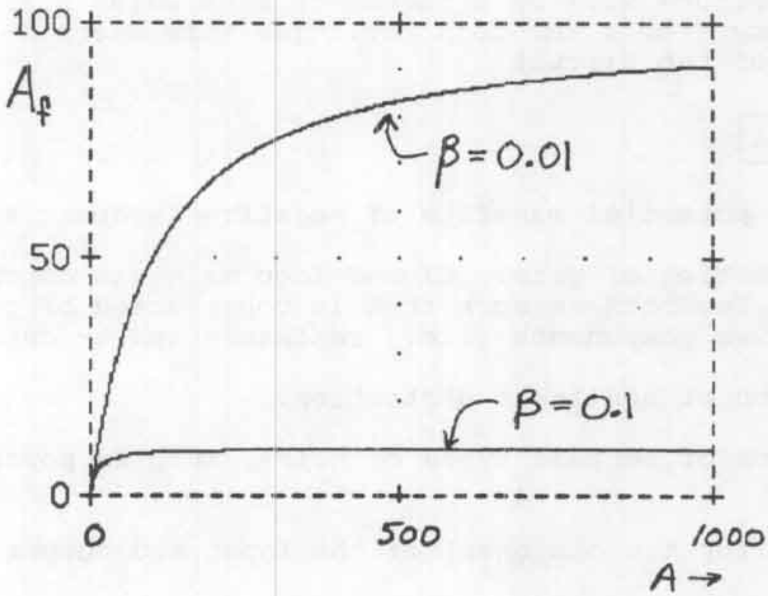
1. Closed-loop gain is highly dependent on device parameters which vary greatly with temperature, operating point and from device to device. Thus, positive feedback leads to poor gain stability--much worse than for the original amplifier.

2. Oscillation in which the amplifier generates signals unrelated to those being amplified.

Problem 9.3

In a negative feedback amplifier that has $A\beta >> 1$, the feedback signal x_f is approximately equal to the source signal x_s. Therefore the input to the amplifier $x_i = x_s - x_f$ is very small compared to either x_s or x_f. Often to simplify analysis we assume that x_i is zero and we refer to this condition as the summing-point constraint.

Problem 9.4



Problem 9.5

For A = 1000, we have $A_f = A/(1 + A\beta) = 9.9$.

$x_o(t) = A_f x_s = 9.9\cos(\omega t)$

$x_f(t) = \beta x_o = 0.99\cos(\omega t)$

$x_i(t) = x_s - \beta x_o \cong 0.01\cos(\omega t)$

For $A = 10^4$, we have $A_f = A/(1 + A\beta) = 9.99$.

$x_o(t) = A_f x_s = 9.99\cos(\omega t)$

$x_f(t) = \beta x_o = 0.999\cos(\omega t)$

$x_i(t) = x_s - \beta x_o \cong 0.001\cos(\omega t)$

As A approaches ∞, $x_i(t)$ approaches zero.

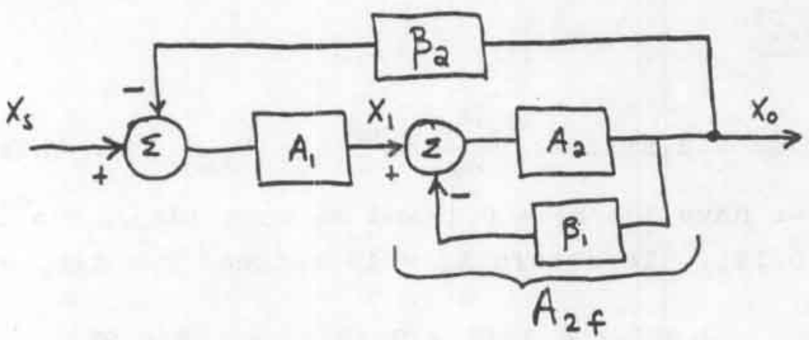
Problem 9.6

Equation 9.2 states: $\dfrac{dA_f}{A_f} = \dfrac{dA}{A}\dfrac{1}{(1 + A\beta)}$. In this amplifier we have $|dA/A| = 0.03$ and we want $|dA_f/A_f| \le 0.001$ (which is 0.1%). Thus:

$$0.001 \ge 0.03/(1 + 10^4\beta) \quad \Rightarrow \quad \beta \ge 29 \times 10^{-4} \quad \Rightarrow \quad A_f = 333$$

Problem 9.7

(a)



$$A_{2f} = X_o/X_1 = A_2/(1 + \beta_1 A_2)$$

$$A_f = \frac{X_o}{X_s} = \frac{A_2 A_{2f}}{1 + \beta_2 A_1 A_{2f}} = \frac{A_1 A_2}{1 + \beta A_2 + \beta A_1 A_2}$$

(b) Refer to Figure P9.7b in the book. Notice that the subsystem consisting of A_2 and β_2 is identical to the system discussed in the book and its gain is $A_2/(1 + \beta_2 A_2)$. This block plus A_1 and A_2 form an amplifier having a a gain of $A_1[A_2/(1 + A_2\beta_2)]A_3$. Finally, we can write the closed-loop gain of the entire system as:

$$\frac{A_1[A_2/(1 + A_2\beta_2)]A_3}{1 + \beta_1 A_1[A_2/(1 + A_2\beta_2)]A_3} = \frac{A_1 A_2 A_3}{1 + A_2\beta_2 + A_1 A_2 A_3 \beta_1}$$

Problem 9.8

(a) $A_f = A/(1 - A\beta)$ In this amplifier, the closed-loop gain magnitude is less than the open-loop gain magnitude if $(1 - A\beta)$ is larger than unity. This happens if either A or β (but not both) assume negative values. (We assume that both A and β are real numbers.)

(b) If A is negative and β is positive, x_f should be added to x_s (as in Figure P9.8 in the book) to attain negative feedback.

(c) If both A and β are negative, x_f should be subtracted from x_s (as in Figure 9.1 in the book) to attain negative feedback.

Problem 9.9

Equation 9.2 states: $\frac{dA_f}{A_f} = \frac{dA}{A}\frac{1}{(1 + A\beta)}$. In this amplifier we have $|dA/A| = 0.1$ and we want $|dA_f/A_f| \le 0.001$ (which is 0.1%). To attain $A_f = 10$ we need $\beta \cong 1/A_f = 0.1$ Thus:

$$0.001 \ge 0.1/(1 + 0.1A) \quad \Rightarrow \quad A \ge 990$$

Assuming that A = 990, we need $\beta = 0.098989$ to achieve $A_f = 10$. In practice, we might include a variable resistor to adjust β to the required value.

Problem 9.10

To be effective in reducing distortion, we need to have $|A\beta| > 1$.

Problem 9.11

In a negative feedback amplifier with distortion, the input signal to the amplifier $x_i = x_s - x_f$ is distorted in a manner that tends to compensate for the nonlinearity of the amplifier.

Problem 9.12

See Figure 9.7 on page 563 in the book. Crossover distortion occurs because v_s must reach approximately 0.7 V in magnitude before either transistor enters the active region.

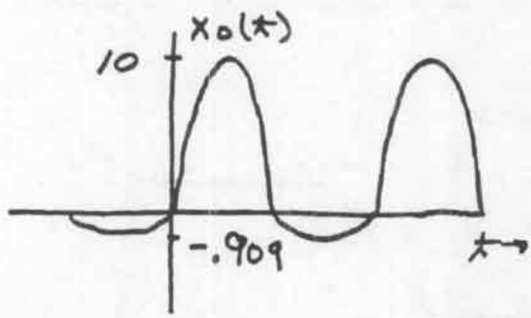
Problem 9.13

For the configuration of Figure P9.8, we have $A_f = A/(1 - A\beta)$. Substituting values, we have

$A = 10$ and $A_f = 100$ for $0 < x_i < 1$ or $0 < x_o < 10$

$A = 5$ and $A_f = 9.09$ for $-2 < x_i < 0$ or $-10 < x_o < 0$

Thus for $x_s = 0.1\sin(\omega t)$, the positive peak of the output is $100 \times 0.1 = 10$ V and the negative peak is $9.09 \times (-0.1) = -0.909$. A sketch of the output waveform is



With positive feedback, the ratio of the positive peak to the negative peak is 11.0, whereas the ratio is 2 without feedback. Notice that the output waveform is more distorted for the amplifier with positive feedback than for the amplifier without feedback.

Problem 9.14

(a) For $v_s > 0.7$ V, Q_1 and Q_3 are conducting whereas Q_2 and Q_4 are cutoff. On the other hand, for $v_s < -0.7$ V, Q_2 and Q_4 are conducting whereas Q_1 and Q_3 are cutoff. Finally for $-0.7 < v_s < 0.7$, all of the transistors are cutoff and $v_o = 0$.

Assuming that $v_{BE} = 0.7$ V in the active region and that $v_s > 0.7$, we have $i_{E1} = (v_s - 0.7)/R_E$, $i_{C1} = \alpha_1 i_{E1} = \beta_1 i_{E1}/(\beta_1 + 1)$, $i_{C3} = \beta_3 i_{C1}$, and $v_o = 8i_{C3}$. Using the values given in the problem these relationships yield

$$v_o = 9.9(v_s - 0.7) \quad \text{for } v_s > 0.7 \text{ and } v_o < 14.8 \text{ V}$$

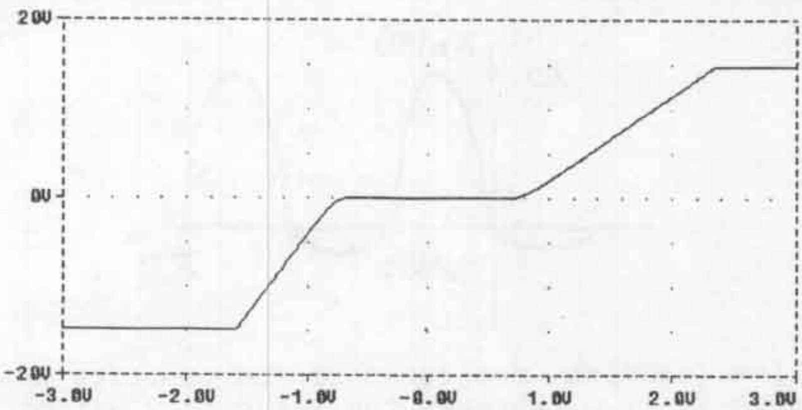
When v_o reaches 14.8 V, Q_3 becomes saturated, and v_o no longer increases with v_s.

Similarly we have

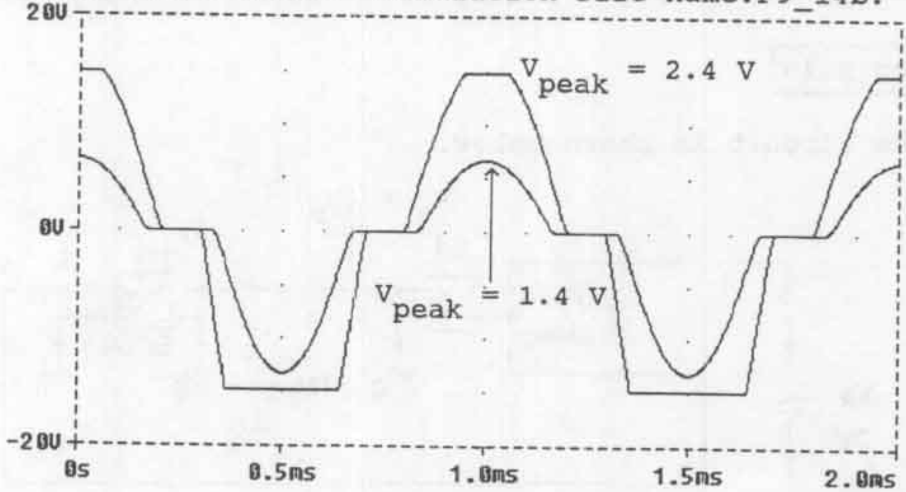
$$v_o = 19.8(v_s + 0.7) \quad \text{for } v_s < -0.7 \text{ and } v_o > -14.8 \text{ V}$$

When v_o reaches -14.8 V, Q_4 becomes saturated and v_o no longer decreases with v_s.

A simulation that plots v_o versus v_s is stored in the file named P9_14a. The plot shown below agrees very well with the equations derived above.

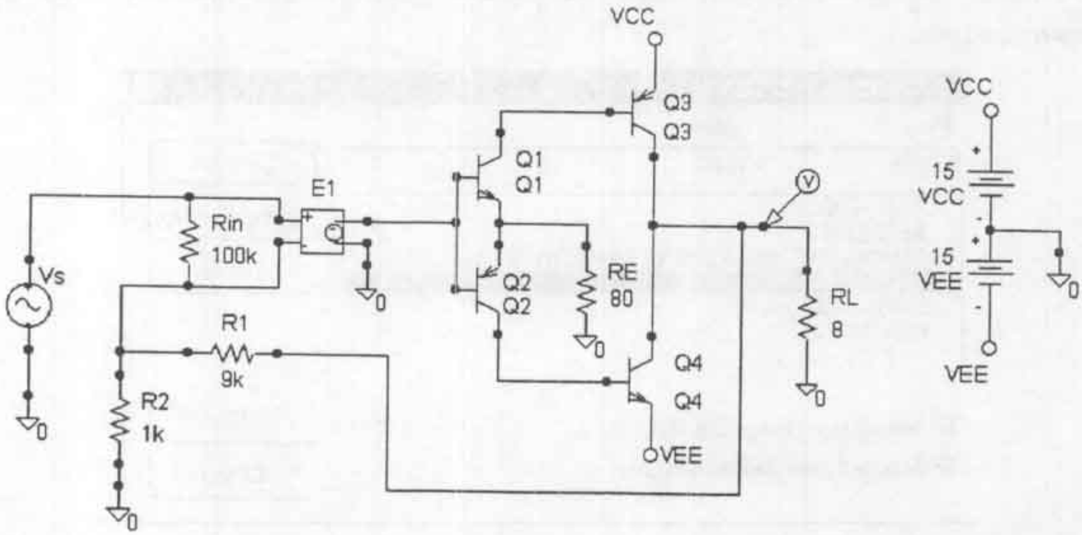


Simulating the circuit for the specified input sine waves yields the waveforms shown below. Simulation file name:P9_14b.



For a peak source voltage of 1.4 V, we observe only crossover distortion. For a peak source voltage of 2.4 V, we observe both clipping and crossover distortion.

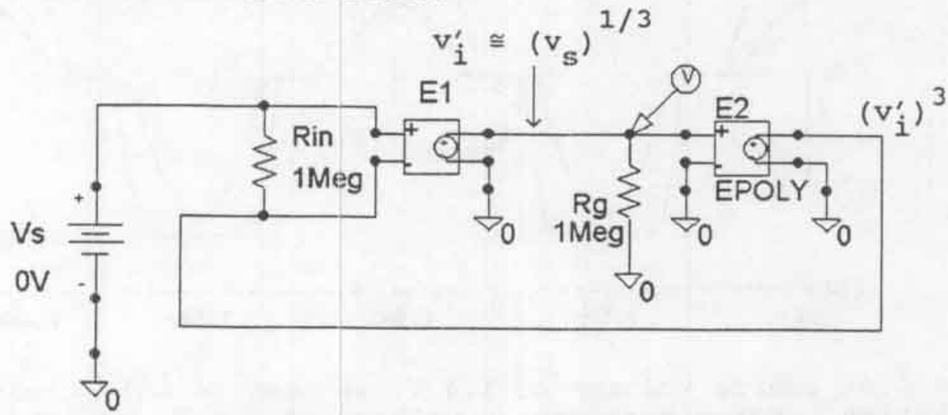
(b) To achieve $A_f = 10$ in a negative feedback amplifier, we need $\beta \cong 0.1$ (assuming that $A\beta >> 1$). Thus we select $R_1 \cong 9R_2$. The circuit diagram is shown below.



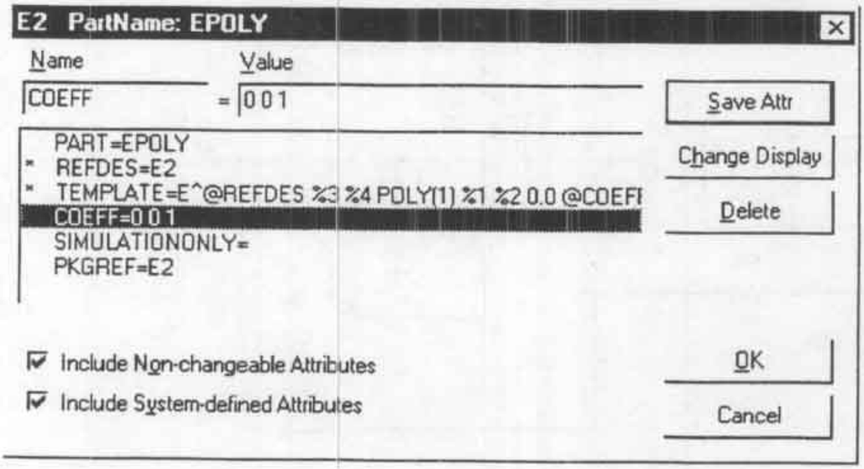
(c) The simulation, which is stored in the file named P9_14c, shows that negative feedback effectively eliminates the crossover distortion. Of course negative feedback cannot overcome clipping due to saturation of the transistors. Unfortunately this cannot be demonstrated for the circuit of P9_14c due to convergence problems with a source amplitude of 2.4 V. File P9_14c_alt replaces the controlled source with a μA741 op amp and makes a convincing demonstration of the limitations of negative feedback.

Problem 9.15

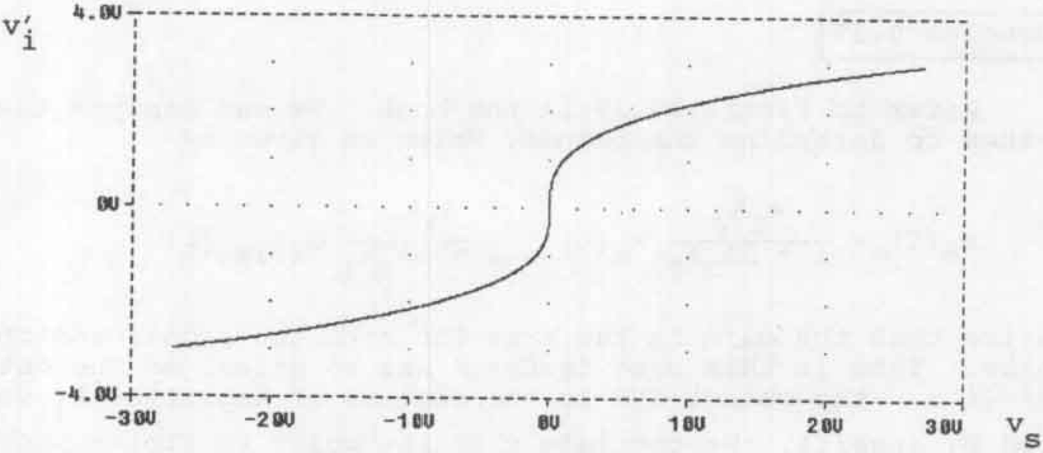
The circuit is shown below.



R_{in} and E_1 model the differential preamplifier. If R_g is not included, PSpice aborts because it requires at least two elements connected to each node. (The input to E_2 is an open circuit.) Otherwise R_g has no effect on the operation of the circuit. E_2 models the cube circuit. The setup window for E_2 is shown below.



The simulation is stored in the file named P9_15. A plot of the cube-root output versus v_s is shown on the next page. It can be verified that the values of v'_i are almost exactly equal to the cube root of v_s.



Problem 9.16

$$SNR_{dB} = 10\log(P_{signal}/P_{noise})$$

Problem 9.17

If a low-noise preamplifier can be found to place ahead of the noisy amplifier, feedback can be effective in improving the SNR at the output. An example of a situation in which this is often possible is an audio power amplifier operating from a poorly filtered supply with a great deal of ripple. Then we design a high-gain low-noise preamplifier supplied with ripple-free dc and use feedback to bring the gain back down to the desired value. The advantage is that it is relatively easy to provide ripple-free dc at a lower power level of the preamplifier.

Problem 9.18

$$P_o = (V_{signal})^2/R_L \quad \Rightarrow \quad V_{signal} = 17.9 \text{ V rms}$$

$$90 = 10\log(P_{signal}/P_{noise}) \quad \Rightarrow \quad P_{noise} = 40/10^9$$

$$P_{noise} = (V_{noise})^2/R_L \quad \Rightarrow \quad V_{noise} = 566\ \mu\text{V rms}$$

Problem 9.19

Refer to Figure P9.19 in the book. We can analyze the system to determine the output, which is given by

$$x_o(t) = \frac{A_1A_2}{1 + \beta A_1A_2} x_s(t) + \frac{A_1A_2}{1 + \beta A_1A_2} x_{noise}(t)$$

Notice that the gain is the same for both the signal and the noise. Thus in this case feedback has no effect on the output SNR (i.e., the output SNR is the same as if amplifier A_1 were used by itself). We conclude that the noisy amplifier should be placed after the low-noise preamplifier.

Problem 9.20

(a) For an SNR of 50 dB, we have $50 = 20\log(V_s/V_{noise})$, which implies that $V_{noise} = V_s \times 10^{-(50/20)} = 47.4$ mV rms.

(b) According to Equation 9.17 on page 569, the SNR with feedback is equal to the gain of the preamplifier squared times the SNR before feedback. To improve the SNR by a factor of 100, the gain of the preamplifier must be 10. The gain of the system with feedback is $A_f = A_1A_2/(1 + \beta A_1A_2)$. Setting $A_f = A_1$ and $A_2 = 10$ we determine that $\beta = 0.9/A_1$.

Problem 9.21

The block diagram of the system is shown in Figure 9.13 on page 568 in the book. We are given $A_1 = 100$ and $X_{noise} = (2\ \text{V})/A_1 = 20$ mV peak. The output of the system is given by Equation 9.15.

$$x_o(t) = x_s(t)\frac{A_1A_2}{1 + \beta A_1A_2} + x_{noise}(t)\frac{A_1}{1 + \beta A_1A_2}$$

We require that the gain for the signal is 100 and that the output noise is 0.1 V peak. Thus we have

$$\frac{A_1A_2}{1 + \beta A_1A_2} = 100$$

and $0.1 = (20\ \text{mV})\dfrac{A_1}{1 + \beta A_1A_2}$

Solving, we find the $A_2 = 20$ and $\beta = 0.0095$ are required.

Problem 9.22

In voltage feedback, a current or voltage that is proportional to the output voltage is returned to the input. In current feedback, a current or voltage that is proportional to the output current is returned to the input. In series feedback, the signal source, the amplifier input terminals, and the output terminals of the feedback network are in series. In parallel feedback, the signal source, the amplifier input terminals, and the output terminals of the feedback network are in parallel.

Problem 9.23

Conceptually, we test for voltage feedback by short-circuiting the output terminals, thereby reducing the output voltage to zero. If feedback is disabled by shorting the output, we have voltage feedback.

Conceptually, we test for current feedback by open-circuiting the output terminals, thereby reducing the output current to zero. If feedback is disabled by opening the output, we have current feedback.

Problem 9.24

In series feedback, the signal source, the feedback signal, and the amplifier input terminals are in series. Since the input voltage to the amplifier is the sum of the source voltage and the feedback voltage, it is natural to treat the signal source as a voltage source in a series feedback system.

In parallel feedback, the signal source, the output terminals of the feedback network, and the amplifier input terminals are in parallel. Since the amplifier input current is the difference between the source current and the feedback current, it is natural to treat the signal source as a current source in a parallel feedback system.

Problem 9.25

Feedback type	Gain	Units for β
Series voltage	Voltage	V/V
Series current	Transconductance	Ω
Parallel voltage	Transresistance	Siemens
Parallel current	Current	A/A

Problem 9.26

Negative series feedback increases input impedance. Negative parallel feedback reduces input impedance.

Problem 9.27

To make the output terminals of a feedback amplifier appear as a nearly ideal voltage source (i.e., nearly zero output impedance), negative voltage feedback is needed. To make the output act as a nearly ideal current source (i.e., very large output impedance), negative current feedback is needed.

Problem 9.28

See Table 9.1 on page 573 in the book.

Problem 9.29

To obtain a nearly ideal transresistance amplifier, we use negative parallel voltage feedback. Because $A_f \cong 1/\beta$ for $|A\beta| >> 1$, we need $\beta = 1/2000 = 500\ \mu S$ to achieve $R_{mf} \cong 2000\ \Omega$.

Problem 9.30

We assume an open circuit load and neglect loading by the feedback network. Then we have $A_v \cong A_{vo}$. Using the formulas given in Table 9.1 we have

$$A_{vf} = \frac{A_v}{1 + A_v\beta} = 9.9990$$

$$R_{if} = R_i(1 + A_v\beta) = 10^3(1 + 10^5 \times 0.1)$$

$$= 10\ \text{M}\Omega$$

$$R_{of} = R_o/(1 + A_{vo}\beta) = 1000/(1 + 10^5 \times 0.1)$$

$$= 0.1\ \Omega$$

Problem 9.31

To obtain a nearly ideal current amplifier, we use negative parallel current feedback. Because $A_f \cong 1/\beta$ for $|A\beta| >> 1$, we need $\beta = 1/10$ to achieve $A_{if} \cong 10\ \Omega$.

Problem 9.32

The short circuit open-loop transconductance gain is

$$G_{msc} = i_o/v_i = [A_{vo}v_i/R_o]/v_i = A_{vo}/R_o = 10^5/(1\ \text{k}\Omega) = 100\ \text{S}$$

We assume a short-circuit load and neglect loading by the feedback network. Then we have $G_m \cong G_{msc} = 100$ S. Using the formulas from Table 9.1, we obtain

$$G_{mf} = G_m/(1 + G_m\beta) = 100/(1 + 100 \times 10^4) \cong 100\ \mu\text{S}$$

$$R_{if} = R_i(1 + G_m\beta) = 10^3(1 + 100 \times 10^4) = 1\ \text{G}\Omega$$

$$R_{of} = R_o(1 + G_m\beta) = 10^3(1 + 100 \times 10^4) = 1\ \text{G}\Omega$$

Problem 9.33

To obtain a nearly ideal transconductance amplifier, we use negative series current feedback. Because $A_f \cong 1/\beta$ for $|A\beta| >>$ 1, we need $\beta = 1/0.05 = 20\ \Omega$ to achieve $G_{mf} \cong 0.05$ S.

Problem 9.34

To achieve a nearly ideal voltage amplifier, we should use negative series voltage feedback. Because $A_f \cong 1/\beta$ for $|A\beta| >> 1$, we need $\beta = 1/25 = 0.04$ V/V to achieve $A_{vf} \cong 25$.

Problem 9.35

$$A_{isc} = i_o/i_i = (A_{vo}v_i/R_o)/(v_i/R_i)i_i = A_{vo}R_i/R_o = 10^5$$

We neglect loading effects (in which case $A_i = A_{isc}$) and use the formulas from Table 9.1.

$$A_{if} = A_i/(1 + \beta A_i) = 10^5/(1 + 0.1 \times 10^5) = 9.9990$$

$$R_{if} = R_i/(1 + \beta A_i) = 10^3/(1 + 0.1 \times 10^5) = 0.1\ \Omega$$

$$R_{of} = R_o(1 + \beta A_{isc}) = 10^3(1 + 0.1 \times 10^5) = 10\ \text{M}\Omega$$

Problem 9.36

$$R_{moc} = v_o/i_i = (A_{voc}v_i)/(v_i/R_i) = A_{vo}R_i = 10^8\ \Omega$$

We neglect loading effects (in which case $R_m = R_{msc}$) and use the formulas from Table 9.1.

$$R_{mf} = R_m/(1 + \beta R_m) = 10^8/(1 + 0.01 \times 10^8)$$

$$= 100\ \Omega$$

$$R_{if} = R_i/(1 + \beta R_m) = 10^3/(1 + 0.01 \times 10^8)$$

$$= 1\ \text{m}\Omega$$

$$R_{of} = R_o/(1 + \beta R_m) = 10^3/(1 + 0.01 \times 10^8)$$

$$= 1\ \text{m}\Omega$$

Problem 9.37

See Figure 9.19 on page 578 in the book. Other correct answers exist, for example see the circuits and answers for Exercise 9.9 on page 580. In series feedback the source, the amplifier input terminals, and the output port of the feedback network should be in series. In parallel feedback, they are in parallel. For voltage feedback the signal fed back should vanish when the load is a short circuit. In current feedback, the signal fed back should become zero when the load becomes an open circuit.

Problem 9.38

(a) This circuit has negative series voltage feedback with $\beta = v_f/v_o = -R_2/(R_1 + R_2)$. (The minus sign is due to the reference polarity for v_f shown in Figure P9.38.) Also notice that the open-loop amplifier gain is negative. For very large loop gain, the amplifier tends toward an ideal voltage amplifier with $A_{vf} = 1/\beta = -(1 + R_1/R_2)$, the input impedance approaches infinity, and the output impedance approaches zero.

(b) This circuit has negative series current feedback with $\beta = v_f/i_o = -R/5$. (The minus sign is due to the reference polarity for v_f shown in Figure P9.38.) Also notice that the open-loop amplifier gain is negative. For very large loop gain, the amplifier tends toward an ideal transconductance amplifier with $G_{mf} = 1/\beta = -5/R$, the input impedance approaches infinity, and the output impedance approaches infinity.

(c) This circuit has negative parallel current feedback with $\beta = i_f/i_o = -R_1/(R_1 + R_2)$. (The minus sign is due to the reference direction for i_f and i_o shown in Figure P9.38.) Also notice that the open-loop amplifier gain is negative. For very large loop gain, the amplifier tends toward an ideal current amplifier with $A_{if} = 1/\beta = -(1 + R_2/R_1)$, the input impedance approaches zero, and the output impedance approaches infinity.

(d) This circuit has negative series voltage feedback with

$$\beta = \frac{v_f}{v_o} = \frac{R_2 || (R_1 + R_2)}{R_1 + R_2 || (R_1 + R_2)} \times \frac{R_2}{R_1 + R_2} = \frac{R_2^2}{R_1^2 + 3R_1R_2 + R_2^2}$$

where as usual $R_2||(R_1 + R_2)$ denotes the parallel combination of R_2 and $(R_1 + R_2)$. For very large loop gain, the amplifier tends toward an ideal voltage amplifier with $A_{vf} = 1/\beta = 1 + 3(R_1/R_2) + (R_1/R_2)^2$, the input impedance approaches infinity, and the output impedance approaches zero.

Problem 9.39

Many correct answers exist. One is the circuit of Figure P9.38d. Using the result of Problem 9.38d, we have

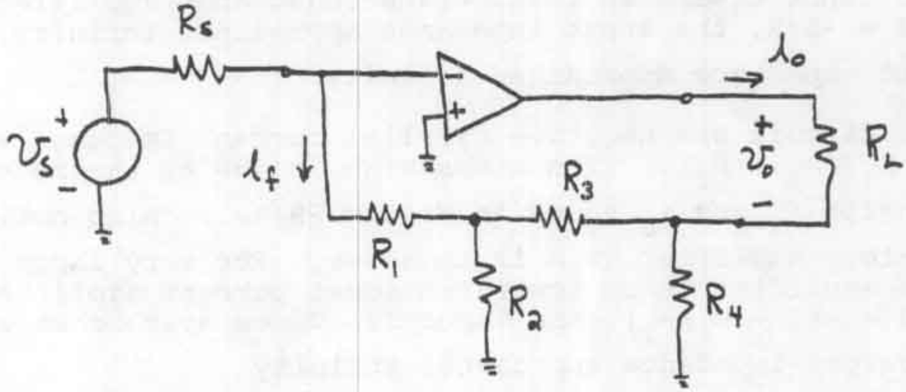
$$\beta = 0.01 = \frac{R_2^2}{R_1^2 + 3R_1R_2 + R_2^2}$$

$$1/\beta = 100 = 1 + 3(R_1/R_2) + (R_1/R_2)^2$$

Solving we obtain $R_1/R_2 = 8.56$. Thus we could use $R_2 = 10$ kΩ and $R_1 = 85.6$ kΩ. Of course other resistance values would work as long as their ratio is correct.

Problem 9.40

Here is a suitable circuit configuration:



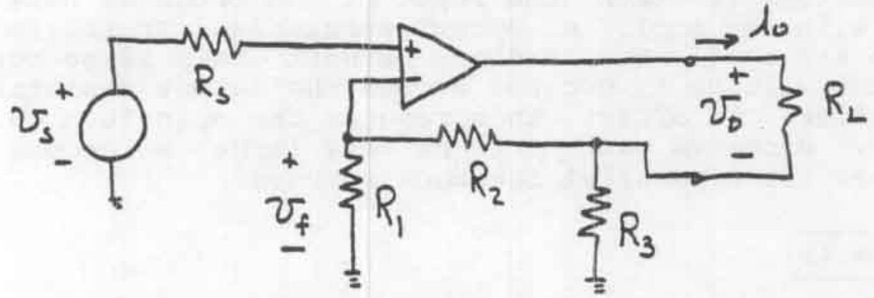
By repeated application of the current divider principle, we have

$$\beta = \frac{i_f}{i_o} = -\frac{R_2}{R_1 + R_2} \times \frac{R_4}{R_3 + (R_1||R_2) + R_4}$$

One set of resistances that meets the objective is $R_1 = 909$ Ω, $R_2 = 100\ \Omega$, $R_3 = 909\ \Omega$, and $R_4 = 113\ \Omega$. Many other correct solutions exist.

Problem 9.41

Here is a suitable circuit configuration:



Using the current divider principle and Ohm's law, we have

$$\beta = \frac{v_f}{i_o} = R_1 \times \frac{R_3}{R_1 + R_2 + R_3}$$

A suitable choice of resistances is $R_1 = 1\ k\Omega$, $R_2 = 8\ k\Omega$ and $R_3 = 1\ k\Omega$ (8.06 kΩ is a standard 1%-tolerance value). Many other correct solutions to this problem exist.

Problem 9.42

In series feedback, the output port of the feedback network is in series with the amplifier input terminals. Thus, the output resistance of the feedback network is in series with the amplifier input. If the feedback resistors are very large, a significant part of the source voltage appears across this output resistance instead of across the amplifier input terminals. In effect, this reduces the open-loop gain of the amplifier. Since we want $A\beta$ to be very large, we try to choose small resistances in a series feedback network.

Problem 9.43

In parallel feedback, the output port of the feedback network is in parallel with the amplifier input terminals. Thus, the output resistance of the feedback network is in parallel with the amplifier input. If the feedback resistors are very small, a significant part of the source current flows through this output resistance instead of into the amplifier input terminals. In effect, this reduces the open-loop gain of the amplifier. Since we want $A\beta$ to be very large, we choose large resistances for a parallel feedback network.

Problem 9.44

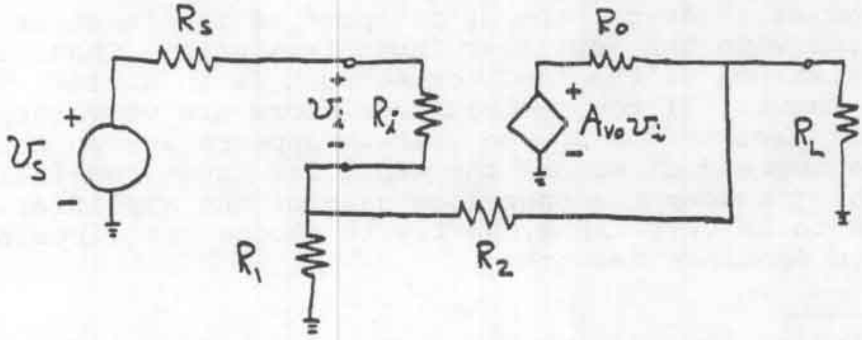
In voltage feedback, the input of the feedback network is in parallel with the amplifier output terminals. If the feedback resistors are small, the feedback network draws large current and significant voltage is dropped across the output resistance of the amplifier. In effect, this reduces the open-loop gain of the amplifier. Since we want $A\beta$ to be very large, we choose large resistances for a parallel feedback network.

Problem 9.45

In current feedback, the input of the feedback network is in series with the amplifier output terminals. If the feedback resistors are large, significant voltage is dropped across the input resistance of the feedback network. In effect, this reduces the open-loop gain of the amplifier. Since we want $A\beta$ to be very large, we choose large resistances for a parallel feedback network.

Problem 9.46

To attain a nearly ideal voltage amplifier, we should use series voltage feedback. A suitable circuit configuration is



Because $A_{vf} \cong 1/\beta$ we want $R_1/(R_1 + R_2) = \beta \cong 0.01$. To avoid problems with loading, we want $R_1 << R_i$ and $R_1 + R_2 >> R_o$. A good choice is $R_1 = 1$ kΩ and $R_2 = 100$ kΩ. Using the formulas of Table 9.1 we have:

$A_{vf} = A_v/(1 + A_v\beta) = 5000/[1 + 5000(1/101)] = 99.0$
$R_{if} = R_i(1 + A_v\beta) = 5.05\ M\Omega$
$R_{of} = R_o/(1 + A_v\beta) = 0.99\ \Omega$

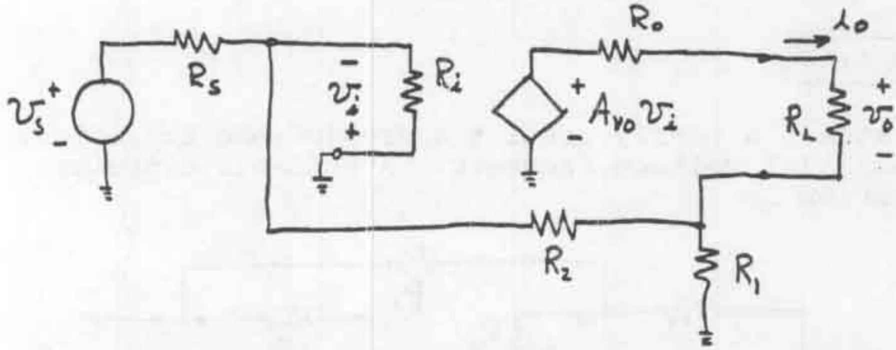
Using a PSpice transfer function analysis yields:

$A_{vf} = 98.86 \quad R_{if} = 4.82\ M\Omega \quad R_{of} = 1.01\ \Omega$

(The formulas in Table 9.1 do not account for loading effects of the feedback network and are therefore approximate.)

Problem 9.47

To attain a nearly ideal current amplifier, we should use parallel current feedback. A suitable circuit configuration is

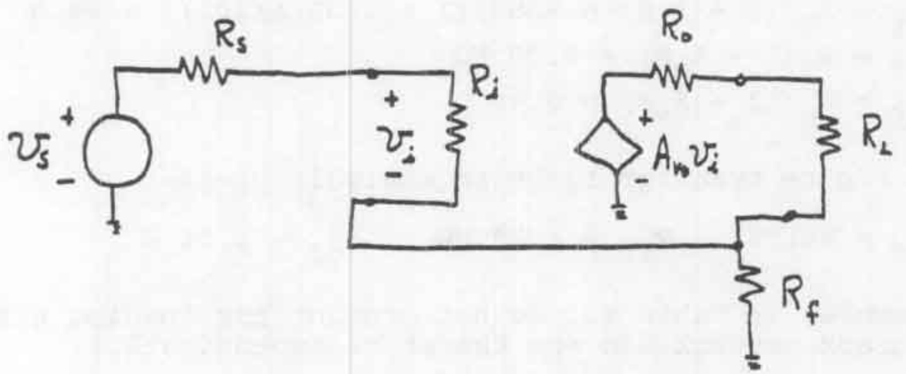


Because $A_{if} \cong 1/\beta$, we want $-R_1/(R_1 + R_2) = \beta \cong -0.01$. To avoid problems with loading, we want $R_2 >> R_i$ and $R_1||R_2 << R_o$. These requirements cannot all be met. A good compromise is $R_1 = 1\ k\Omega$ and $R_2 = 100\ k\Omega$. Because we do not have $R_2 >> R_i$ and $R_1||R_2 << R_o$, loading effects are significant. Thus if we neglect loading effects and use the formulas of Table 9.1, the results are inaccurate. Instead we use a PSpice analysis, from which we obtain:

$A_{if} = -100.9 \quad R_{if} = 41.2\ \Omega \quad R_{of} = 49.6\ \Omega$

Problem 9.48

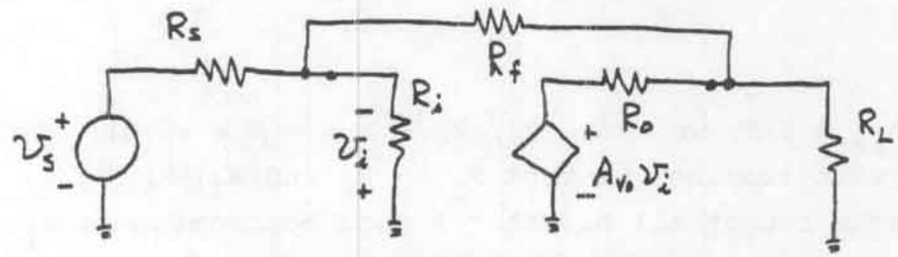
To attain a nearly ideal transconductance amplifier, we use series current feedback. The circuit configuration is:



We need $\beta = R_f \cong 1/G_{mf} = 500\ \Omega$. Using SPICE, we determine that $G_{mf} = 1.999 \times 10^{-3}$ S, $R_{if} = 161.4$ MΩ and $R_{of} = 2.46$ MΩ. Because we have $R_{if} >> R_s$ and $R_{of} << R_L$ the circuit is nearly an ideal transconductance amplifier.

Problem 9.49

To attain a nearly ideal transresistance amplifier, we choose parallel voltage feedback. A suitable circuit configuration is



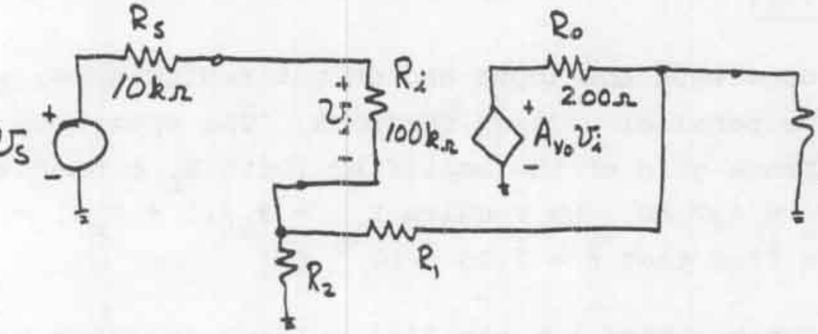
We need $\beta = -1/R_f = 1/R_{mf}$ thus we choose $R_f = R_{mf} = 5$ kΩ. Because we do not have $R_f >> R_i$, loading effects are significant, and we use SPICE to analyze the circuit. This yields:

$R_{mf} = 5000\ \Omega \quad R_{if} = 1.06\ \text{M}\Omega \quad R_{of} = 0.0604\ \Omega$

Problem 9.50

(a) To increase input resistance and reduce output resistance, we need to use negative series voltage feedback. Neglecting loading, we have $R_{if} = (1 + A_v\beta)R_i = (1 + 5000\beta)100\ \text{k}\Omega = 1\ \text{M}\Omega$. Solving we determine that $\beta = 1.8 \times 10^{-3}$.

(b) A suitable circuit configuration is:



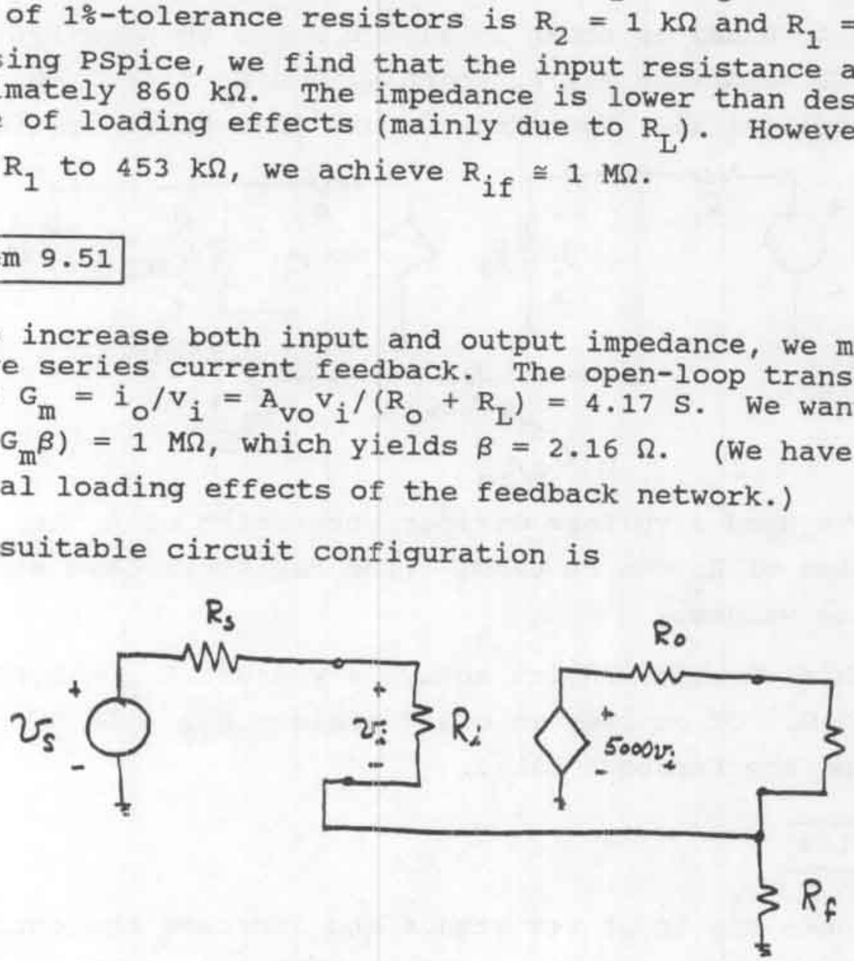
To avoid loading, we want $R_2 << R_i$ and $R_1 >> R_o$. A suitable choice of 1%-tolerance resistors is R_2 = 1 kΩ and R_1 = 549 kΩ.

(c) Using PSpice, we find that the input resistance achieved is approximately 860 kΩ. The impedance is lower than desired because of loading effects (mainly due to R_L). However, if we reduce R_1 to 453 kΩ, we achieve $R_{if} \cong 1$ MΩ.

Problem 9.51

(a) To increase both input and output impedance, we must use negative series current feedback. The open-loop transconductance gain is $G_m = i_o/v_i = A_{vo}v_i/(R_o + R_L)$ = 4.17 S. We want $R_{if} = R_i(1 + G_m\beta)$ = 1 MΩ, which yields β = 2.16 Ω. (We have neglected potential loading effects of the feedback network.)

(b) A suitable circuit configuration is

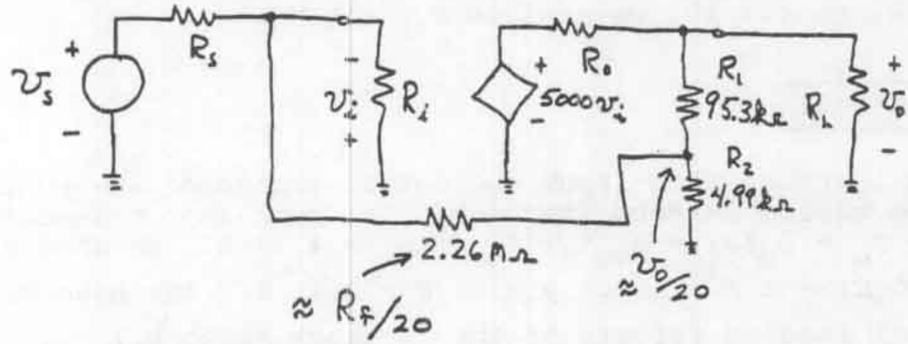


in which $R_f = \beta$ = 2.16 Ω. We have $R_f << R_i$ and $R_f << R_o$, so loading by the feedback network is negligible. PSpice analysis yields R_{if} = 998 kΩ and R_{of} = 10.0 kΩ.

Problem 9.52

(a) To reduce both the input and output resistances, we need to use negative parallel voltage feedback. The open-loop transresistance gain of the amplifier (with R_L connected) is $R_m = v_o/i_i = A_v R_i = 417\ M\Omega$. We require $R_{if} = R_i/(1 + R_m\beta) = 10\ k\Omega$. Solving, we find that $\beta = 2.16 \times 10^{-8}$ S.

(b) One configuration for parallel voltage feedback simply places a resistance R_f between the inverting input terminal and the output terminal as shown in Figure 9.19c on page 578. For this circuit we have $\beta = 1/R_f$ which yields $R_f = 46.3\ M\Omega$. This value is impractical. Therefore we use this configuration:



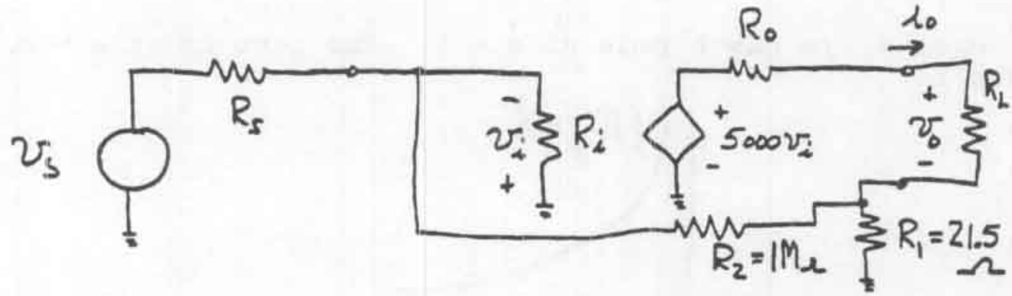
Here we have used a voltage divider consisting of R_1 and R_2 so a smaller value of R_f can be used. (The resistors have standard 1%-tolerance values.)

(c) For this circuit, PSpice analysis yields: $R_{if} = 9.82\ k\Omega$ and $R_{of} = 100.2\ \Omega$. Of course, we could achieve $R_{if} = 10\ k\Omega$ exactly by adjusting the feedback ratio.

Problem 9.53

(a) To reduce the input resistance and increase the output resistance, we need to use negative parallel current feedback. We have an open-loop current gain $A_i = A_{vo}R_i/(R_o + R_L) = 4.17 \times 10^5$. We want $R_{if} = 10\ k\Omega = R_i/(1 + \beta A_i)$ which yields $\beta = 2.15 \times 10^{-5}$.

(b) A suitable circuit configuration is



For this circuit, we have $\beta = R_1/(R_1 + R_2)$ and the resistance values shown achieve the desired feedback ratio.

(c) PSpice analysis reveals that the circuit has $R_{if} = 10.1$ kΩ and $R_{of} = 1.19$ kΩ.

Problem 9.54

See Figure 9.32 on page 597 in the book.

Problem 9.55

See Figure 9.31 on page 596 in the book.

Problem 9.56

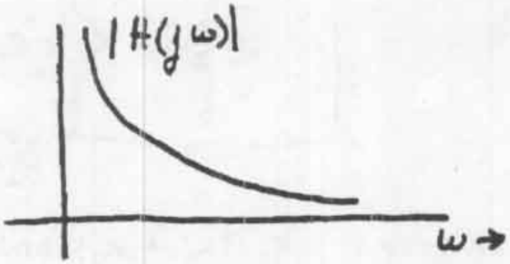
Poles in the right-half plane produce responses that grow exponentially until the system is driven into nonlinear operation. Usually the response settles into a constant-amplitude distorted sine wave. Poles on the $j\omega$ axis produce constant-amplitude sinusoidal responses.

Problem 9.57

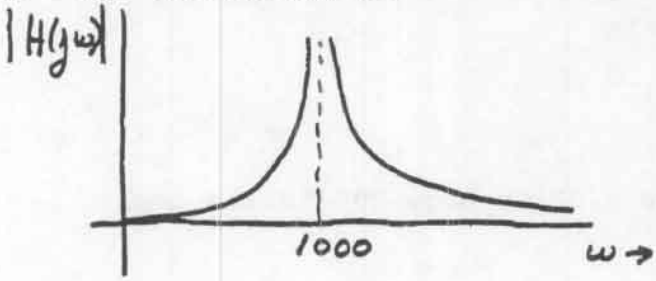
We imagine laying a sheet of rubber over the complex s-plane. The sheet is nailed down at the locations of zeros (including the periphery at $s = \infty$, if there are zeros at $s = \infty$). The sheet is pushed up by infinitely high thin posts at the locations of poles. The imagined height of the sheet above the $j\omega$ axis is proportional to the magnitude of the network function versus ω.

Problem 9.58

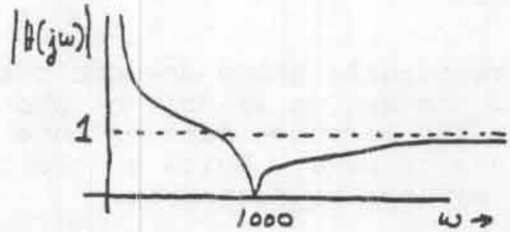
(a) $H(s) = 1/s$ has a pole at $s = 0$. The zero is at $s = \infty$. The sketch is:



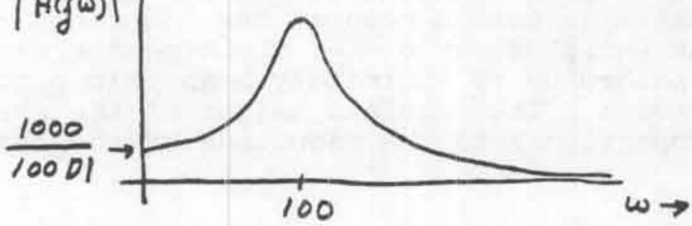
(b) $H(s) = s/(s^2 + 10^6)$ has poles at $s = \pm j10^3$, a zero at $s = 0$ and a zero at $s = \infty$. The sketch is:



(c) $H(s) = (s^2 + 10^6)/s^2$ has a double pole at $s = 0$ and zeros at $s = \pm j10^3$. Notice that as s approaches ∞, H(s) approaches unity. The sketch is



(d) $H(s) = (s + 1000)/(s^2 + 2s + 10001)$ has poles at $s = -1 \pm j100$, a zero at $s = -1000$ and a zero at $s = \infty$. The sketch is:



Problem 9.59

(a) transient response = Aexp(-t)

(b) transient response = Asin(1000t) + Bcos(1000t)

(c) transient response = Aexp(-3t) + Bexp(-4t)

(d) transient response = Aexp(-t)sin(1000t) + Bexp(-t)cos(1000t) in which A and B are constants that depend on initial conditions, the excitation and the zeros.

Problem 9.60

The product of the closed-loop dc gain and the half-power bandwidth of a dominant pole amplifier is constant with respect to changes in the feedback ratio β. As dc gain is reduced, the half-power bandwidth increases.

Problem 9.61

A single-pole is always stable with negative feedback because its pole remains on the negative real axis in the s-plane as β increases.

Because its poles move outward along a vertical line that lies in the left-half plane as β increases, a two-pole amplifier remains stable for all values of β, but it can display undesirable overshoot and ringing in its transient response and peaks in its frequency response.

The poles of an amplifier with three or more poles can move into the right-half plane so the amplifier becomes unstable for sufficiently large values of β.

Problem 9.62

A macromodel is a circuit that models certain external characteristics of an amplifier. It usually does not resemble the internal circuits of the amplifier.

Problem 9.63

For a single-pole amplifier, we have $A_{0f}f_{bf} = A_0 f_b = 1000 \times 1000$ Hz $= 10^6$. Thus for $A_{0f} = 10$, the bandwidth is $f_{bf} = 10^5$ Hz. The closed-loop pole is located at $s_p = -2\pi \times 10^5$ and the time constant is $\tau = -1/s_p = 1.59\ \mu s$. For $A_{0f} = 1$, the bandwidth is $f_{bf} = 10^6$Hz and the time constant is $0.159\ \mu s$.

Problem 9.64

Using Equation 1.19 (page 47 in the book), we have $B = f_{bf} \cong 0.35/t_r = 0.35/(1\ \mu s) = 350$ kHz. Thus the gain-bandwidth product is $A_{0f}f_{bf} = 100 \times 350$ kHz $= 35$ MHz. Then the open-loop bandwidth is $f_b = (35 \text{ MHz})/A_0 = (35 \text{ MHz})/10^5 = 3500$ Hz.

Problem 9.65

The poles are given by Equation 9.50:

$$s = -\frac{1}{2}(2\pi f_1 + 2\pi f_2) \pm \frac{1}{2}\sqrt{(2\pi f_1 + 2\pi f_2)^2 - 16\pi^2 f_1 f_2(1 + A_0\beta)}$$

substituting $f_1 = 1000$, $f_2 = 500$, $A_0 = 1000$, and $\beta = 0.1$, we eventually obtain

$$s = -4712 \pm j\ 44.4 \times 10^3$$

Problem 9.66

The closed-loop poles are the roots of

$$\beta A(s) + 1 = 0$$

For this problem, we have $\beta = 1$, and

$$A(s) = \frac{10^5}{[s/\omega_1 + 1][s/\omega_2 + 1][s/\omega_3 + 1]}$$

in which $\omega_1 = 2\pi(5 \times 10^6)$, $\omega_2 = 2\pi(20 \times 10^6)$ and $\omega_3 = 2\pi f_3$. Rearranging, we have

$$s^3 + s^2(\omega_1 + \omega_2 + \omega_3) + s(\omega_1\omega_2 + \omega_1\omega_3 + \omega_2\omega_3) + (10^5 + 1)\omega_1\omega_2\omega_3 = 0$$

We used the MATLAB command, roots(p), to determine the roots of this polynomial, adjusting the value of f_3 by trial and error to determine the value at which the roots become imaginary. This turns out to be $f_3 = 11$ Hz.

Problem 9.67

We have a two-pole amplifier, for which the closed-loop poles are given by Equation 9.50:

$$s = -\frac{1}{2}(2\pi f_1 + 2\pi f_2) \pm \frac{1}{2}\sqrt{(2\pi f_1 + 2\pi f_2)^2 - 16\pi^2 f_1 f_2(1 + A_0\beta)}$$

Substituting $A_0 = 500$, $f_1 = 100/2\pi$, $f_2 = 1000/2\pi$, and $\beta = 1$, we eventually find that the poles are

$$s = -550 \pm j\,7057 = -\sigma \pm j\omega$$

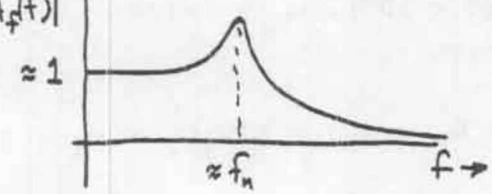
Then using Equations 9.36, 9.37 and 9.38 (page 594 in the book), we obtain

$$\omega_n = \sqrt{\sigma^2 + \omega^2} = 7078$$

$$\delta = \frac{\sigma}{\omega_n} = 0.0777$$

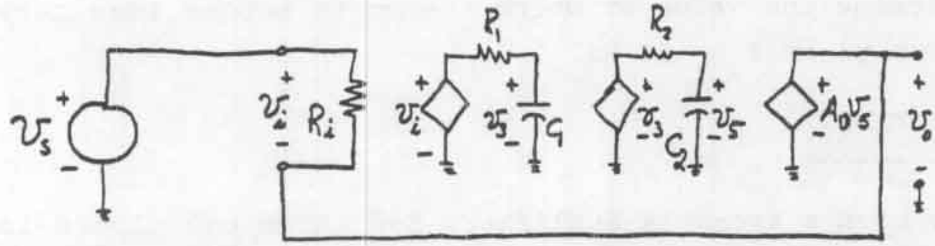
$$Q = \frac{1}{2\delta} = 6.43$$

The zeros of the closed-loop transfer function are at ∞. Using the rubber-sheet analogy we obtain the sketch:

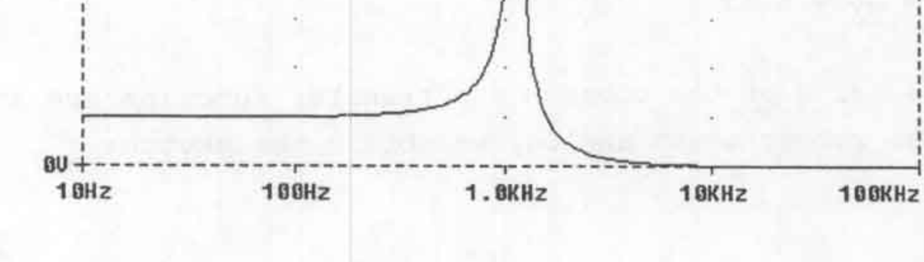


Problem 9.68

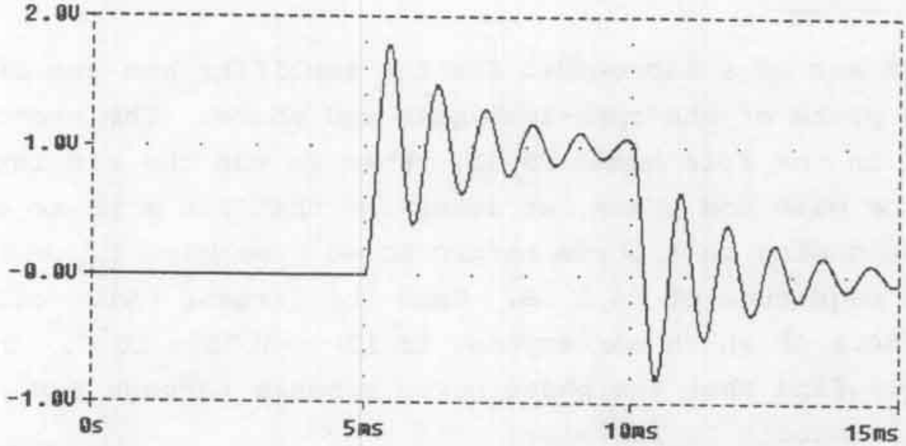
Here is a macromodel for the feedback amplifier:



We have assumed an open-loop output impedance of zero and a very high value (1 MΩ) for the open-loop input resistance. Arbitrarily we chose $R_1 = R_2 = 10$ kΩ. Then to achieve poles at $s_{p1} = -100$ and $s_{p2} = -1000$, the capacitances need to be $C_1 = -1/Rs_{p1} = 1\ \mu F$ and $C_2 = -1/R_2 s_{p2} = 0.1\ \mu F$. The schematic is stored in the file named P9_68. We set up the input source as 1 V for the ac analysis and as a 1-V 5-ms pulse for the transient analysis. The closed-loop gain magnitude is plotted versus frequency:



The pulse response is:



Problem 9.69

Gain margin is the amount (in dB) by which the loop-gain magnitude is less than 0 dB at the frequency f_{GM} for which the phase shift of the loop gain is 180°.

Phase margin is 180° plus the phase of the loop gain at the frequency f_{PM} for which the loop-gain magnitude is unity (0 dB). For example if the loop gain has a phase of -135° at f_{PM}, the phase margin is 45°.

Problem 9.70

As a general rule of thumb, we design feedback amplifiers to have gain margins of at least 10 dB and phase margins of at least 45°. Otherwise the transient response displays overshoot and ringing and the frequency response displays a high peak. Both of these characteristics are usually undesirable.

Problem 9.71

The phase margin for a single pole amplifier approaches 90° (from higher values) as $A_0\beta$ becomes large.

Problem 9.72

We set up a macromodel for the amplifier and use SPICE to obtain plots of the open-loop gain and phase. The macromodel is stored in the file named P9_72. When we run the simulation and plot the gain and phase, we determine that for a phase of 120° (corresponding to a phase margin of 60°) we have $f_{PM} \cong 77$ Hz and a gain magnitude of 54.2 dB. Thus the largest value allowed for β is -54.2 dB which corresponds to $|\beta| = 1.95 \times 10^{-3}$. Using the plots we find that the phase never crosses through 180°. Thus the gain margin is infinite.

Problem 9.73

We set up a macromodel for the amplifier and use SPICE to obtain plots of the open-loop gain and phase. The macromodel is stored in the file named P9_73. When we run the simulation and plot the gain and phase, we determine that for a phase of 120° (corresponding to a phase margin of 60°) we have $f_{PM} \cong 51$ Hz and a gain magnitude of 58.4 dB. Thus the largest value allowed for β is -58.4 dB which corresponds to $|\beta| = 1.20 \times 10^{-3}$. We also find that the gain is 43.1 dB at $f_{GM} = 152$ Hz. Thus the gain margin is 58.4 - 43.1 = 15.3 dB.

Problem 9.74

Compensation of an amplifier to be used with feedback consists of modifying its open-loop gain and phase so adequate gain and phase margins are obtained with the desired feedback ratio. Compensation is sometimes needed to avoid overshoot, ringing, sharp frequency response peaks, and/or instability. Compensation is never needed for a single-pole amplifier. Compensation may be needed for amplifiers with two or more poles.

Problem 9.75

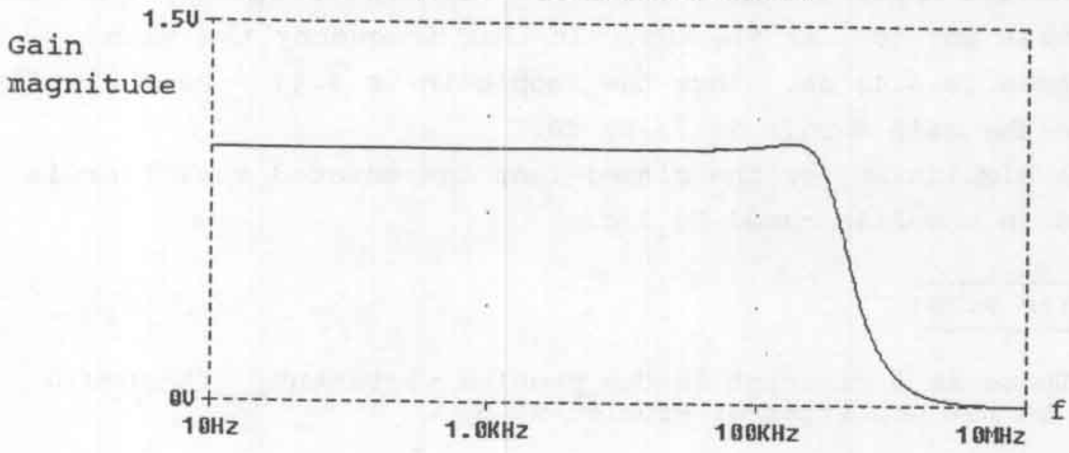
Dominant-pole compensation either adds a (very low frequency) open-loop pole or moves an existing open-loop pole to a much lower frequency.

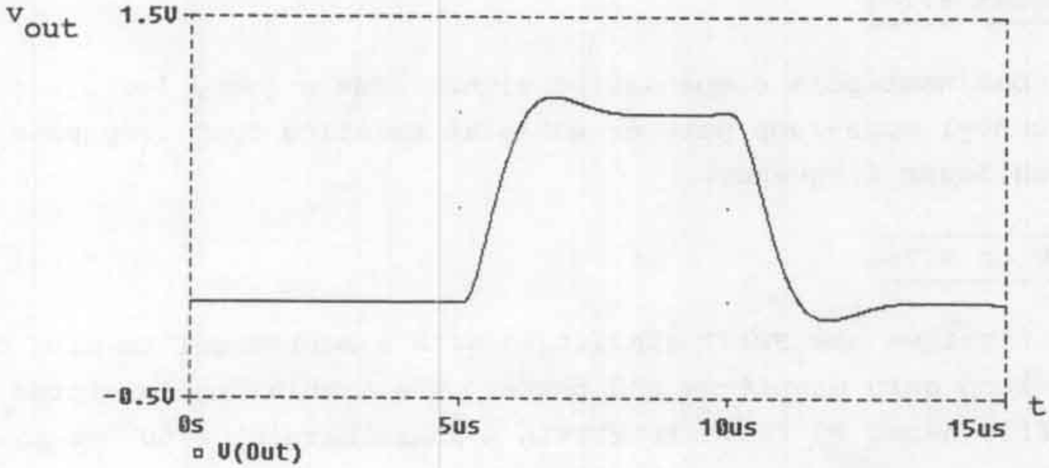
Problem 9.76

First we use SPICE simulation with a macromodel to plot the open-loop gain magnitude and phase. The simulation is stored in the file named P9_76a. To attain a phase margin of 60° we look for the frequency at which the uncompensated phase is -30° because we anticipate that the compensating pole will contribute -90°. This frequency turns out to be 244 kHz and at that frequency the gain magnitude is 79 dB. Thus the compensating pole must contribute an attenuation of 79 dB at 244 kHz. Thus we have $f_C = (244\ \text{kHz})/10^{(79/20)} = 27.4$ Hz.

A simulation for the open-loop gain and phase of the compensated amplifier is in file P9_77b. The frequency at which the phase is -180° is 1.28 MHz. At that frequency the gain magnitude is -22.5 dB. This is the loop gain because $\beta = 0$ dB. Thus the gain margin is 22.5 dB.

A simulation for the closed-loop compensated amplifier is stored in the file named P9_76c. The resulting closed-loop gain magnitude and pulse response are shown below:





Problem 9.77

First we use SPICE simulation with a macromodel to plot the open-loop gain magnitude and phase. (See file P9_77a.) To attain a phase margin of 60°, we look for the frequency at which the uncompensated phase is -30° (because we anticipate that the compensating pole will contribute -90°). This frequency turns out to be 177 kHz and at that frequency the gain magnitude is 99.6 dB. Thus keeping in mind that β = -20 dB, the compensating pole must contribute an attenuation of 79.6 dB at 177 kHz. Thus we have $f_C = (177\text{ kHz})/10^{(79.6/20)} = 18.5\text{ Hz}$.

A simulation for the open-loop gain and phase of the compensated amplifier is in file P9_77b. The frequency at which the phase is -180° is 576 kHz. At that frequency the gain magnitude is 6.41 dB. Thus the loop gain is 6.41 - 20 = -13.59 dB and the gain margin is 13.59 dB.

A simulation for the closed-loop compensated amplifier is stored in the file named P9_77c.

Problem 9.78

There is a misprint in the problem statement. It should refer to the amplifier of Problem 9.76.

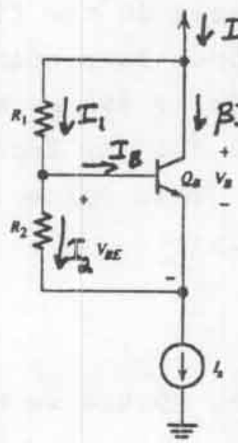
First, we use SPICE simulation with a macromodel to plot the open-loop gain magnitude and phase of the amplifier without the pole at f_1. (See file P9_78a.) To attain a phase margin of 60°, we look for the frequency at which the uncompensated phase is -30° (because we anticipate that the compensating pole will contribute -90°). This frequency turns out to be 1.80 MHz and at that frequency the gain magnitude is 79.3 dB. Thus the compensating pole must contribute an attenuation of 79.3 dB at 1.80 MHz. Thus we have $f_1' = (1.80\text{ MHz})/10^{(79.3/20)} = 195$ Hz.

A simulation to obtain open-loop gain and phase is stored in the file named P9_78b. The gain margin turns out to be 17.8 dB (for $\beta = 1$).

A simulation for the closed-loop compensated amplifier is stored in the file named P9_78c.

Problem 9.79

(a)



From the circuit we can write:

$I_2 = V_{BE}/R_2 \qquad I_1 = I_2 + I_B \qquad I_s = I_1 + \beta I_B \qquad V_B = I_1 R_1 + V_{BE}$

Using algebra, we eventually obtain:

$$V_B = V_{BE}\frac{R_1 + R_2}{R_2} + R_1\frac{I_s - V_{BE}/R_2}{\beta + 1} \qquad (1)$$

Assuming that β is very large, the second term on the right-hand side of the previous equation becomes negligible, and we have:

$$V_B \cong V_{BE} \frac{R_1 + R_2}{R_2} \qquad (2)$$

(b) If R_1 and R_2 are too small in value, the current I_s might not be large enough to cause sufficient voltage drop across R_2 so that the transistor turns on.

(c) Substituting values into Equation (2), we have

$$1.5 = 0.6 \frac{R_1 + 2}{2}$$

Solving, we determine $R_1 = 3$ kΩ.

Problem 9.80

Use the library file named Fig9_62.lib. The simulation of the open-loop circuit is stored in the file named P9_80. We use the simulation to plot the open-loop gain magnitude and phase. We need to have a phase shift of 45° at the frequency for which the gain magnitude crosses 0 dB. By trial and error, we find that $C_x = 7.2$ μF is needed. This value is much too large for implementation within an IC.

Problem 9.81

For the system of Figure P9.81a we have:

$$A_{fa} = \frac{A_1A_2}{1 + \beta A_1A_2}$$

For the system of Figure P9.81b, we have:

$$A_{fb} = \frac{A_1}{1 + \beta_1A_1} \times \frac{A_2}{1 + \beta_2A_2}$$

Evaluating, we find the values given in the table:

	$A_1 = 100$	$A_1 = 90$	% change
A_{fa}	99.01	98.90	0.11%
A_{fb}	82.64	81.82	1.0%

Thus, overall feedback is better for obtaining precision values of closed-loop gain.

Problem 9.82

Refer to the circuit diagram shown in Figure 9.65 in the book. The differential voltage gain is given approximately by the equation on page 636 in the book: $A_v \cong R_7/R_3 = 12.5$. The current I_1 splits equally between Q_1 and Q_2. Thus $I_{CQ1} = I_{CQ2} = I_1/2 = 1$ mA. Similarly $I_{CQ3} = I_{CQ4} = I_2/2 = 1$ mA. Also $I_{CQ5} \cong I_3 = 2$ mA and $I_{CQ6} \cong I_4 = 2$ mA. The voltages at the collectors of Q_3 and Q_4 are both equal to $V_{CC} - I_{CQ3}R_5 = 5 - 1 = 4$ V. Then the output voltages are $4 - V_{BE5} = 3.4$ V.

The simulation is stored in P9_82. The midband differential gain turns out to be 10.46 compared to the approximate computed value of 12.5. The bias points agree reasonably well with the approximate analysis. The half-power bandwidth is 1.80 MHz.

Problem 9.83

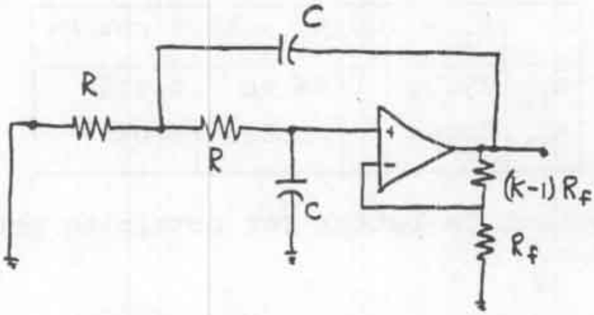
See Figure 9.68 on page 637 in the book.

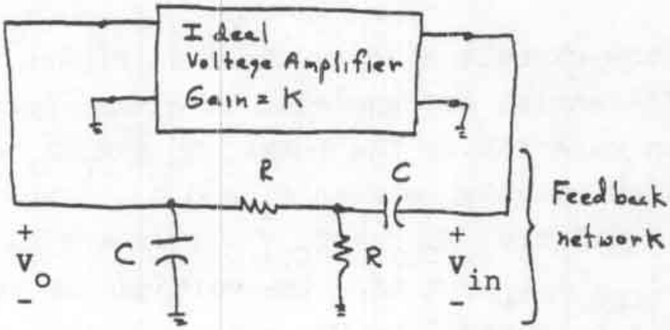
Problem 9.84

The Barkhausen criterion for linear oscillators, states that the frequency of oscillation is the frequency for which the loop gain has 0° phase shift. Furthermore, oscillation occurs only if the magnitude of the loop gain exceeds unity. In mathematical terms, the Barkhausen criterion is $A(f)\beta(f) = 1$.

Problem 9.85

The op amp and the resistors $(K - 1)R_f$ and R_f form an ideal voltage amplifier with an open-circuit voltage gain of K.





Analysis of the feedback network yields:

$$\beta(f) = \frac{V_o}{V_{in}} = \frac{1}{3 + j[\omega RC - 1/(\omega RC)]}$$

(Keep in mind that the input is on the right-hand side of the β network and the output is on the left-hand side.) Then the Barkhausen criterion requires $K\beta(f) = 1$. This eventually yields $K = 3$ (or greater) and $\omega = 1/RC$.

Problem 9.86

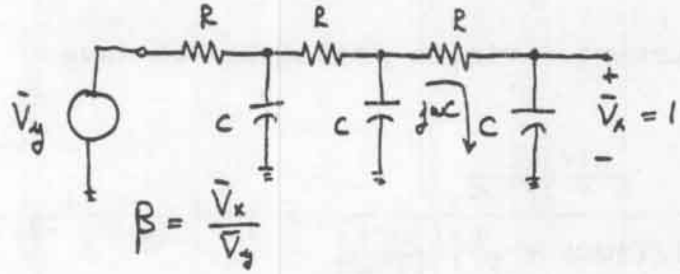
(a) $$\beta(f) = \frac{\dfrac{R(j\omega L)}{R + j\omega L}}{2R + j\omega 2L + \dfrac{R(j\omega L)}{R + j\omega L}} = \frac{1}{5 - j[2R/(\omega L) - 2\omega L/R]}$$

Then $A\beta = 1$ yields $A = 5$ (or greater) and $\omega = R/L$. Because A is positive, a noninverting amplifier is needed.

(b) $\beta = \frac{R}{3R + j\omega L - j/(\omega C)} = \frac{1}{3 + j[(\omega L/R) - 1/(\omega RC)]}$

Then $A\beta = 1$ yields $A = 3$ (or greater) and $\omega = 1/\sqrt{LC}$. Because A is positive, a noninverting amplifier is needed.

(c) The feedback network is:



Our approach is to assume that the output V_x is 1 V and to work back though the circuit to determine V_y. Then $\beta = 1/V_y$. This yields:

$$\beta = \frac{1}{1 - 5R^2\omega^2C^2 + j(6R\omega C - R^3\omega^3C^3)}$$

Finally setting $A\beta = 1$ yields A = 29 or greater and $\omega = \sqrt{6}/(RC)$. Thus a noninverting amplifier is needed.

(d) Here our approach is to set the loop gain to unity.

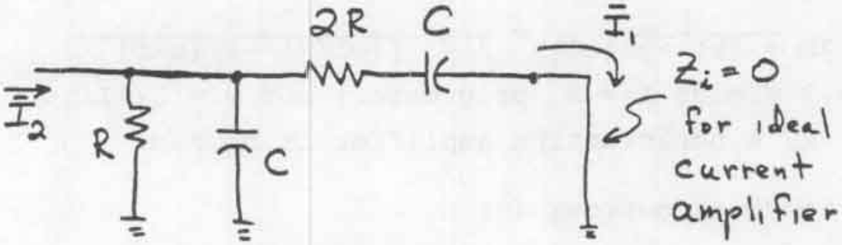
$$A\left(\frac{R}{R + 1/(j\omega C)}\right)^3 = 1$$

$$\frac{AR^3}{R^3 + 3R^2/(j\omega C) - 3R/(\omega C)^2 - 1/(j\omega C)^3} = 1$$

This yields $\omega = 1/(RC\sqrt{3})$ and $A = -8$. Thus an inverting amplifier with gain magnitude greater than 8 is required.

Problem 9.87

(a) The feedback network is:

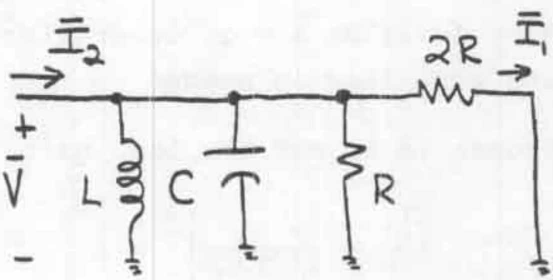


Applying the current division principle, we have

$$\beta = \frac{I_1}{I_2} = \frac{\dfrac{R/(j\omega C)}{R + 1/j\omega C}}{2R + 1/(j\omega C) + \dfrac{R/(j\omega C)}{R + 1/j\omega C}} = \frac{1}{4 + j[2\omega RC - 1/(\omega RC)]}$$

Then setting $A_i\beta = 1$, yields $A_i = 4$ (noninverting) and $\omega = 1/[RC\sqrt{2}]$.

(b) The feedback network is



$$V = I_2 \times \frac{1}{1/(j\omega L) + j\omega C + 1/R + 1/(2R)}$$

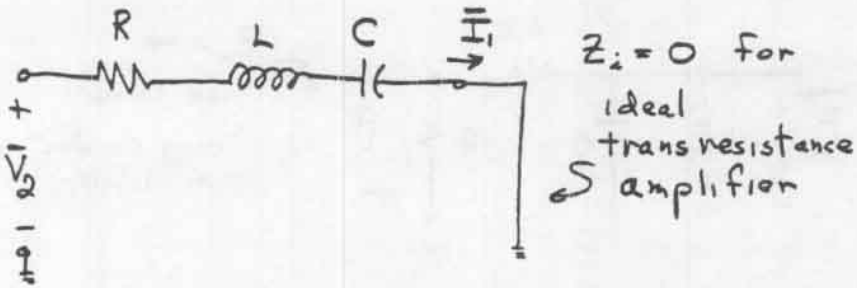
$$I_1 = V/2R = I_2 \times \frac{1}{2R[1/(j\omega L) + j\omega C + 1/R + 1/(2R)]}$$

$$\beta = \frac{I_1}{I_2} = \frac{1}{3 + j[2\omega RC - 2R/(\omega L)]}$$

Then setting $A_i\beta = 1$ yields $A_i = 3$ (noninverting) and $\omega = 1/\sqrt{LC}$.

Problem 9.88

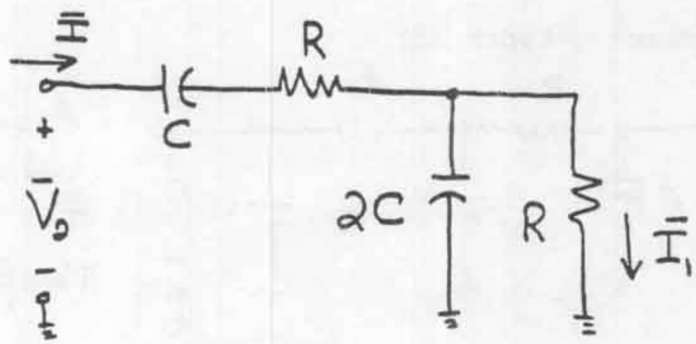
(a) The feedback network is:



$$\beta = \frac{I_1}{V_2} = \frac{1}{R + j(\omega L - 1/\omega C)}$$

Setting $R_m\beta = 1$, yields $R_m = R$ and $\omega = 1/\sqrt{LC}$

(b) The feedback network is:



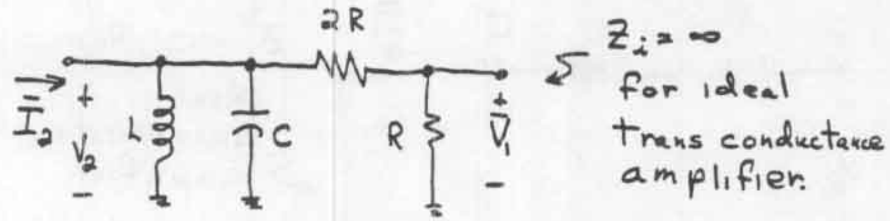
$$I_1 = \frac{I/(j\omega 2C)}{R + 1/(j\omega 2C)} = \frac{V_2 \dfrac{1/(j\omega 2C)}{R + 1/(j\omega 2C)}}{1/(j\omega C) + R + \dfrac{R/(j\omega 2C)}{R + 1/(j\omega 2C)}}$$

$$\beta = \frac{I_1}{V_2} = \frac{1}{4R + j[2R^2\omega C - 1/(\omega C)]}$$

Setting $R_m\beta = 1$ yields $R_m = 4R$ and $\omega = 1/(RC\sqrt{2})$.

Problem 9.89

(a) The feedback network is:

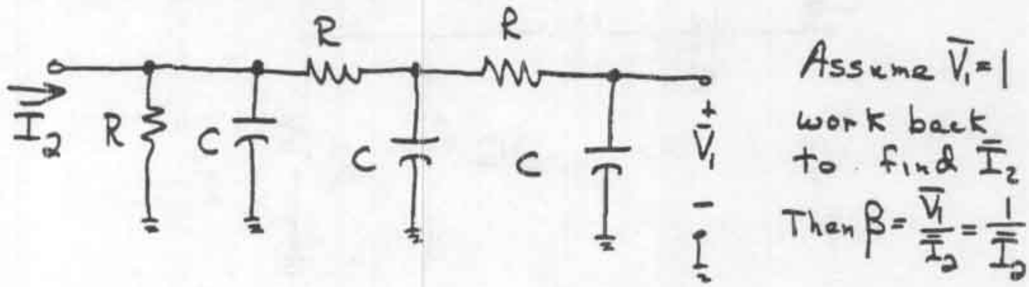


$$V_2 = I_2 \frac{1}{1/3R + j\omega C + 1/(j\omega L)} \qquad V_1 = V_2/3$$

$$\beta = \frac{V_1}{I_2} = \frac{1}{1/R + j3(\omega C - 1/\omega L)}$$

Setting $G_m\beta = 1$ yields $G_m = 1/R$ and $\omega = 1/\sqrt{LC}$.

(b) The feedback network is:



$$\beta = \frac{V_1}{I_2} = \frac{1}{1/R - 5\omega^2C^2R + j(6\omega C - \omega^3C^3R^2)}$$

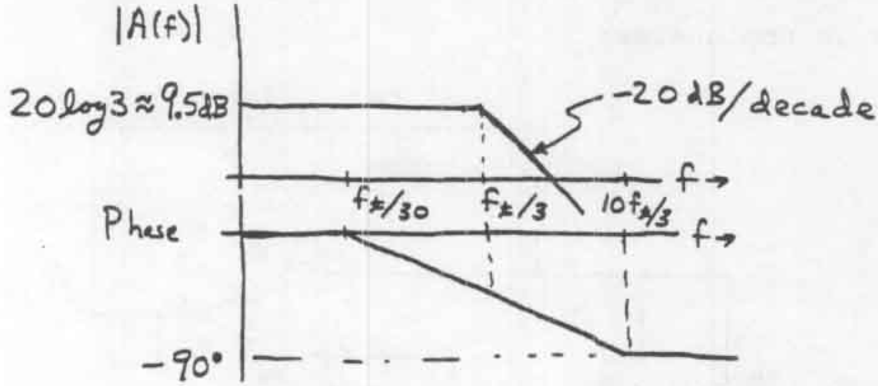
Setting $G_m\beta = 1$ yields $G_m = -29/R$ and $\omega = \sqrt{6}/RC$.

Problem 9.90

See Figure 9.73 on page 641 in the book.

Problem 9.91

With $R_2 = 2R_1$, the low-frequency closed loop gain of the amplifier is 3, and the closed-loop half-power bandwidth is $f_t/3$. The Bode magnitude and phase plots for the closed-loop gain are:



The phase shift departs from zero at approximately $f_t/30$. We conclude that if the frequency of oscillation exceeds $f_t/30$ the op amp will significantly influence the frequency.

Problem 9.92

In Exercise 9.25 we determined that the gain requirement is given by

$$A = 1 + R_2/R_1 \geq 1 + \frac{R_A}{R_B} + \frac{C_B}{C_A}$$

Rearranging we have

$$R_2 \geq R_1\left(\frac{R_A}{R_B} + \frac{C_B}{C_A}\right)$$

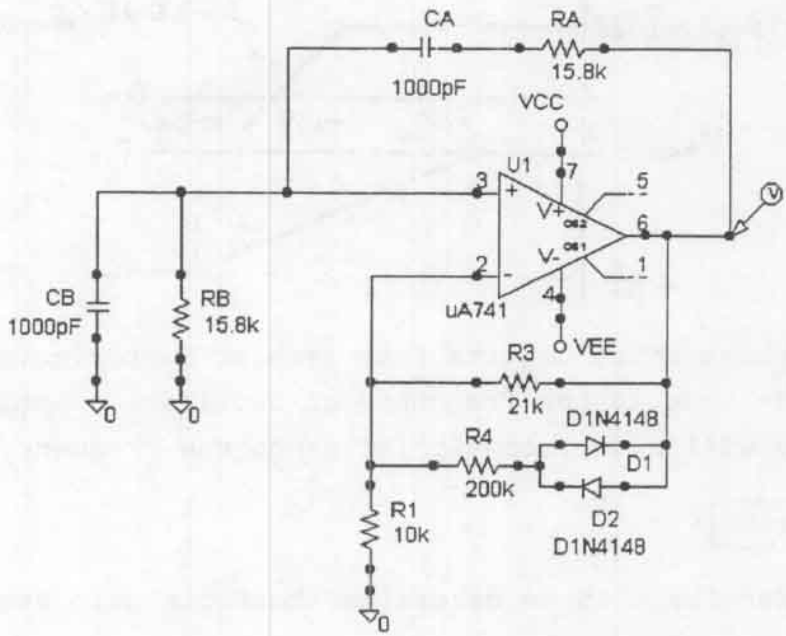
Assuming 5%-tolerance components and that the nominal value of R_1 is 10 kΩ, the largest value of right-hand side of this inequality becomes

$$R_2 = 1.05 \times 10\ \text{k}\Omega \times \left(\frac{1.05}{0.95} + \frac{1.05}{0.95}\right) = 23.2\ \text{k}\Omega$$

To ensure that the actual value of R_2 always exceeds the required value, we must choose the nominal value of R_2 to be 27 kΩ.

Problem 9.93

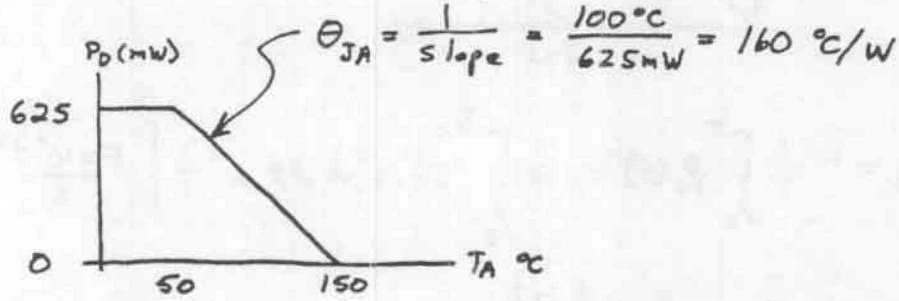
Here is one answer:



All resistors and capacitors are 5%-tolerance. The simulation is stored in the file named P9_93.

Chapter 10

Exercise 10.1



Exercise 10.2

$T_{Jmax} = 175°C \qquad P_{Dmax} = 15$ W @ $T_C = 25°C \qquad P_D = 5$ W

$\theta_{CS} = 1°C/W \qquad \theta = 5°C/W$

(a) $$\theta_{JC} = \frac{T_{Jmax} - 25}{P_{Dmax} \; @T_C = 25°} = \frac{175 - 25}{15} = 10°C/W$$

(b) $$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} = 10 + 1 + 5 = 16°C/W$$

$$T_J = T_A + P_D\theta_{JA} = 50 + 5 \times 16 = 130°C$$

$$T_C = T_A + P_D\theta_{CA} = 50 + 5(1 + 5) = 80°C$$

(c) $$T_A = T_J - P_D\theta_{JA} = 175 - 5(16) = 95°C$$

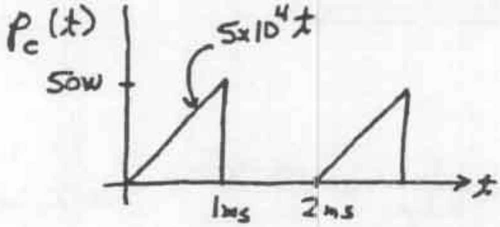
Exercise 10.3

(a) $$I_{Aavg} = \frac{1}{T}\int_0^T i_A(t)\,dt = \frac{1}{T}\int_0^{T/2} 1\,dt = 0.5 \text{ A}$$

$$P_A = V_A I_{Aavg} = 5 \text{ W}$$

(b) $p_B(t) = v_B(t)i_B(t) = 0$ for all t Therefore $P_B = 0$.

(c) $p_C(t) = v_C(t) i_C(t)$



$$P_c = \frac{1}{T}\int_0^T p_c(t) = \frac{1}{T}\int_0^{T/2} 5\times10^4 t\, dt = \frac{1}{T}\left[\frac{5\times10^4 t^2}{2}\right]_0^{T/2}$$

$$= \frac{1}{T}\quad\frac{5\times10^4\ T^2/4}{2} = 6.25\times10^3\, T$$

$$= 6.25\times10^3\times 2\times10^{-3} = 12.5\, W$$

Exercise 10.4

$P_o = 0$ because of zero signal amplitude

$P_{CC} = P_{EE} = V_{CC}I_{bias} = 12.85 \times 1.58 = 20.3$ W

$P_{bias} = V_{EE}I_{bias} = 12.85 \times 1.58 = 20.3$ W

$P_{Q1} = P_{CC} + P_{EE} - P_o = 20.3$ W

Exercise 10.5

For an open-circuit load, very little current flows through the diodes. Then the voltage across the filter capacitor approaches the peak ac input. Thus $v_C \cong 30$ V dc. However, the regulator maintains the load voltage at 15 V dc.

Exercise 10.6

Many correct answers exist. One possibility is to change the value of R_2 to 8 kΩ. (We assume that R_2 is adjustable so it need not be a standard value.) The simulation is stored in the file named Exer10_6.

Exercise 10.7

(a) For the circuit of Figure 10.36a, the output of the op amp is at least 0.5 lower than V_A. Furthermore V_B must be $2V_{BE}$ lower than the op amp output for the transistors to be in the active region. Thus the minimum value for V_{AB} (which is the dropout voltage) is 1.9 V.

(b) For the circuit of Figure 10.36b, the minimum value of V_{AB} is the saturation voltage of the BJT, which is approximately 0.2 V.

Exercise 10.8

There is a misprint in the statement of the Exercise, it should refer to Example 10.8. See Figure 10.42 on page 717 in the book. The simulation is stored in the file named Fig10_42b. Using SPICE, we find that the secondary current is approximately 2.6 A rms {request a plot of rms[i(D1) + i(D2)]}, the capacitor current is approximately 2.25 A rms, and the minimum load voltage is 9.5 V.

Problem 10.1

Assuming steady-state thermal conditions, the junction-to-case thermal resistance is temperature differential (i.e., the difference between the junction temperature and the case temperature) divided by the average power dissipation of the device.

Problem 10.2

As device designers we control junction-to-case thermal resistance by placing the chip in good thermal contact with a massive metal case. Also if the junction is of large area, the power dissipation is spread out reducing the peak temperature rise.

As circuit designers, we choose devices that have sufficiently low junction-to-case thermal resistance. Then we minimize the case-to-ambient thermal resistance by our choice of a heat sink and its mounting Furthermore, we make sure, perhaps by using thermally conductive grease, that the device case is in good thermal contact with the heat sink.

Problem 10.3

Sometimes we use a mica washer between the case of a power BJT and the heat sink to provide electrical insulation between the collector (which may be electrically connected to the case) and the heat sink.

Problem 10.4

Heat sinks should be mounted in a location and in an orientation that maximizes air flow over the fins of the sink.

Problem 10.5

A typical power-derating curve for a power transistor is shown in Figure 10.3 on page 670 in the book.

Problem 10.6

We assume that the junction is at its maximum allowed temperature for $T_C = 25^\circ$ and $P_D = 40$ W. Thus we have

$$\theta_{JC} = (T_J - T_C)/P_D = 3.75^\circ C/W$$

Problem 10.7

(a) The junction-to-case thermal resistance is minus the inverse of the slope of the derating curve, which is $150^\circ/(100\ W) = 1.5\ ^\circ C/W$.

(b) The maximum junction is the intersection of the derating curve with the temperature axis. Thus $T_{Jmax} = 200^\circ C$.

Problem 10.8

(a) $\theta_{JC} = (T_{Jmax} - T_C)/P_{Dmax} = (200 - 25)/15 = 11.67^\circ C/W$

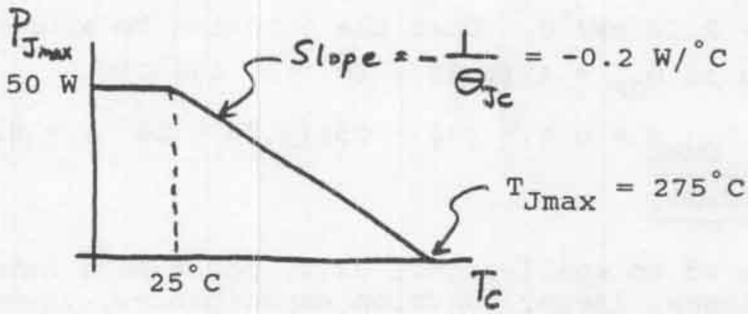
(b) $T_{Jmax} = (\theta_{JC} + \theta_{CS} + \theta_{SA})P_D + T_A$

$$\theta_{SA} = (T_{Jmax} - T_A)/P_D - \theta_{JC} - \theta_{CS}$$
$$= (200 - 75)/5 - 11.67 - 1$$
$$= 12.33^\circ C/W$$

(c) $T_C = T_A + P_D(\theta_{CS} + \theta_{SA}) = 75 + 5(1 + 12.33) = 141.7^\circ C$

Problem 10.9

(a)



(b) $T_{Jmax} = 275^\circ C$ (This is a very high value.)

(c) $\theta_{JC} = 5^\circ C/W$

Problem 10.10

The third sentence of the problem should read: "The case-to-sink thermal resistance is $\theta_{CS} = 0.5^\circ C/W$." Then we have

$$\theta_{JC} = (T_{Jmax} - T_C)/P_D = (200 - 25)/20 = 8.75^\circ C/W$$
$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} = (T_J - T_A)/P_D$$
$$\theta_{JA} = 8.75 + 0.5 + \theta_{SA} = (150 - 50)/5 = 20$$
$$\theta_{SA} = 10.75^\circ C/W$$

Problem 10.11

$$T_J = (0.7 - 0.5)/0.0025) + 25 = 105^\circ C$$

$$\theta_{JA} = (T_J - T_A)/P_D = (105 - 30)/(0.5) = 45^\circ C/W$$

Problem 10.12

(a) From page 867 we find that $P_{Dmax} = 1.2$ W at a case temperature of 25°C. This is to be derated at 6.85 mW/°C. The junction-to-case thermal resistance is $\theta_{JC} = 1/(6.85 \times 10^{-3}) =$ 146°C/W. (The thermal resistances are denoted as $R_{\theta JC}$ and $R_{\theta JA}$ on the data sheet, and their values are interchanged.)

(b) For an ambient temperature of 25°C, $P_{Dmax} = 0.4$ W derated by 2.28 mW/°C. Thus the junction to ambient thermal resistance is $\theta_{JA} = 1/(2.28 \times 10^{-3}) = 439$°C/W.

(c) $P_{Dmax} = 0.4 - (75 - 25)(2.28 \times 10^{-3}) = 0.286$ W

Problem 10.13

Compared to small-signal BJTs, power BJTs have larger junction areas, larger junction capacitances, lower βs, larger leakage currents, lower f_t's, and larger more massive cases.

Problem 10.14

As temperature increases, V_{BEQ} decreases, the leakage current I_{CBO} increases, and β increases. In most power amplifiers, all of these effects tend to raise I_{CQ} and dissipated power which leads to higher temperature and even higher values of I_{CQ} and P_D. In extreme cases, this can lead to thermal runaway and destruction of the device.

Problem 10.15

The maximum ratings to consider for a power BJT include junction temperature, collector current, collector-to-emitter voltage, and second breakdown.

Problem 10.16

Second breakdown occurs in BJTs with higher collector-to-emitter voltages that concentrate the current in a small part of the junction. This causes localized overheating of part of the junction.

Problem 10.17

Power MOSFETs require very little drive current (i.e., gate current) compared to that of power BJTs. Switching times are generally shorter for power MOSFETs than for power BJTs. Furthermore, at higher currents, drain current of a power MOSFET tends to decrease with temperature, which makes MOSFETs less likely than BJTs to experience thermal runaway.

Problem 10.18

$P_{Dmax} = I_{Cmax}V_{CE} = (T_{Jmax} - T_A)/\theta_{JA}$

$I_{Cmax} = (T_{Jmax} - T_A)/(\theta_{JA}V_{CE}) = (150 - 50)/(3 \times 25) = 1.33$ A

Problem 10.19

In a class-A amplifier, current flows through the transistors for the entire signal cycle (360°).

Problem 10.20

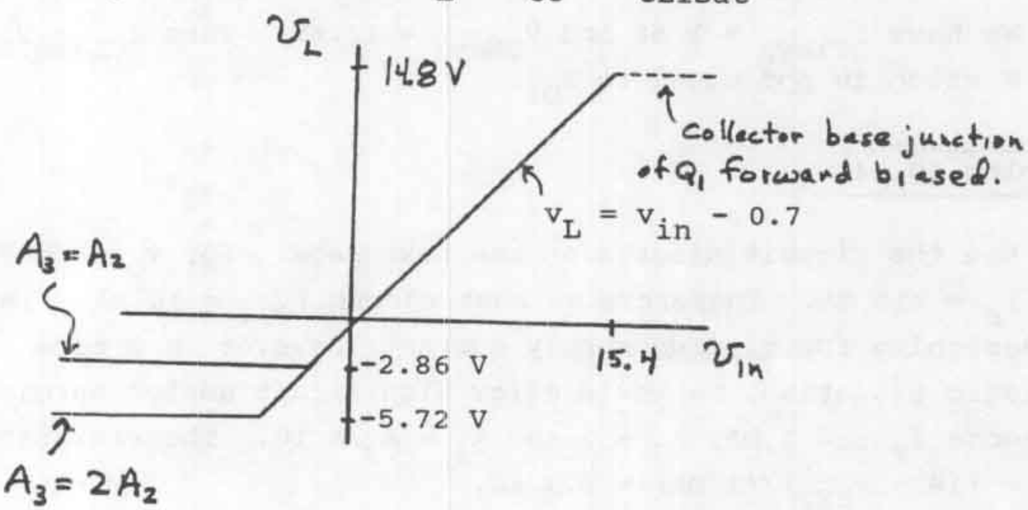
See Figure 10.11 on page 680 in the book.

Problem 10.21

If either the current or the voltage is constant with time, the average power is the product of the average current and the average voltage. If both the current and the voltage vary with time, the average power dissipation is not equal to the product of average current and average voltage in general.

Problem 10.22

$I_{CQ2} = (15 - 0.7)/(5\ k\Omega) = 2.86\ mA = I_{CQ3} = I_{CQ1}$.
For Q_1 at cutoff, $v_L = -2.86\ mA \times 1\ k\Omega = -2.86$ V.
For Q_1 in saturation, $v_L = V_{CC} - V_{CE1sat} = 14.8$ V.



When $A_3 = 2A_2$, $I_{CQ3} = 2 \times 2.86 = 5.72$ mA.

Problem 10.23

$$P_{Q1} = \frac{1}{T}\int_0^T v_{CE1}(t)\, i_{C1}(t)\, dt$$

$$P_{Q1} = \frac{1}{T}\int_0^T [12.65 - 12.65\sin(2000\pi t)][1.58\sin(2000\pi t) + 1.58]dt$$

$$P_{Q1} = \frac{1}{T}\int_0^T 20dt - \frac{1}{T}\int_0^T 20\sin^2(2000\pi t)\, dt$$

[We have made use of the fact that $\frac{1}{T}\int_0^T \sin(2000\pi t)\, dt = 0.$]

Using the trigonometric identity $2\sin^2(x) = 1 - \sin(2x)$, we have

$$P_{Q1} = \frac{1}{T}\int_0^T 20dt - \frac{1}{T}\int_0^T 10 - 10\sin(4000\pi t)\, dt$$

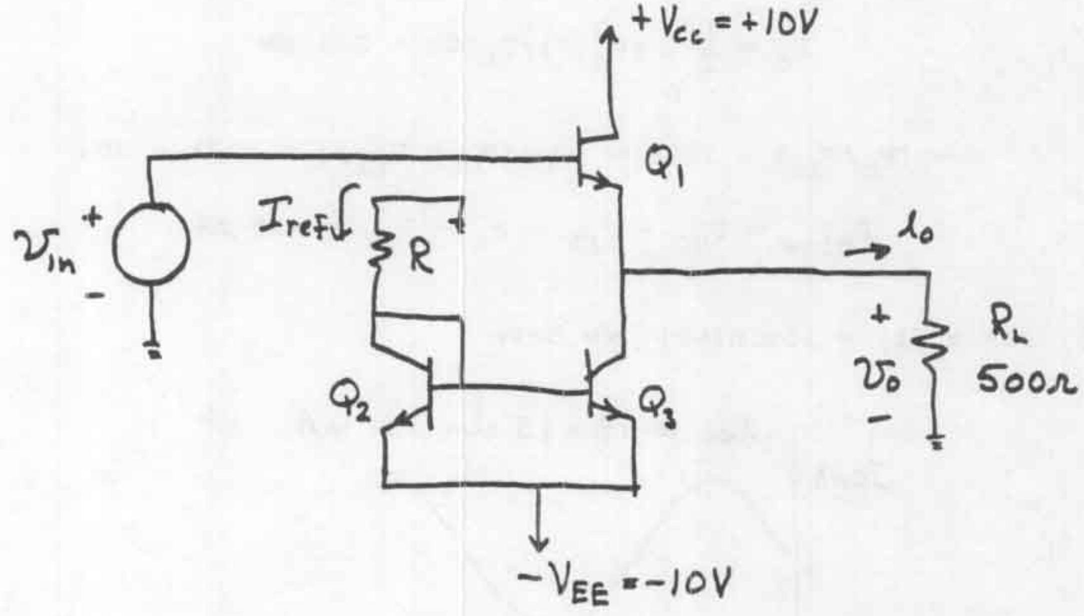
$$= 20 - 10$$

$$= 10 \text{ W}$$

We have $I_{C1avg} = 1.58$ and $V_{CEavg} = 12.65$. Thus $I_{C1avg}V_{CEavg}$ = 20 W which is not equal to P_{Q1}.

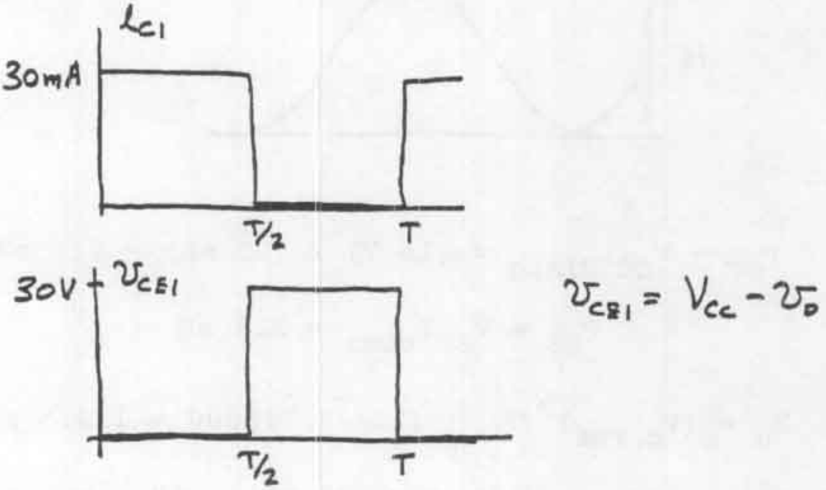
Problem 10.24

See the circuit diagram on the next page. For $v_o = \pm 5$ V we have $i_o = \pm 10$ mA. Therefore we must choose $I_{CQ3} = 10$ mA. (We are designing for minimum supply current, however in a more realistic situation, we would allow significant design margin.) We choose $I_{ref} = 1$ mA, $A_2 = 1$ and $A_1 = A_3 = 10$. The resistance is $R = (10 - V_{BE2})/(1 \text{ mA}) = 9.3$ kΩ.



Problem 10.25

(a)



$$P_{Q1} = \frac{1}{T}\int_0^T v_{CE1}(t)\, i_{C1}(t)\ dt = 0$$

$$P_{CC} = V_{CC} I_{C1avg} = (15\ \text{V}) \times (15\ \text{mA}) = 225\ \text{mW}$$

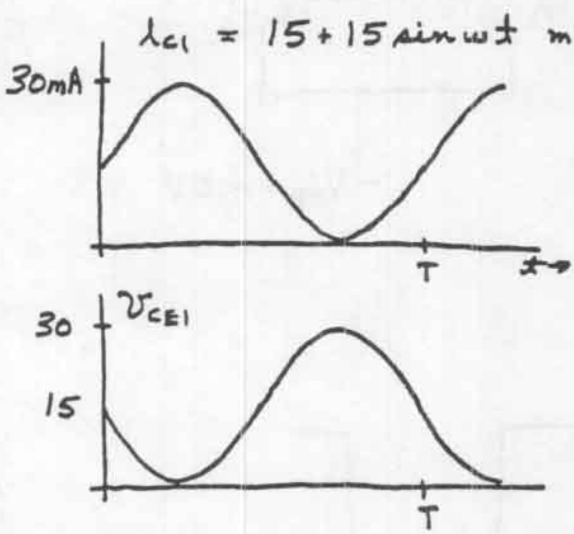
$$P_{EE} = V_{EE} I_{bias} = 225\ \text{mW}$$

$$P_o = \frac{1}{T}\int_0^T [v_o^2(t)/R_L]dt = 225 \text{ mW}$$

$$\eta = (P_o/P_{in}) \times 100\% = [P_o/(P_{CC} + P_{EE})] \times 100\% = 50\%$$

$$P_{bias} = P_{CC} + P_{EE} - P_o - P_{Q1} = 225 \text{ mW}$$

(b) For $v_o(t) = 15\sin(\omega t)$, we have



$$P_{CC} = V_{CC}I_{C1avg} = (15 \text{ V}) \times (15 \text{ mA}) = 225 \text{ mW}$$

$$P_{EE} = V_{EE}I_{bias} = 225 \text{ mW}$$

$$P_o = (V_{o,rms})^2/R_L = (15/\sqrt{2})^2/1000 = 112.5 \text{ mW}$$

$$P_{bias} = I_{bias}(V_{oavg} + V_{EE}) = (15 \text{ mA}) \times (0 + 15) = 225 \text{ mW}$$

$$P_{Q1} = P_{CC} + P_{EE} - P_{bias} - P_o = 112.5 \text{ mW}$$

$$\eta = [P_o/(P_{CC} + P_{EE})] \times 100\% = 25\%$$

Problem 10.26

(a) $$I_{CCavg} = \frac{1}{T}\int_0^T i_{CC}(t)\,dt$$

$$= \frac{1}{T}\int_0^T [4 + 2\sin(\omega t)]\,dt = 4\text{ A}$$

$$P_{CC} = V_{CC}I_{CCavg} = 60\text{ W}$$

(b) $$I_{CCavg} = \frac{1}{T}\int_0^{2T/3} 5\,dt + \frac{1}{T}\int_{2T/3}^{T} 2\,dt = 4\text{ A}$$

$$P_{CC} = V_{CC}I_{CCavg} = 60\text{ W}$$

(c) $I_{CCavg} = 0.5$ A $\quad P_{CC} = 7.5$ W

Problem 10.27

$$v(t) = V_{DC} + V_m\sin(\omega t)$$

$$i(t) = V_{DC}/R + (V_m/R)\sin(\omega t)$$

$$P_{avg} = \frac{1}{T}\int_0^T v(t)i(t)dt$$

$$= \frac{1}{T}\left[\int_0^T (V_{DC}^2/R)dt + (2V_mV_{DC}/R)\int_0^T \sin(\omega t)dt + V_m^2/R\int_0^T \sin^2(\omega t)dt\right]$$

$$= V_{DC}^2/R + 0 + V_m^2/2R\int_0^T [1 + \sin(2\omega t)]dt$$

$$= V_{DC}^2/R + V_m^2/2R$$

$$= P_{DC} + P_{AC}$$

Problem 10.28

(a) The peak load current is $\pm V_{CC}/R_L$ when one transistor is on the edge of saturation and the other is on the edge of cutoff. Thus the bias currents are $I_{CQ1} = I_{CQ2} = I_{o,peak} = V_{CC}/R_L$.

$$P_{in} = 2V_{CC}I_{CQ} = 2V_{CC}^2/R_L \qquad P_o = V_{o,rms}^2/R_L = V_{CC}^2/(2R_L)$$

$$\eta = (P_o/P_{in}) \times 100\% = 25\%$$

(b) For $P_o = 50 = V_{CC}^2/(2R_L)$ we have $V_{CC} = 28.3$ V and $I_{CQ} = I_{o,peak} = V_{CC}/R_L = 3.54$ A.

Problem 10.29

See Figure 10.22 on page 693 in the book.

Problem 10.30

See Figure 9.10 on page 565 in the book.

Problem 10.31

Two reasons that we don't rely entirely on negative feedback to eliminate crossover distortion are that it requires a very high loop gain to eliminate severe distortion. Very high loop gain requires added complexity and makes frequency compensation more difficult. Another reason is that if no bias is included in the class-B circuit, the output of the driver must slew very rapidly when one transistor turns off and the other turns on.

Problem 10.32

See Figure 10.21 on page 692 in the book.

Problem 10.33

For a sinusoidal signal the maximum efficiency of a class-A amplifier is 25%. For class-B amplifiers it is $(\pi/4) \times 100\% \cong 78.5\%$. (We are assuming that the saturation voltages of the transistors are negligible.)

Problem 10.34

The capacitor is included so the feedback ratio is unity for dc, which results in unity closed-loop gain for any dc offsets that may be present, thereby reducing the dc voltage applied to the load.

Problem 10.35

(a) Neglecting saturation voltages, the peak output voltage is equal to V_{CC}. Thus we have

$$P_o = 50 = (V_{CC}/\sqrt{2})R_L$$

$$V_{CC} = 28.3 \text{ V}$$

(b) The peak collector current equals the peak load current which is (28.3 V)/(8 Ω) = 3.54 A. The peak current rating of the transistors should be larger than this value.

(c) When the load voltage reaches its peak value V_{CC}, we have

$$|V_{CE2max}| = V_{CC} + V_{EE} = 56.6 \text{ V}$$

The peak V_{CE} ratings of the transistors should exceed this value.

(d) The peak power dissipated in the transistors (assuming a sinusoidal signal) is given by Equation 10.40 on page 696 in the book.

$$P_{DQ1max} = P_{DQ2max} = (2/\pi^2)P_{omax}$$

$$= (2/\pi^2)50$$

$$= 10.1 \text{ W}$$

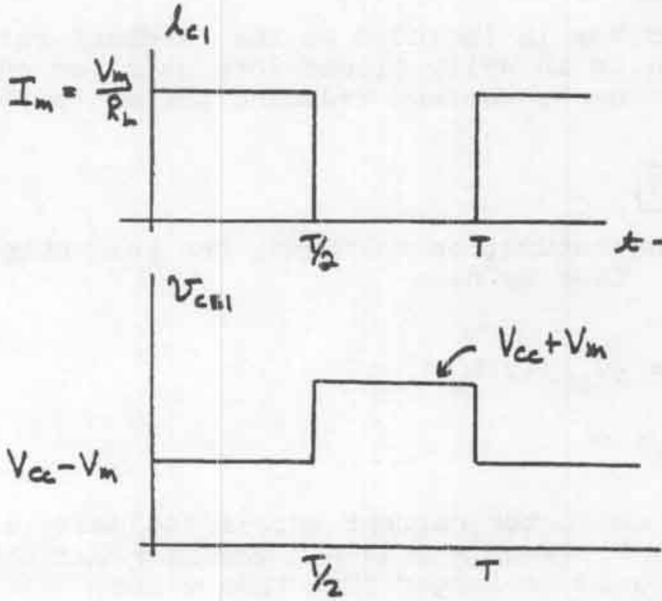
Thus the thermal design should accommodate at least 10.1 W without exceeding the maximum junction temperatures of the devices.

Problem 10.36

Following the approach of Problem 10.35 for $R_L = 50\ \Omega$, we find $V_{CC} = 70.7$ V, $I_{Cpeak} = 1.41$ A, $V_{CEmax} = 141$ V, and $P_{DQmax} = 10.1$ W.

Problem 10.37

(a)

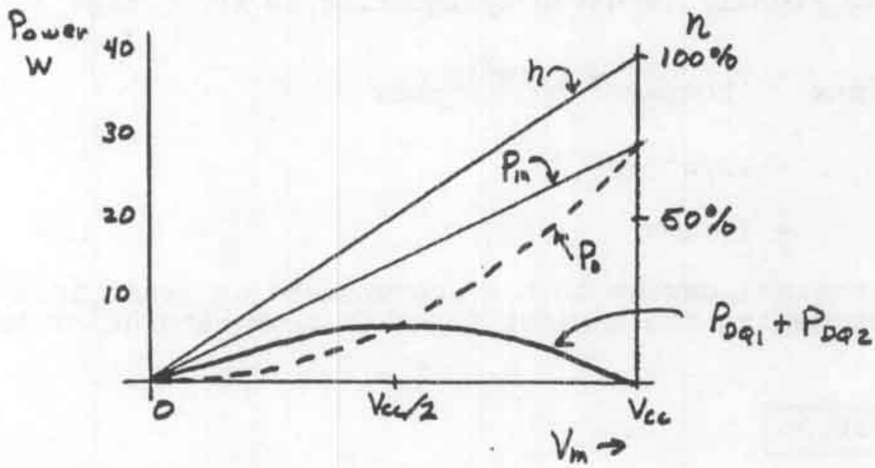


(b) $P_{in} = V_{CC}I_{C1avg} + V_{EE}I_{C2avg} = 2V_{CC}I_{C1avg} = V_{CC}V_m/R_L$

$P_o = V_m^2/R_L \quad P_{DQ1} = P_{DQ2} = (P_{in} - P_o)/2 = V_m(V_{CC} - V_m)/(2R_L)$

$\eta = (P_o/P_{in}) \times 100\% = (V_m/V_{CC}) \times 100\%$

(c)



The maximum efficiency is 100%.

(d) For a very low frequency, we should design the heat sink to accommodate the peak power dissipated rather than the average, because thermal conditions will reach steady state during the interval of peak power dissipation. The peak power dissipation for Q_1 occurs for $V_m = V_{CC}/2$.

$$P_{Q1max} = (V_{CC}/2) \times V_{CC}/(4R_L) = V_{CC}^2/(8R_L) = 3.51 \text{ W}$$

Problem 10.38

(a) If we neglect V_{CEsat}, at peak output signal, we have

$$V_{o,peak} = V_{CC} - V_{RE1} = 13.5 \text{ V}$$

$$I_{o,peak} = V_{o,peak}/R_L = 1.69 \text{ A}$$

$$R_{E1} = (1.5 \text{ V})/I_{o,peak} = 0.89\ \Omega$$

(b) $I_{B1,peak} = I_{C1,peak}/\beta_{min} = 33.8$ mA

$$I = 2I_{B1,peak} = 67.6 \text{ mA}$$

(c) $I_2 = I/4 = 16.9$ mA

$$R_2 = V_{BE3}/I_2 = (0.6 \text{ V})/(16.9 \text{ mA}) = 35.5\ \Omega$$

If we tried to make $I_2 = 2I$ then Q_3 will be in cutoff. If we make $I_2 = I/100$, then the base current of Q_3 will have a large effect and V_{CE3} will depend on β_3. Because β varies considerably from unit-to-unit, some of the circuits may be improperly biased.

(d) Neglecting I_{B3}, $R_1 = R_2 = 35.5\ \Omega$.

(e) Simulation file name: P10_38. The total harmonic distortion for various values of R_1 are shown in the table:

R_1 (Ω)	0	15	35.5	55
THD %	1.6	0.97	0.13	0.59

Problem 10.39

For the class-A circuit, the impedance seen looking into the primary of the transformer is 8 Ω for the ac signal and zero for dc. Thus $V_{CEQ3} = V_{CC}$.

(a) $I_{CQ3} = (15\ V)/(8\ \Omega) = 1.88\ A$ (minimum)

(b) $P_D = P_{in} = V_{CC}I_{CQ3} = 28.1\ W$ (Class A)

$P_D = P_{in} = 0$ (Class B)

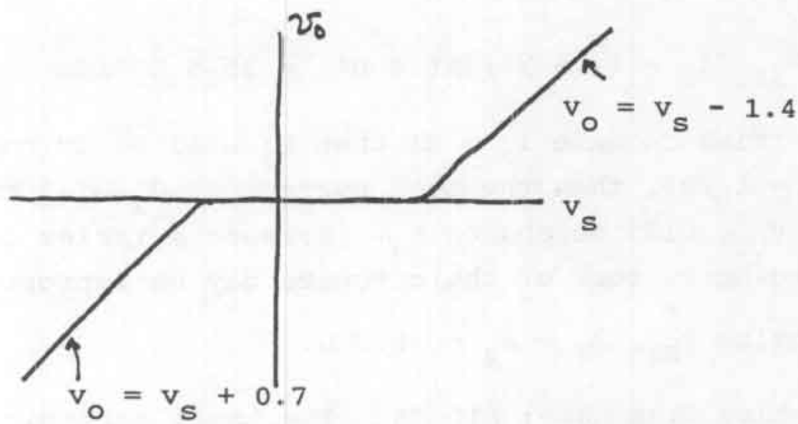
(c) $P_{omax} = (15/\sqrt{2})^2/R_L = 14.1\ W$ for either circuit.

(d) <u>Class</u> <u>A:</u> P_{in} is constant with output signal amplitude.
$\eta = (P_o/P_{in}) \times 100\% = (1.41/28.1) \times 100\% = 5\%$

<u>Class</u> <u>B:</u> For $P_o = 1.41\ W$ we have $V_m = 4.75\ V$.
$\eta = (V_m\pi)/(4V_{CC}) \times 100\ \%$ (This is Equation 10.39.)
$= 24.9\%$

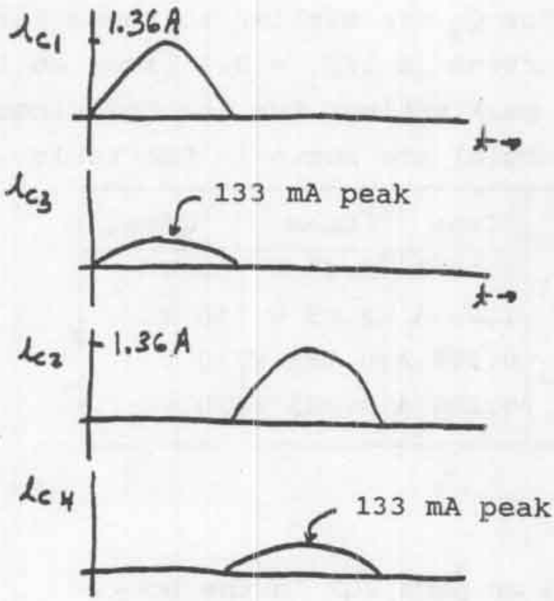
Problem 10.40

(a)



To eliminate most of the crossover distortion,we need to have $V_{b1} \cong 1.4$ and $V_{b2} \cong 0.7\ V$.

(b)



(c) The current and voltage waveforms for each transistor are similar to those of the class-B amplifier of Figure 10.22 on page 693. For example, Q_1 carries a half sine wave of current and its collector-to-emitter voltage is $v_{CE}(t) = V_{CC} - v_o$, exactly like Q_1 in Figure 10.22. The power dissipation for Q_1 is given by Equation 10.37 on page 695.

$$P_{DQ1} = \frac{V_{CC}V_m}{\pi R_L} - \frac{V_m^2}{4R_L}$$

We need to know the peak power dissipation to determine the specifications for Q_1. Thus we set the derivative with respect to V_m equal to zero and solve for V_m.

$$\frac{dP_{DQ1}}{dV_m} = 0 = \frac{V_{CC}}{\pi R_L} - \frac{2V_m}{4R_L} \quad \Rightarrow \quad V_m = 2V_{CC}/\pi$$

Substituting this into the expression for P_{DQ1} we have an expression for the maximum power dissipation.

$$P_{DQ1max} = V_{CC}^2/(\pi^2 R_L) = 2.85 \text{ W}$$

The peak collector-to-emitter voltage for Q_1 is approximately $2V_{CC}$. The peak collector current is approximately 15/8 = 1.88 A.

The conditions for Q_3 are similar to those for Q_1 except that its collector current is $1/\beta_1 = 0.1$ times as large.

The approximate peak ratings for the transistors (leaving very little design margin) are shown in the table:

	I_{Cmax}	P_{Dmax}	$\lvert V_{CEmax}\rvert$
Q_1	1.88 A	2.85 W	30 V
Q_2	1.88 A	2.85 W	30 V
Q_3	0.188 A	0.285 W	30 V
Q_4	0.188 A	0.285 W	30 V

Problem 10.41

See Figure 10.30 on page 702 in the book.

Problem 10.42

See Figure 10.31 on page 704 in the book.

Problem 10.43

The emitter and collector terminals of a series pass transistor are connected to the raw power supply and to the load. The load current is the collector/emitter current of the pass transistor. The 2N2222 transistor in Figure 10.32 on page 704 is an example of a series pass transistor. Some alternative configurations are shown in Figure 10.36 on page 708 in the book.

Problem 10.44

Dropout voltage is the minimum difference between input voltage and load voltage for a series regulator in normal operation. When the input voltage drops below the desired load voltage plus the dropout voltage, the load voltage dips.

Problem 10.45

The regulator is a negative feedback system that acts to drive v_i to zero. Thus we have $v_2 = V_{ref}$. In a good design the input current to the differential amplifier is negligible compared to the currents through R_1 and R_2. Thus we have

$$v_2 = \frac{v_L R_2}{R_1 + R_2} = V_{ref}$$

Substituting values and solving we find $R_1 = 20\ k\Omega$.

Problem 10.46

The load voltage is maintained at three times the reference voltage. Thus the load contains 15 mV of peak-to-peak ripple. As temperature increases, the load voltage increases by 24 mV/°C.

Problem 10.47

Equation 10.48 on page 703 gives the load voltage:

$$v_L = \frac{v_C}{A\beta + 1} + \frac{AV_{ref}}{A\beta + 1}$$

Thus the ripple component of the load voltage will be

$$V_{L,ripple} = \frac{V_{C,ripple}}{A\beta + 1}$$

We substitute $V_{L,ripple} = 10^{-3}$, $V_{C,ripple} = 2$ V and $\beta = 1/3$. Then solving, we obtain $A \cong 6000$.

Problem 10.48

For $V_L = 15$ V:

$P_{in} = V_{in}I_L = 20 \times 1 = 20$ W

$P_o = V_L I_L = 15$ W

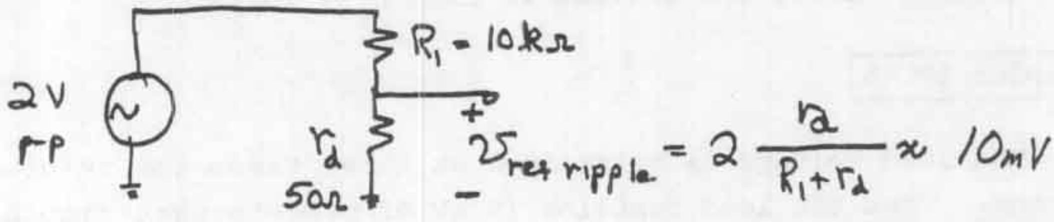
$\eta = (P_o/P_{in}) \times 100\% = 75\%$

For $V_L = 5$ V:

$P_{in} = 20$ W $P_o = 5$ W $\eta = 25\%$

Problem 10.49

(a) For D_1: $I_{DQ1} = (20 - 5)/10^4 = 1.5$ mA.
The small-signal equivalent circuit is:

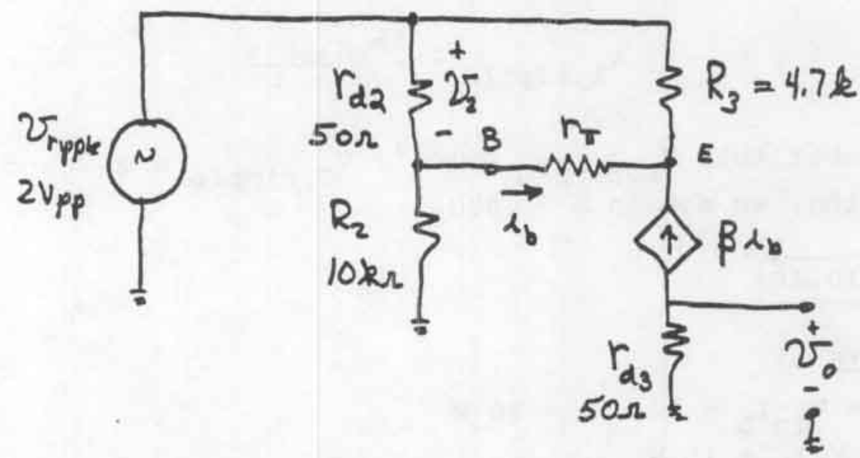


(b) For the transistor, $I_{EQ} = (5 - 0.7)/4700 = 0.915$ mA, $I_{BQ} = I_{EQ}/(\beta + 1) = 9.06\ \mu A$ and $I_{CQ} = 0.906$ mA. $r_\pi = \beta V_T/I_{CQ} \cong 2870\ \Omega$.

$$I_{DQ2} = 15/10^4 - I_{BQ} = 1.49 \text{ mA}$$

$$I_{DQ3} = I_{CQ} = 0.906 \text{ mA}$$

The small-signal equivalent circuit is:



We will see that the base current i_b is too small to significantly affect the value of v_2. Thus we have

$$v_2 \cong 2 \times \frac{r_{d2}}{R_2 + r_{d2}} = 10 \text{ mV}$$

$$v_2 + r_\pi i_b + R_3(\beta + 1) i_b = 0$$

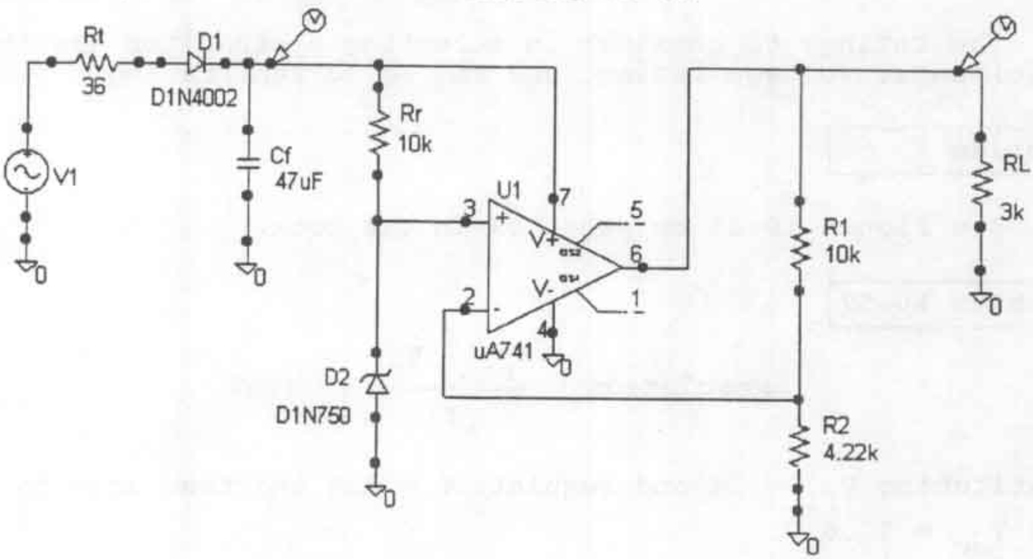
$$i_b = -\frac{v_2}{r_\pi + (\beta + 1)R_3} = -21 \text{ nA}$$

$$v_o = -\beta i_b r_{d3} = 0.105 \text{ mV peak-to-peak ripple}$$

Thus circuit (b) has much better ripple rejection.

Problem 10.50

The input connections to the op amp do not need to be reversed as suggested in the problem. We remove the op amp, reduce the value of C_F to take advantage of smaller size and cost, and change the value of R_2. The circuit diagram is shown below and the simulation is stored in the file named P10_50. As simulated, the output voltage is 15.4 V, however if R_2 is adjustable, we could achieve exactly 15 V.



Problem 10.51

The important functions of the transformer are to adjust the input voltage to the rectifier and to isolate the load from the ac power system.

Problem 10.52

Important transformer ratings are the regulation, voltage, and current ratings.

Problem 10.53

$$\text{Regulation} = \frac{V_{oc} - V_{fl}}{V_{fl}} \times 100\%$$

where V_{oc} is the open-circuit secondary voltage, and V_{fl} is the full load secondary voltage with a resistive load drawing rated current.

Problem 10.54

Important ratings to consider for the diodes in a rectifier are the peak-current and peak-inverse-voltage (PIV) ratings.

Problem 10.55

The ratings to consider in selecting a capacitor are its capacitance, voltage rating, and rms ac current rating.

Problem 10.56

See Figure 10.37 on page 709 in the book.

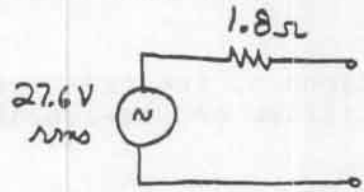
Problem 10.57

$$\text{Regulation} = \frac{V_{oc} - V_{fl}}{V_{fl}} \times 100\%$$

Substituting $V_{fl} = 24$ and regulation = 15% and then solving, we have $V_{oc} = 27.6$ V.

$$R_{th} = (V_{oc} - V_{fl}) = 1.8\ \Omega$$

The Thévenin equivalent circuit is:



Problem 10.58

The minimum input to the regulator must be $v_{in,min} = 16 + 2 = 18$ V. Let v_s = peak open-circuit secondary voltage at a line voltage of 105 V rms. Allowing 3 V for drop across the transformer resistance and design margin, we estimate

$$v_s = v_{in,min} + 2V_{diode} + 3 = 24 \text{ V}$$

Then at a line voltage of 120 V, the peak open-circuit secondary voltage is $24 \times (120/105) = 27.4$ V. Assuming a transformer with a 10% regulation rating, the rated secondary voltage (under load) is $v_{s,peak} = (27.4/1.1)/\sqrt{2} = 17.6$ V rms. Using the estimate for the rms secondary current given in Figure 10.37b on page 709 in the book, we have $I_{t,rms} \cong 1.8I_{Lavg} = 0.54$ A. We should allow some design margin so a secondary current rating of at least 0.75 A rms would seem prudent.

Problem 10.59

The minimum input to the regulator must be $v_{in,min} = 16 + 2 = 18$ V. Let v_s = peak open-circuit secondary voltage at a line voltage of 105 V rms. Allowing 3 V for drop across the transformer resistance and design margin, we estimate

$$v_s = v_{in,min} + V_{diode} + 3 = 22.5 \text{ V}$$

Then at a line voltage of 120 V, the peak open-circuit secondary voltage is $22.5 \times (120/105) = 25.7$ V. Assuming a transformer with a 10% regulation rating, the rated secondary voltage (under load) is $v_{s,peak} = (25.7/1.1)/\sqrt{2} = 16.5$ V rms (for each half of the secondary winding). Using the estimate for the rms secondary current given in Figure 10.37c on page 709 in the book, we have $I_{t,rms} \cong 1.2I_{Lavg} = 0.36$ A. We should allow some design margin so a secondary current rating of at least 0.5 A rms would seem prudent.

Problem 10.60

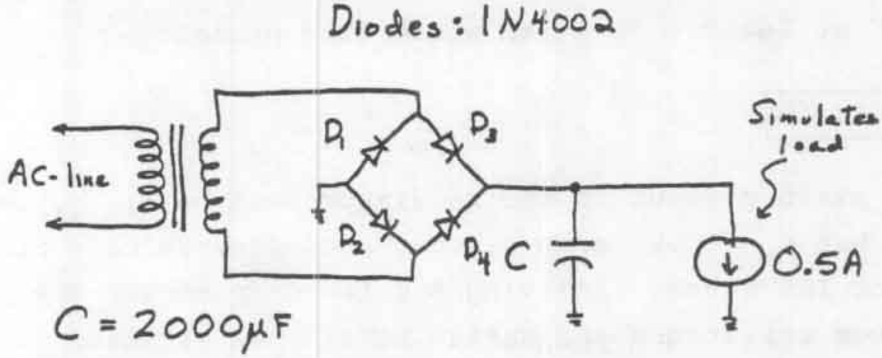
The simulations are stored in the files named P10_60a and P10_60b. To find the rms value of the current, we request Probe to plot rms(i(d1)) and use the cursor to determine the steady-state value. The results for the two circuits are:

	I_{surge}	I_{rms}
(a)	3.5 A	0.65 A
(b)	130 A	0.94 A

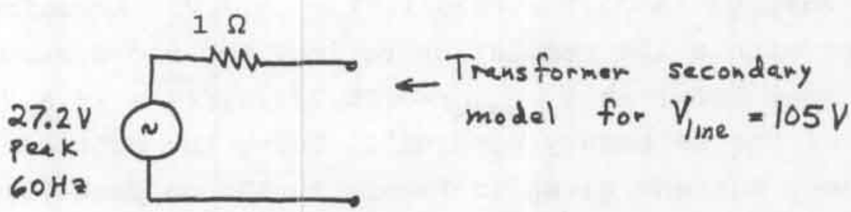
The point of the problem is that the formulas given for the rms currents in Figure 10.37 on page 709 are rule-of-thumb estimates for component values typically found in power-supply rectifiers.

Problem 10.61

There are many ways to satisfy the requirements of this problem. One possibility:



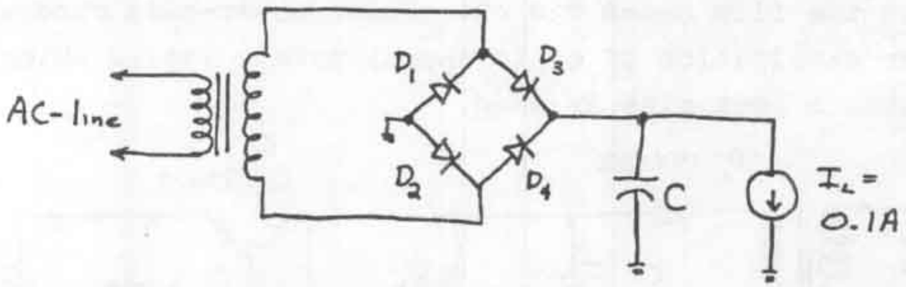
The transformer secondary ratings are 20 V rms at V_{line} = 120 V rms and full load, 2 A rms, 10% regulation. The model for the transformer is:



The simulation is stored in the file named P10_61. The secondary current is approximately 1.8 A rms and the capacitor current is approximately 1.64 A rms. The capacitor should be rated for a voltage of at least $20 \times \sqrt{2} \times (130/120) = 30.6$ V.

Problem 10.62

There are many ways to satisfy the requirements of this problem. One possibility is shown on the next page. We estimate the capacitance required using Equation 3.6 from the book. $C = I_L T/2V_r = 0.1(1/60)/(2 \times 10) = 83.3\ \mu F$. Thus we pick $C = 100\ \mu F$ which is a standard value.

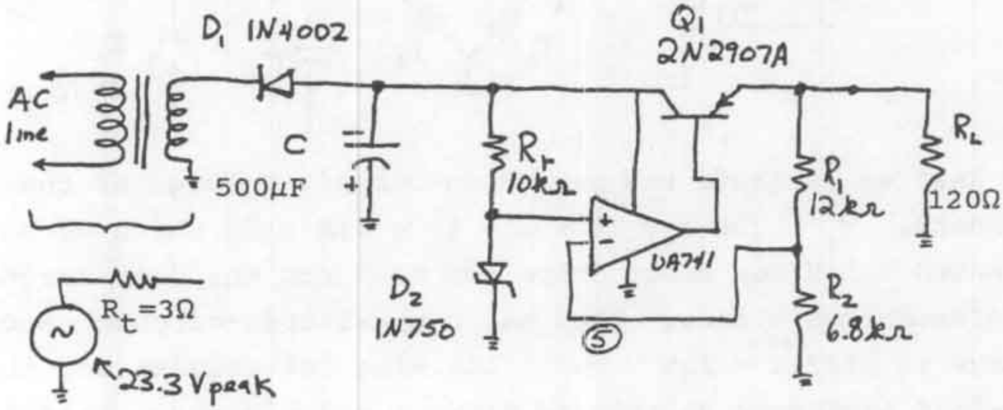


Next we estimate the peak open-circuit voltage of the secondary. $V_s = 300 + V_r/2 + 3 + 10 = 318$ V in which we have estimated 1.5 V for diode drops and 10 V for the drop across the transformer resistance. Thus the nominal open-circuit secondary voltage is $318/\sqrt{2} = 225$ V rms. Assuming 10% regulation, the full-load secondary voltage is $225/1.1 = 205$ V rms. Therefore we choose a 205 V rms rating for the secondary. Using the equation from Figure 10.37b we estimate the secondary current as $1.8I_L = 0.18$ A. However for higher voltage rectifiers the current flows in very brief pulses and the estimate is too low. Thus we (eventually after several rounds of trial and error) choose a transformer with a current rating of 1.0 A rms. The Thévenin equivalent for the transformer is a 319-V peak sine wave source in series with 20.5 Ω.

The simulation is stored in the file named P10_62. The secondary current is approximately 0.9 A rms and the capacitor current is approximately 0.9 A rms. The peak voltage across the capacitor with high line and no load could be as high as 205 × 1.1 × $\sqrt{2}$ × (130/120) = 345 V. The diodes should be rated for a voltage of at least 2 × 205 × 1.1 × $\sqrt{2}$ × (130/120) = 690 V. To be on the safe side we selected the 1N4007 which has a PIV of 1000 V.

Problem 10.63

There are many ways to solve this problem. The circuit diagram for one solution is shown on the next page. The transformer is rated for 15 V rms and 0.5 A. The simulation is stored in the file named P10_63. Under worst-case conditions, the power dissipation of Q_1 is approximately 700 mW which is too high unless a heat sink is used.



Problem 10.64

(a) θ_{JC} = (150 - 75)/20 = 3.75°C/W

(b) T_{Jmax} is the temperature for zero power dissipation which is 150°C.

Problem 10.65

(a) The power dissipation in the regulator is approximately the load current times the difference between the input and output voltages. This is P_D = (12 - 5) × 0.5 = 3.5 W.

(b) $\theta_{JAmax} = (T_{Jmax} - T_A)/P_D$ = 125/3.5 = 35.7°C/W

(c) $\theta_{SA} = \theta_{JAmax} - \theta_{JC} - \theta_{CS}$ = 32.7°C/W

Chapter 11

Exercise 11.1

$$|H(f)| = \frac{H_0}{\sqrt{1 + (f/f_b)^{2n}}}$$

For $f >> f_b$ this becomes

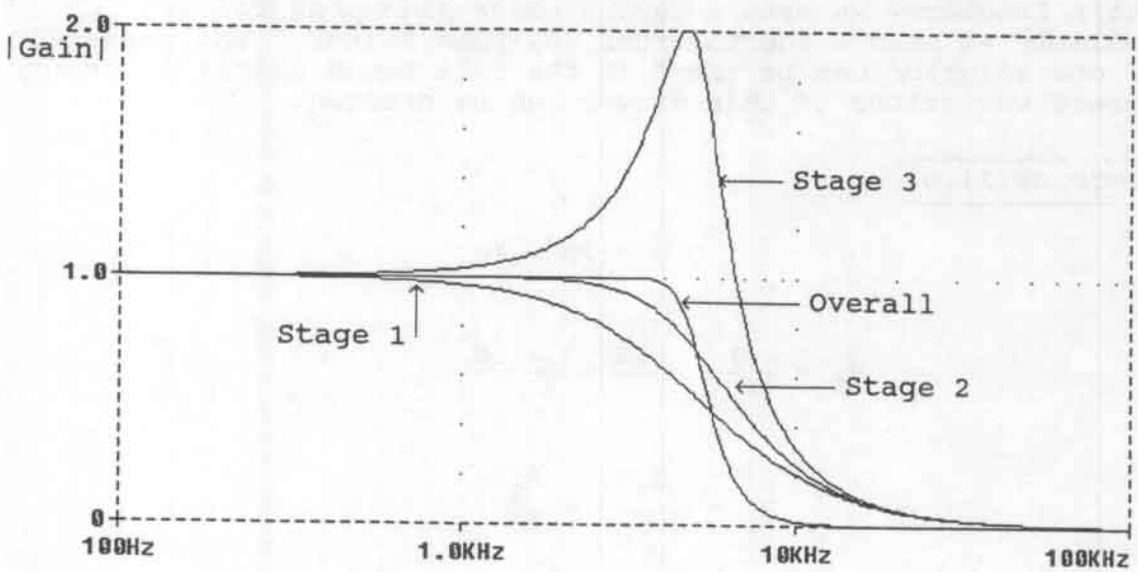
$$|H(f)| \cong H_0(f_b/f)$$

$$|H(f)|_{dB} \cong 20\log H_0 + 20\log(f_b) - 20\log(f)$$

The last term on the right-hand side of this expression shows that the gain magnitude declines at 20 dB/decade.

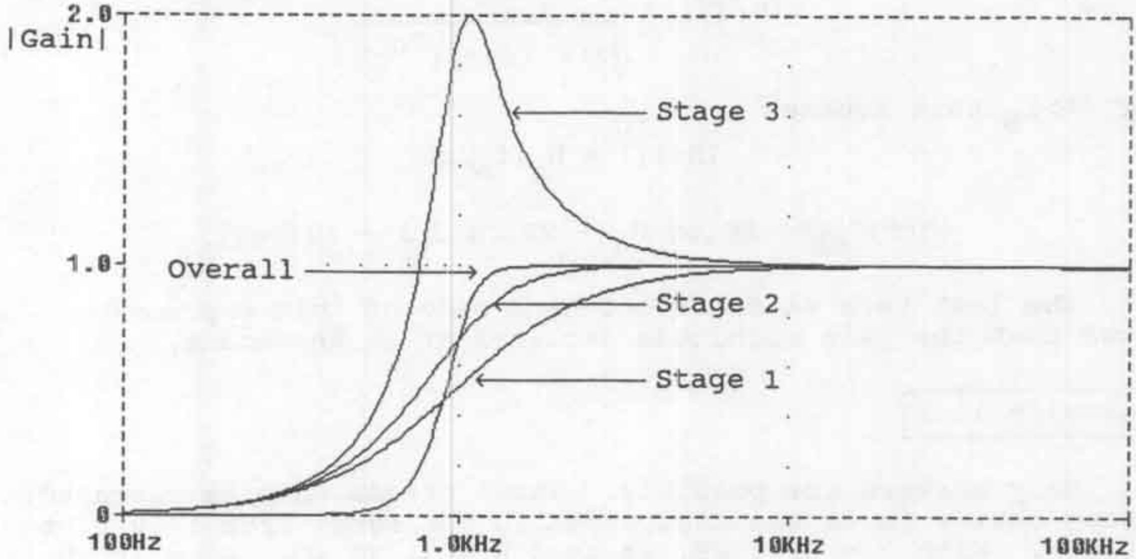
Exercise 11.2

Many answers are possible. Three stages must be cascaded. A good choice is to use capacitors in the range from 1000 pF to 0.01 μF. With C = 0.01 μF, we need R = 3.183 kΩ. R_f = 10 kΩ is a good choice. From Table 11.1 we find the gain values to be 1.068, 1.586, and 2.483. The simulation is stored in the file named Exer11_2. Plots of the gains normalized to their dc values are shown below:



Exercise 11.3

Many answers are possible. Three stages must be cascaded. $R = 15.92\ k\Omega$ and $R_f = 10\ k\Omega$ are good choices. From Table 11.1, we find the gain values to be 1.068, 1.586, and 2.483. The simulation is stored in the file named Exer11_3. Plots of the normalized gains are:



Exercise 11.4

To achieve 30 dB of attenuation one decade below the lower cutoff frequency we need a second-order high-pass filter. Similarly we need a fourth-order low-pass filter. The schematic for one solution can be found in the file named Exer11_4. Many correct variations of this answer can be created.

Exercise 11.5

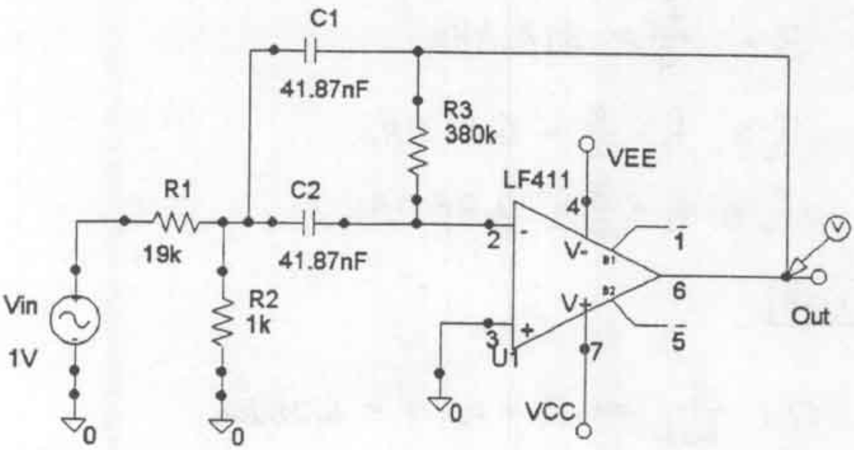
$$Q = f_0/B = 10$$

$$R_3 = \frac{Q}{\pi f_0 C} = \frac{15.92 \times 10^{-3}}{C}$$

$$R_1 = \frac{R_3}{2\ H_0} = \frac{R_3}{20}$$

$$R_2 = \frac{R_3}{4Q^2 - 2H_0} = \frac{R_3}{380}$$

We select R_3 sufficiently high so that R_2 is not too low. For example we choose R_3 = 380 kΩ and then R_2 = 1 kΩ, R_1 = 19 kΩ and C = 41.87 nF. The simulation is stored in the file named Exer11_5. The circuit diagram is:



Exercise 11.6

$$Q = \frac{\omega_0 L}{R} \quad \Rightarrow \quad L = \frac{QR}{\omega_0} = \frac{10(100)}{2\pi 10^7} = 15.92\ \mu H$$

$$Q = \frac{1}{\omega_0 CR} \quad \Rightarrow \quad C = \frac{1}{\omega_0 QR} = \frac{1}{2\pi 10^7 (10) 100} = 15.92\ pF$$

$$I = \frac{1\angle 0^\circ}{R + j\omega L - j/(\omega C)} = 10\angle 0^\circ \text{ mA}$$

$$\mathbf{V}_R = RI = 1\angle 0^\circ \qquad \mathbf{V}_L = j\omega_0 LI = j1000 \times 0.01 = 10\angle 90^\circ$$

$$\mathbf{V}_C = I/(j\omega_0 C) = 10\angle -90^\circ$$

See Figure 11.24 on page 750 for the phasor diagram.

Exercise 11.7

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{5\times10^{-6}\times100\times10^{-12}}} = 7.12\,MHz$$

$$Q = \frac{\omega_0 L}{R} = 22.4$$

$$B = \frac{f_0}{Q} = 318\ kHz$$

$$f_L \approx f_0 - \frac{B}{2} = 6.96\,MHz$$

$$f_H \approx f_0 + \frac{B}{2} = 7.28\,MHz$$

Exercise 11.8

$$Q = \frac{R}{\omega_0 L} \Rightarrow R = \omega_0 L Q = 6.28\,k\Omega$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \Rightarrow C = \frac{1}{\omega_0^2 L} = 25.33\,pF$$

$$B = \frac{f_0}{Q} = 1\,MHz$$

$$f_L \approx f_0 - B/2 = 99.5\,MHz$$

$$f_H \approx f_0 + \frac{B}{2} = 100.5\,MHz$$

Exercise 11.9

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = 876\ kHz$$

$$Q = \frac{R}{\omega_0 L} = 54.5 \qquad B = \frac{f_0}{Q} = 16.1\,kHz$$

$$f_L \approx f_0 - \frac{B}{2} = 868\,kHz$$

$$f_H \approx f_0 + \frac{B}{2} = 884\,kHz$$

Exercise 11.10

(a) $Q_s = \frac{\omega L}{R_s} = 188.5$

Because $Q_s >> 1$ $\quad L_p = L_s = L = 1\mu H$

$R_p = Q^2 R_s = 35.5 k\Omega$

(b) $Q_s = \frac{\omega L}{R_s} = 125.6$

$L_p = L_s = 1\mu H$

$R_p = Q^2 R_s = 15.8 k\Omega$

Exercise 11.11

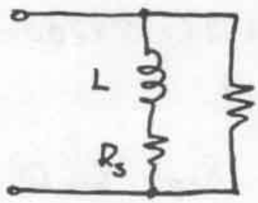
$$Q = \frac{R_P}{1/\omega C} = \omega C R_P = 2\pi 10^7 \, 100\times10^{-12} \times 10^4$$

$Q = 62.8$ $\quad$ Because $Q >> 1$

$C_s = C_p = C = 100pF$

$R_s = \frac{R_P}{Q^2} = 2.53\Omega$

Exercise 11.12



$L = 1mH$

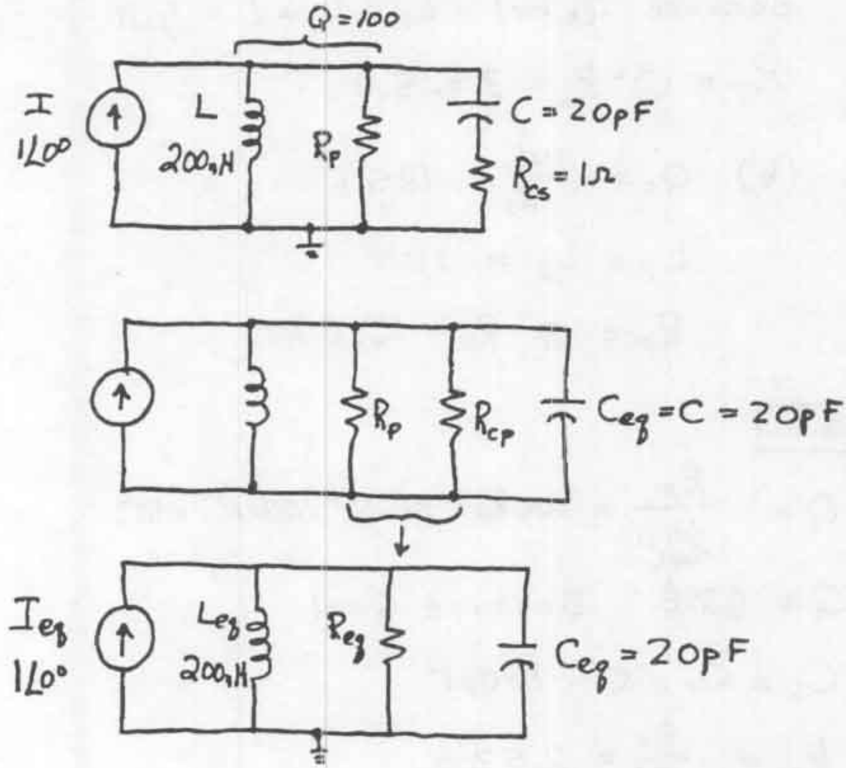
$Q_{max} = 75$ @ $200 kHz$

$$\frac{\omega L}{R_s} = 2Q_{max} \Rightarrow R_s = \frac{\omega L}{2Q_{max}} = 8.38\Omega$$

$$\frac{R_P}{\omega L} = 2Q_{max} \Rightarrow R_P = \omega L \, 2Q_{max} = 188.5k\Omega$$

Exercise 11.13

Assume that high-Q approximations apply.



$$f_o = \frac{1}{2\pi\sqrt{L_{eq} C_{eq}}} = 79.6\ MHz$$

$$R_P = Q\,\omega_o L = 100 \times 2\pi \times 79.6 \times 10^6 \times 200 \times 10^{-9}$$
$$= 10\ k\Omega$$

$$Q_c = \frac{1/\omega_o C}{R_{cs}} = 100 \qquad R_{cp} = R_{cs}\, Q_c^2 = 10 k\Omega$$

$$R_{eq} = R_p \,\|\, R_{cp} = 5 k\Omega$$

Both the original circuit and the simplified equivalent are simulated in file Exer11_13. The voltages across the circuits are virtually identical.

Exercise 11.14

Follow Example 11.8 except with f_0 = 5 MHz and P_o = 10 W.

$$Q_{loaded} = 20$$

$$P_{in} = \frac{10}{0.90} = 11.11$$

$$P_{in} = \left(\frac{2\, V_{CC}}{\pi \sqrt{2}}\right)^2 \frac{1}{R_{Ls} + R_{2s}}$$

$$R_{Ls} + R_{2s} = 2.627\,\Omega$$

$$L = \frac{Q_{loaded}\,(R_{Ls} + R_{2s})}{\omega_0} = 1.672\,\mu H$$

$$R_{Ls} = \frac{\omega_0 L}{Q_{unloaded}} = 0.2627\,\Omega$$

$$R_{2s} = 2.364\,\Omega$$

$$R_L = Q_{C2}^2 R_{2s} \Rightarrow Q_{C2} = 4.599$$

$$X_{C2} = Q_{C2} R_{2s} = 10.87\,\Omega$$

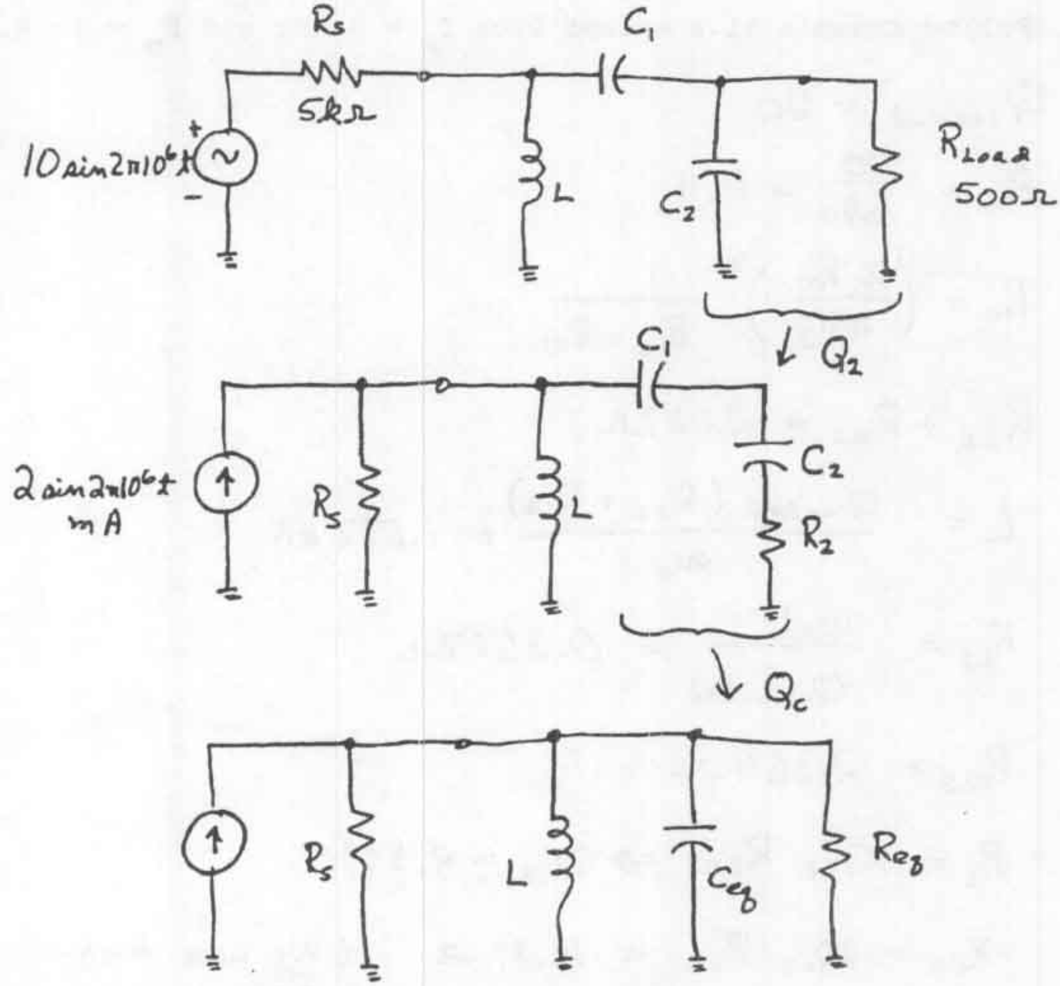
$$X_{C1} = \omega_0 L - X_{C2} = 41.66\,\Omega$$

$$C_1 = \frac{1}{\omega_0 X_{C1}} = 764.1\,pF$$

$$C_2 = \frac{1}{\omega_0 X_{C2}} = 2928\,pF$$

(We use high-Q approximation. In practice one or more components must be adjustable.)

Exercise 11.15



For max power transfer (at the resonant frequency) $R_{eq} = R_s$

$$R = R_{eq} \| R_s = 2500\,\Omega$$

$$Q = \frac{f_o}{B} = \frac{1\,\text{MHz}}{50\,\text{kHz}} = 20$$

$$Q = \frac{R}{\omega_o L} \Rightarrow L = \frac{R}{\omega_o Q} = \frac{2500}{2\pi 10^6 (20)} = 19.89\,\mu\text{H}$$

$$Q = \omega_o C_{eq} R \Rightarrow C_{eq} = \frac{Q}{\omega_o R} = 1273\,pF$$

$$Q_c = \omega_o C_{eq} R_{eq} = 40$$ (This is the Q of the C_{eq} R_{eq} combination.)

$$R_2 = \frac{R_{eq}}{Q_c^2} = \frac{5000}{40^2} = 3.125\,\Omega$$

$$R_{Load} = Q_2^2 R_2 \Rightarrow Q_2 = \sqrt{\frac{R_{Load}}{R_2}} = \sqrt{\frac{500}{3.125}} = 12.65$$

$$Q_2 = \omega_o C_2 R_{Load} \Rightarrow C_2 = \frac{Q_2}{\omega_o R_{Load}} = 4026\,pF$$

$$C_{eq} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2}} \Rightarrow C_1 = 1862\,pF$$

Exercise 11.16

$$Q = \frac{f_o}{B} = 50 \quad C = \frac{1}{L\omega_o^2} = 50.7\,pF$$

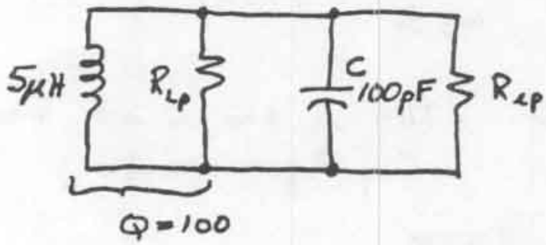
$$R_p = Q_{coil}\,\omega_o L = 200(2\pi\, 10^7)\,5\times 10^{-6} = 62.8\,k\Omega$$

$$R = Q\,\omega_o L = 15.7\,k\Omega$$

$$R = R_L || R_p || r_d \Rightarrow R_L = \frac{1}{\frac{1}{R} - \frac{1}{R_p} - \frac{1}{r_d}} = -1.857\,M\Omega$$

Negative R_L is not possible. Thus $L = 5\mu H$ is not a good choice.

Exercise 11.17



$$\omega_0 = \frac{1}{\sqrt{LC}} = 4.47 \times 10^7$$

$$R_{Lp} = Q\,\omega_0 L = 22.36\ k\Omega$$

$$R_{eq} = R_{Lp} \| R_{ip}$$

If $R_{eq} > 0$ the transient dies out. On the other hand if $R_{eq} < 0$ the transient grows.

$$R_{eq} = \frac{1}{\frac{1}{R_{Lp}} + \frac{1}{R_{ip}}}$$

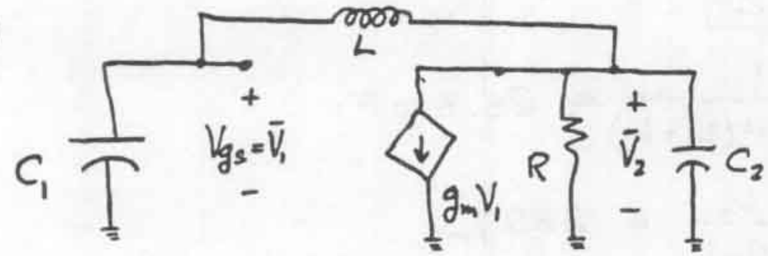
Thus if $0 > R_{ip} > -22.36k\Omega$ the transient grows.

If $R_{ip} > 0$ or $R_{ip} < -22.36k\Omega$ the transient dies.

Exercise 11.18

(a) R_G provides a path for the gate leakage current.

(b)



(c) Write node voltage equations:

$$j\omega C_1 V_1 + \frac{1}{j\omega L}(V_1 - V_2) = 0$$

$$g_m V_1 + \frac{V_2}{R} + j\omega C_2 V_2 + \frac{1}{j\omega L}(V_2 - V_1) = 0$$

Group terms:

$$\left(j\omega C_1 - j\frac{1}{\omega L}\right)V_1 + \left(j\frac{1}{\omega L}\right)V_2 = 0$$

$$\left(g_m + j\frac{1}{\omega L}\right)V_1 + \left(\frac{1}{R} + j\omega C_2 - j\frac{1}{\omega L}\right)V_2 = 0$$

Set system determinant to zero:

$$-\omega^2 C_1 C_2 + \frac{C_2}{L} + \frac{C_1}{L} - \frac{1}{\omega^2 L^2} + j\frac{\omega C_1}{R} - j\frac{1}{R\omega L}$$

$$+ j\frac{g_m}{\omega L} + \frac{1}{\omega^2 L^2} = 0$$

Reals: $\quad -\omega^2 C_1 C_2 + \frac{C_2}{L} + \frac{C_1}{L} = 0 \Rightarrow \omega = \dfrac{1}{\sqrt{L\frac{C_1 C_2}{C_1 + C_2}}}$

Imag: $\quad \frac{\omega C_1}{R} - \frac{1}{R\omega L} + \frac{g_m}{\omega L} = 0 \Rightarrow g_m = C_1/(C_2 R)$

Exercise 11.19

$$C = \frac{1}{\omega^2(L_1+L_2)} = 25.3\,pF$$

$$R = \frac{L_2}{g_m L_1} = 285.7\,\Omega$$

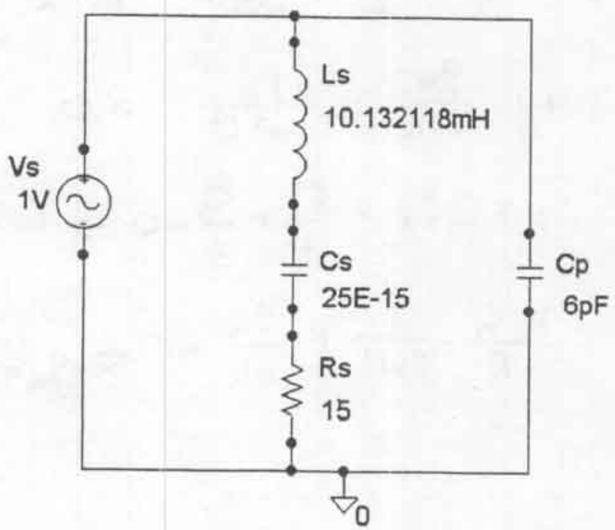
$$\frac{n_2}{n_3} = \sqrt{\frac{R}{R_L}} = 2.450$$

$$L_3 = L_2\left(\frac{n_3}{n_2}\right)^2 = 0.833\,\mu H$$

We expect that oscillator circuits in which the device capacitances are a smaller fraction of C will have better frequency stability.

Exercise 11.20

The simulation of the circuit shown below is stored in the file named Exer11_20. After running the simulation, use Probe to plot 1/II(Vs). Then adjust the scales to obtain the plot shown in Figure 11.59 on page 790 in the book.



Problem 11.1

An active filter is composed of op amps, resistors and capacitors. Ideally an active filter should:

1. Contain few components.

2. Have a transfer function that is insensitive to component tolerances.

3. Place modest demands on the op amp's gain-bandwidth product, output impedance, slew rate, and other specifications.

4. Be easily adjusted.

5. Require a small spread of component values.

6. Allow a wide range of useful transfer functions to be realized.

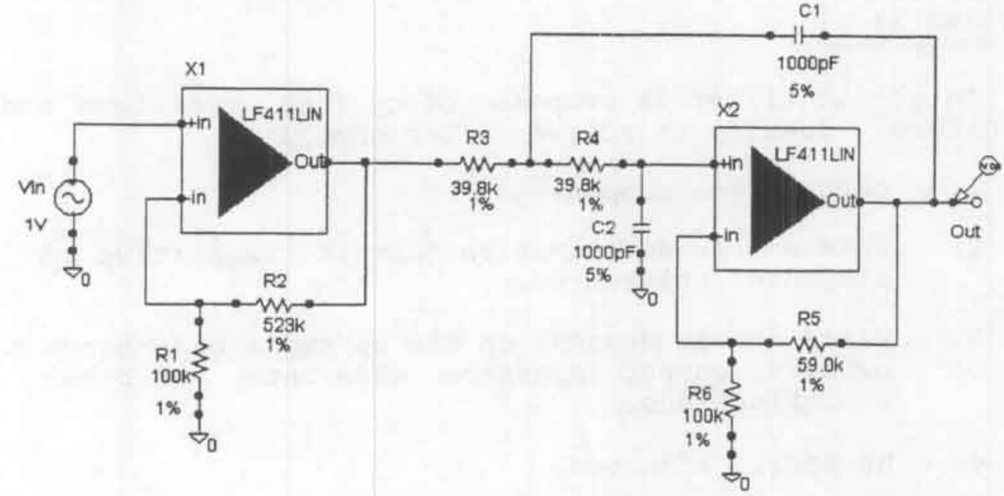
Problem 11.2

$$|H(f)| = \frac{H_0}{\sqrt{1 + (f/f_b)^{2n}}}$$

Problem 11.3

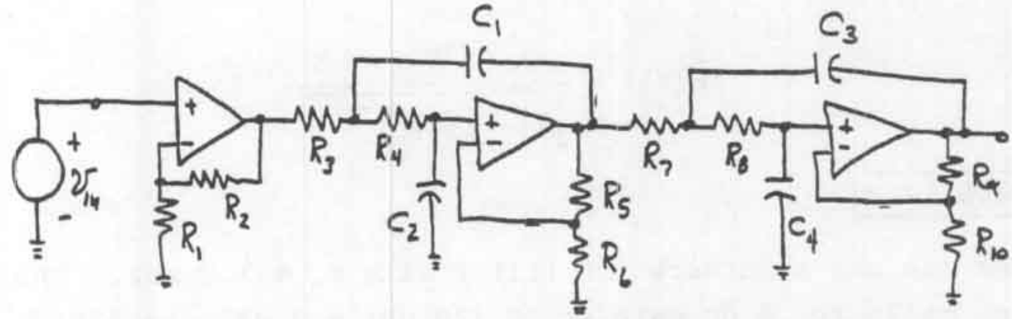
We can use a Butterworth filter with $f_b \cong 3.5$ kHz. The problem calls for a dc gain of 10 (20 dB) and gain magnitude less than 0.5 (-6 dB) at 35 kHz. Thus we need at least 26 dB/decade rolloff. A second-order filter will provide 40 dB/decade. To achieve high input impedance and the desired dc gain, we use a noninverting amplifier as the first stage. The circuit diagram is shown on the next page.

In the circuit, four resistors (R_1, R_2, R_5 and R_6) affect the dc gain. By specifying 1%-tolerance resistors we can ensure that the dc gain tolerance is within the desired 5%. We have designed for a nominal 3-dB frequency of 4 kHz to ensure that the 3-dB bandwidth is greater than 3.5 kHz. A Monte Carlo simulation is stored in the file named P11_3. For 20 runs all of the circuits meet the desired specifications.



Problem 11.4

This is similar to Problem 11.3 except that a higher order filter is needed. One solution is:



$$C_1 = C_2 = C_3 = C_4 = 1000\ pF \pm 5\%$$

$$R_3 = R_4 = R_7 = R_8 = 40.2\ k\Omega \pm 1\%$$

$$R_6 = R_{10} = 100 k\Omega \pm 1\% \qquad R_5 = 15.0 k\Omega \pm 1\%$$

$$R_9 = 124k \pm 1\%$$

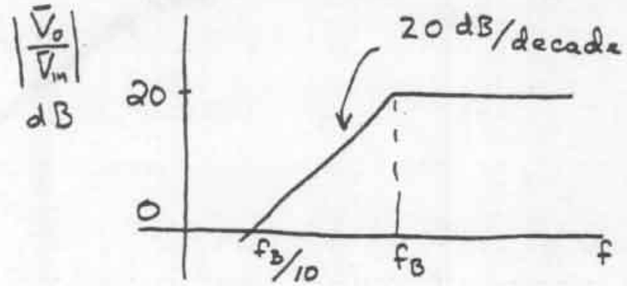
$$R_1 = 100 k\Omega \quad R_2 = 287 k\Omega \pm 1\%$$

A Monte Carlo simulation stored in file P11_4 shows that the circuit meets all of the desired specifications.

Problem 11.5

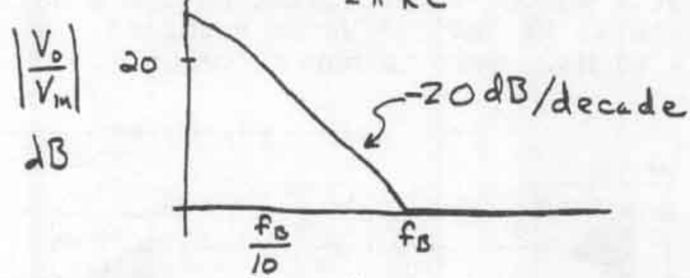
(a) $\frac{\bar{V}_o}{\bar{V}_{in}} = -\frac{10R}{R + \frac{1}{j\omega C}} = \frac{-10}{1 - j\ \frac{f_B}{f}}$

where $f_B = \frac{1}{2\pi RC}$



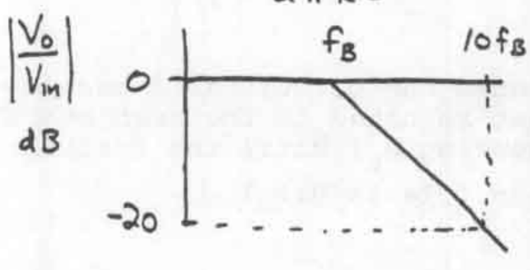
(b) $\frac{\bar{V}_o}{\bar{V}_{in}} = -\frac{R + \frac{1}{j\omega C}}{R} = -\left(1 - j\ \frac{f_B}{f}\right)$

where $f_B = \frac{1}{2\pi RC}$



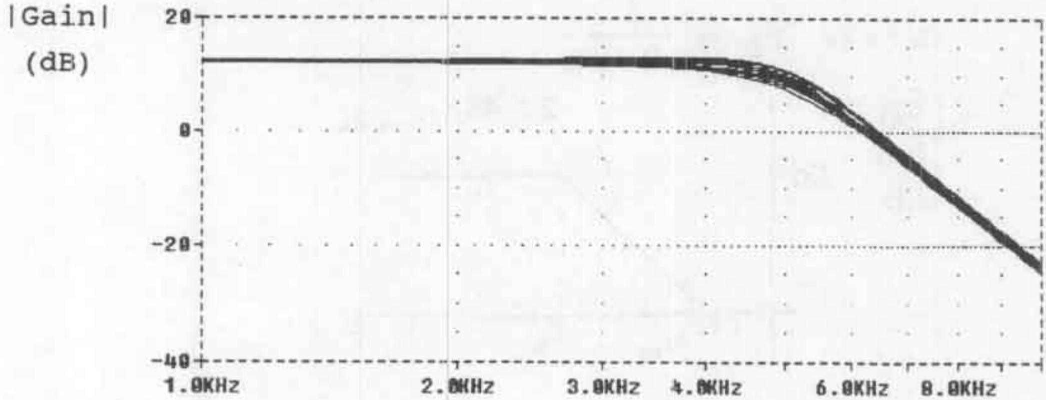
(c) $\left|\frac{\bar{V}_o}{\bar{V}_{in}}\right| = -\frac{\frac{1}{1/R + j\omega C}}{R} = -\frac{1}{1 + j\ f/f_B}$

where $f_B = \frac{1}{2\pi RC}$



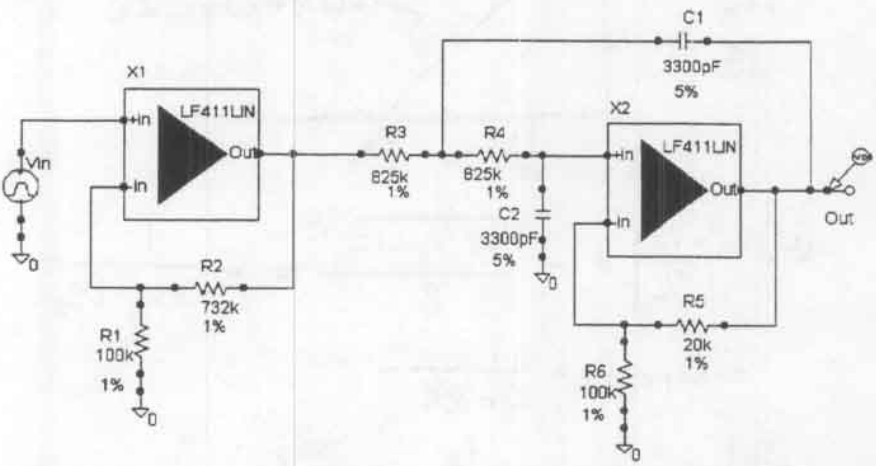
Problem 11.6

The simulation is stored in file P11_6. The gain magnitude versus frequency for 20 runs is:



Problem 11.7

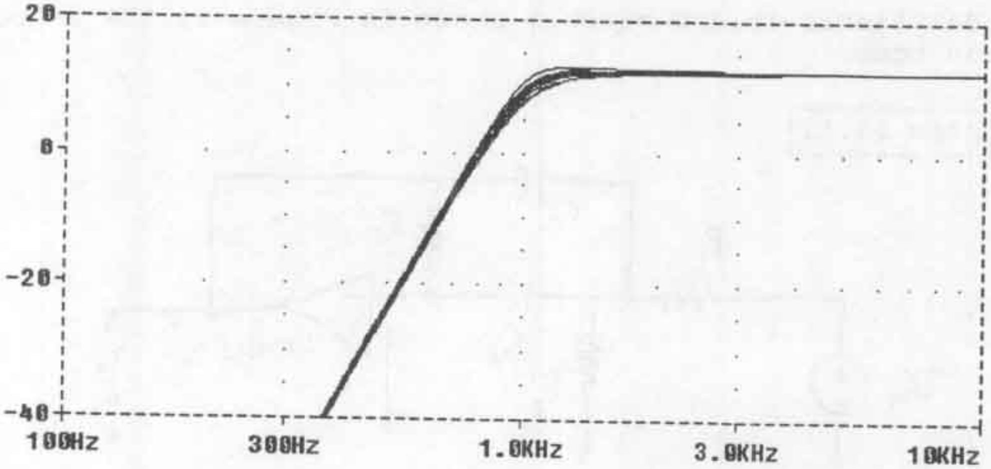
Using Equation 1.19 on page 47 we have $f_b \cong 0.35/t_r = 35$ Hz. Because the gain must roll off by 40 dB between f_b and 1000 Hz, we conclude that a second-order filter having a half-power bandwidth between 35 Hz and 100 Hz is required. We decided to design for $f_b \cong 60$ Hz. Here is our circuit:



Initially, we designed the circuit as a second-order Salen-Key stage. However, that resulted in too much overshoot. We reduced the gain (by reducing R_5) until the desired overshoot was obtained. The simulation file is P11_7.

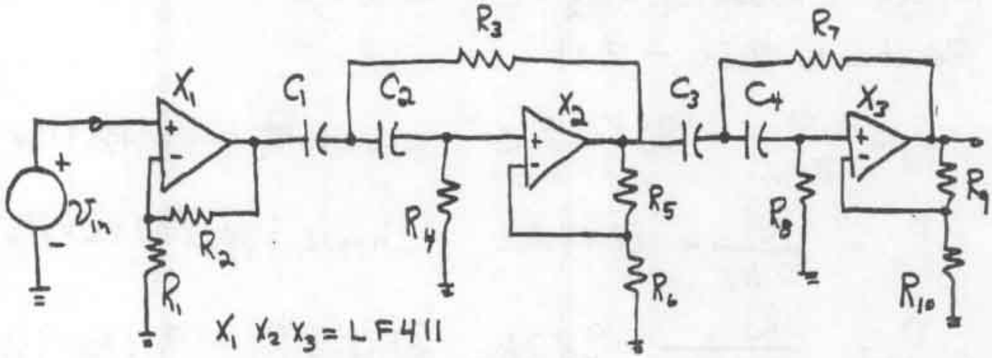
Problem 11.8

The simulation file is P11_8. Gain magnitude plots for 10 runs are:



Problem 11.9

Here is one solution:



$C_1 = C_2 = C_3 = C_4 = 1000\,pF \pm 5\%$ $R_1 = R_6 = R_{10} = 100\,k\Omega \pm 1\%$

$R_3 = R_4 = R_7 = R_8 = 536\,k\Omega \pm 1\%$ $R_2 = 287\,k\Omega \pm 1\%$

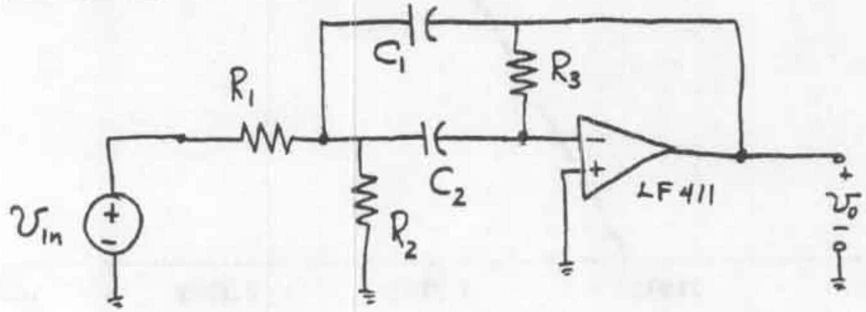
$R_5 = 15.0\,k\Omega \pm 1\%$ $R_9 = 124\,k\Omega \pm 1\%$

The simulation (P11_9) shows that the circuit meets the desired specifications.

Problem 11.10

For a bandpass filter having $f_0/B \cong 1$ we would cascade a low-pass filter with a high-pass filter. For $f_0/B >> 1$, we use the Delyiannis-Friend circuit shown in Figure 11.12a on page 740 in the book.

Problem 11.11



$$Q = \frac{f_0}{B} = \frac{100\,Hz}{20\,Hz} = 5 \qquad H_0 = 5$$

First choose* $C_1 = C_2 = C = 0.018\mu F$ then by Equations 9.30 – 9.31

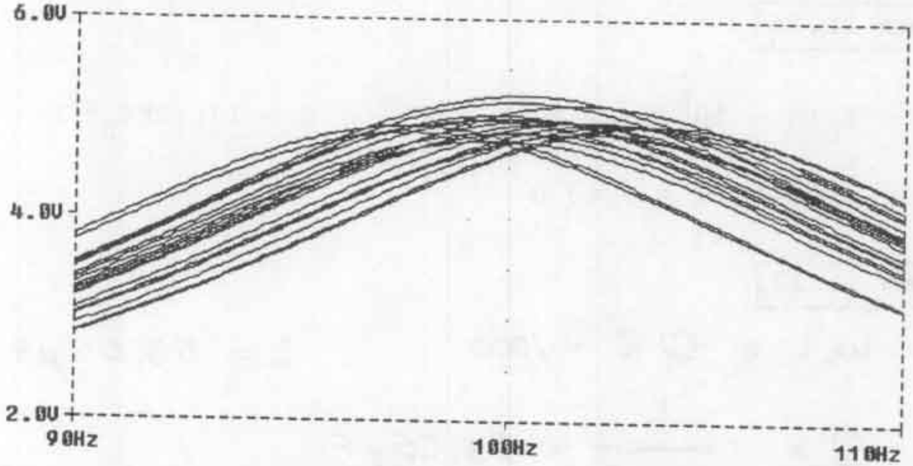
$$R_3 = \frac{Q}{\pi f_0 C} = 884.2\,k\Omega \quad \text{choose } R_3 = 887\,k\Omega \pm 1\%$$

$$R_1 = \frac{R_3}{2H_0} = 88.42\,k\Omega \quad \text{choose } R_1 = 88.7\,k\Omega \pm 1\%$$

$$R_2 = \frac{R_3}{4Q^2 - 2H_0} = 9.82\,k\Omega \quad \text{choose } R_2 = 9.76\,k\Omega \pm 1\%$$

* Choose C as small as possible but not so small that the resistors are too large. It is good to keep $R_3 \lesssim 1M\Omega$.

Using the Monte Carlo simulation (P11_11) we obtained the gain plots shown on the next page.



Using these plots we estimate the center frequency as approximately 100 Hz ± 3% and the center frequency gain as 5 ± 5%.

Problem 11.12

See page 744 and Figure 11.19 on page 746 in the book.

Problem 11.13

See Figure 11.20 on page 747 in the book. $Q = f_0/B$

Problem 11.14

$Q = f_0/B = 10^7/10^5 = 100$

$C = 1/[(2\pi f_0)^2 L] = 50.66$ pF

$R = (2\pi f_0 L)/Q = 3.14\ \Omega$

Problem 11.15

$f_0 = 1/(2\pi\sqrt{LC}) = 1.592$ MHz

$Q = \omega_0 L/R = 50 \quad B = f_0/Q = 31.8$ kHz

$f_L \cong f_0 - B/2 = 1576$ kHz $\qquad f_H \cong f_0 + B/2 = 1608$ kHz

Problem 11.16

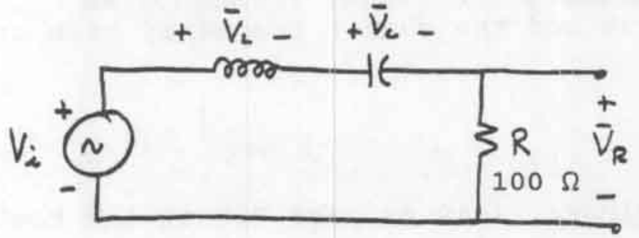
$Q = f_0/B = 10^8/(5 \times 10^6) = 20 \qquad C = 1/[(2\pi f_0)^2 L = 8.44\ \text{pF}$

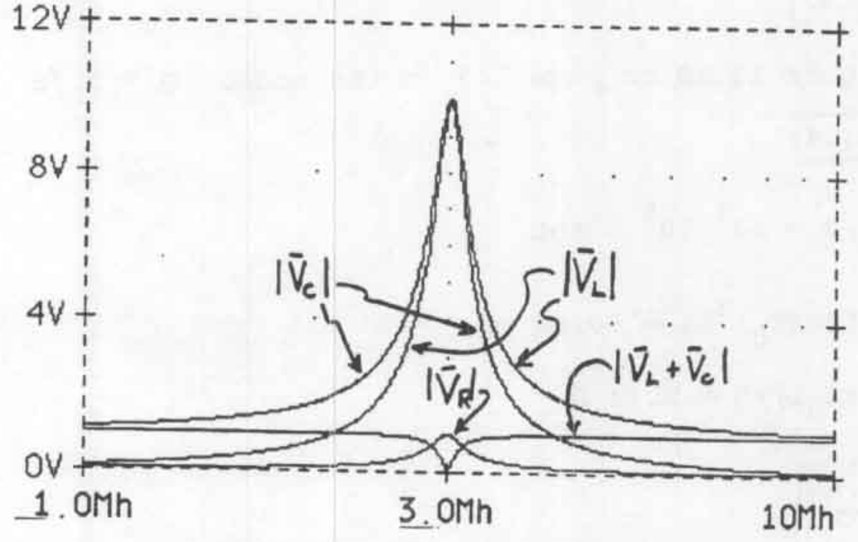
$R = (2\pi f_0 L)/Q = 9.42\ \Omega$

Problem 11.17

$\omega_0 L = QR = 1000 \qquad L = 53.05\ \mu H$

$$C = \frac{1}{\omega_0 Q R} = 53.05\ pF$$





The simulation file is P11_17. At resonance $|\mathbf{V}_C| = |\mathbf{V}_L| = 10$ V and $|\mathbf{V}_R| = 1$ V. The peak value of $|\mathbf{V}_L|$ occurs slightly above resonance (3.008 MHz) and the peak value of $|\mathbf{V}_C|$ occurs slightly below resonance (2.992 MHz).

Problem 11.18

We have $B = f_0/Q$, $f_0 = 1/(2\pi\sqrt{LC})$, and $Q = 2\pi f_0 L/R$. Solving for B in terms of component values, we obtain:

$$B = \frac{R}{2\pi L}$$

Therefore, in a series resonant circuit, to vary the center frequency with constant bandwidth, we choose a constant inductance and variable capacitance.

Problem 11.19

We have $f_{min} = \dfrac{1}{2\pi\sqrt{L_{max}C}}$ and $f_{max} = \dfrac{1}{2\pi\sqrt{L_{min}C}}$. Taking the ratio of the respective sides of these equations and simplifying, we obtain

$$f_{max}/f_{min} = \sqrt{L_{max}/L_{min}}$$

For a $f_{max}/f_{min} = 2$ we need $L_{max}/L_{min} = 4$.

Problem 11.20

The circuit must be resonant at $f_1 = 10$ MHz $= 1/(2\pi\sqrt{LC})$. The voltage transfer ratio is given by Equation 11.25 on page 745 in the book:

$$A_v(j\omega) = \frac{j\omega/\omega_0}{Q[1 - (\omega/\omega_0)^2] + j(\omega/\omega_0)}$$

Substituting $f = f_2 = 15$ MHz, $f_0 = f_1 = 10$ MHz, setting the magnitude of A_v equal to 0.01 and solving for Q we obtain Q = 120. Then we have $B = f_0/Q = 83.3$ kHz, $L = QR/\omega_0 = 95.49$ μH, and $C = 1/(\omega_0 QR) = 2.65$ pF. It is questionable whether these values are practical. See Figure 11.35 on page 760 in the book.

Problem 11.21

Let ω_0 denote the fundamental frequency of the square wave and ω_R denote the resonant frequency. To pass the third harmonic we want $\omega_R = 3\omega_0 = 3$ MHz. At the input, the amplitude of the fundamental is three times larger than the third harmonic. Thus we must have:

$$|A_V(j\omega)|^2 = \left(\frac{0.01}{3}\right)^2 = \frac{(\omega_0/\omega_R)^2}{Q^2[1 - (\omega_0/\omega_R)^2]^2 + (\omega_0/\omega_R)^2}$$

$$\left(\frac{0.01}{3}\right)^2 = \frac{(1/3)^2}{Q^2[1 - (1/3)^2]^2 + (1/3)^2}$$

Solving we find $Q = 112.5$, $L = QR/\omega_R = 298.42$ μH and $C = 1/(\omega_R QR) = 9.4314$ pF. The simulation file is P11_21.

Problem 11.22

See Figure 11.25 on page 751 and Figure 11.26 on page 752 in the book.

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \qquad Q = \frac{R}{\omega_0 L} = R\sqrt{\frac{C}{L}}$$

Problem 11.23

$$R = Q\omega_0 L = 15.7\ \text{k}\Omega \qquad C = 1/(\omega_0^2 L) = 5.07\ \text{pF}$$

$$B = f_0/Q = 2\ \text{MHz}$$

$$f_H \cong f_0 + B/2 = 101\ \text{MHz} \qquad f_L \cong f_0 - B/2 = 99\ \text{MHz}$$

Problem 11.24

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = 1.125\ \text{MHz} \qquad Q = \frac{R}{\omega_0 L} = 14.1$$

$B = f_0/Q = 79.5$ kHz

$f_H \cong f_0 + B/2 = 1.165$ MHz $\qquad f_L \cong f_0 - B/2 = 1.085$ MHz

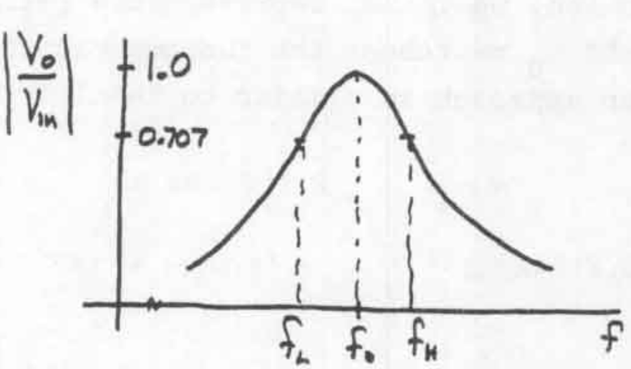
Problem 11.25

(a) $f_0 = \dfrac{1}{2\pi\sqrt{LC}} = 100$ kHz $\qquad Q = \dfrac{R}{\omega_0 L} = 15.92$

$B = f_0/Q = 6.283$ kHz

$f_H \cong f_0 + B/2 = 103.1$ kHz $\qquad f_L \cong f_0 - B/2 = 96.9$ kHz

(b)



(c) The simulation file is P11_25. The results of the simulation agree very well with the values determined above.

Problem 11.26

As in Example 11.4, the Fourier series for the square wave is:

$$i(t) = \frac{4A}{\pi}[\sin(\omega_0 t) + \frac{1}{3}\sin(3\omega_0 t) + \ldots]$$

in which A = 1 mA is the amplitude of the square wave and $f_0 = 1$ MHz is the fundamental frequency.

We design the circuit so the resonant frequency is 1 MHz. At resonance, the impedance of the circuit is R, and the peak voltage due to the fundamental component is 10 V = $R(4A/\pi)$. This yields R = 7.85 kΩ. For the third harmonic we have 0.2 V =

$|Z(j3\omega_0)|[4A/(3\pi)]$ which yields $|Z(j3\omega_0)| = 471\ \Omega$. The impedance is given by Equation 11.36 on page 751 in the book. Taking the magnitude squared of both sides of the equation and substituting values, we have

$$(471)^2 = (7850)^2 \frac{(3)^2}{Q^2[1 - (3)^2]^2 + 3^2}$$

Solving we find $Q = 6.236$. Then $L = R/(Q\omega_0) = 200.26\ \mu H$ and $C = 1/(\omega_0^2 L) = 126.49$ pF. The simulation file is P11_26.

Problem 11.27

In this problem, we let ω_R represent the resonant frequency of the circuit and ω_0 represent the fundamental frequency of the square wave. Our approach is similar to that for Problem 11.26.

$$10 = R\,\frac{4A}{3\pi} \quad \Rightarrow \quad R = 23.56\ k\Omega$$

$$0.2 = |Z(j\omega_0)|(4A/\pi) \quad \Rightarrow \quad |Z(\omega_0)| = 157.1\ \Omega$$

$$|Z(\omega_0)|^2 = (157.1)^2 = (23560)^2 \frac{(1/3)^2}{Q^2[1 - (1/3)^2]^2 + (1/3)^2}$$

Solving we find $Q = 56.23$. Then $L = R/(Q\omega_R) = 22.22\ \mu H$ and $C = 1/(\omega_0^2 L) = 126.63$ pF. The simulation file is P11_27.

Problem 11.28

$$B = \frac{\omega_0}{2\pi Q} = \frac{\omega_0}{2\pi(R/\omega_0 L)} = \frac{\omega_0^2 L}{2\pi R} = \frac{(1/LC)L}{2\pi R} = \frac{1}{2\pi RC}$$

Thus to vary f_0 with constant bandwidth in a parallel resonant circuit, we should use a variable inductor. (On the other hand in Problem 11.18 we found that using a variable capacitor is needed for constant bandwidth in a series resonant circuit.)

Problem 11.29

$$X_p = X_s = X \qquad Q_p = Q_s = Q = X/R_s \qquad R_p = QX = Q^2R_s$$

Problem 11.30

For f = 100 kHz:

$$Q_s = \omega L/R = 12.6 \qquad L_p = L_s = 1 \text{ mH} \qquad R_p = X^2/R_s = 7.9 \text{ k}\Omega$$

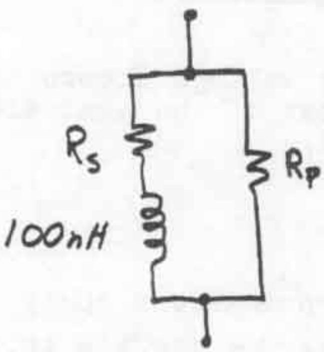
For f = 200 kHz:

$$Q_s = \omega L/R = 25.1 \qquad L_p = L_s = 1 \text{ mH} \qquad R_p = X^2/R_s = 31.6 \text{ k}\Omega$$

Problem 11.31

$$Q_p = R\omega C = 12.57 \qquad Q_s = Q_p = 12.57 \qquad R_s = R_p/Q^2 = 6.33\ \Omega$$

Problem 11.32



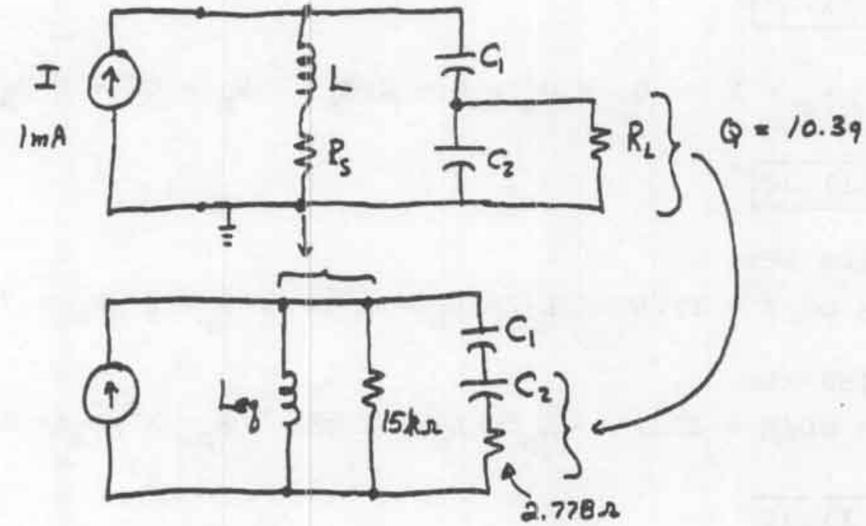
$$\frac{R_p}{\omega L} = 2Q = 150$$

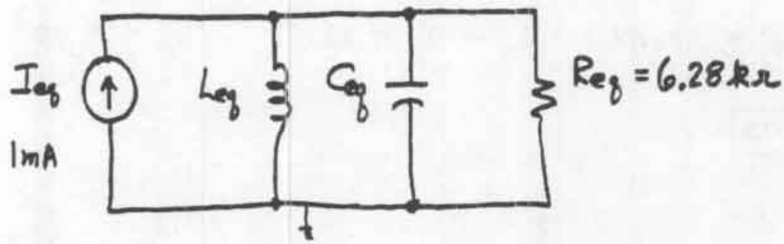
$$R_p = 18.9\text{ k}\Omega$$

$$\frac{\omega L}{R_s} = 2Q = 150 \Rightarrow R_s = 0.838\,\Omega$$

Problem 11.33

Let us assume that high-Q approximations are valid. Then $L_{eq} = L = 0.5\ \mu H$ and $C_{eq} = 1/(1/C_1 + 1/C_2) = 16.67$ pF. Also we have $f_0 = \left[2\pi\sqrt{L_{eq}C_{eq}}\right]^{-1} = 55.133$ MHz.

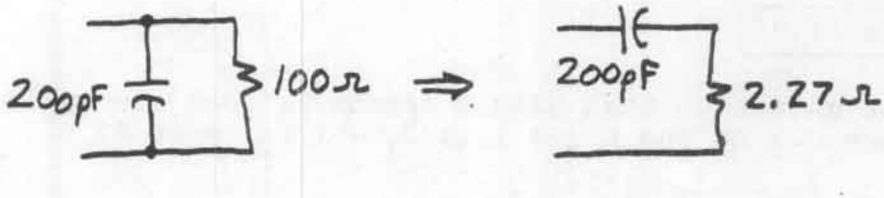


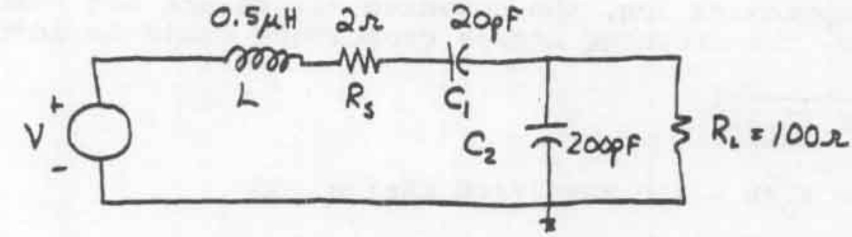


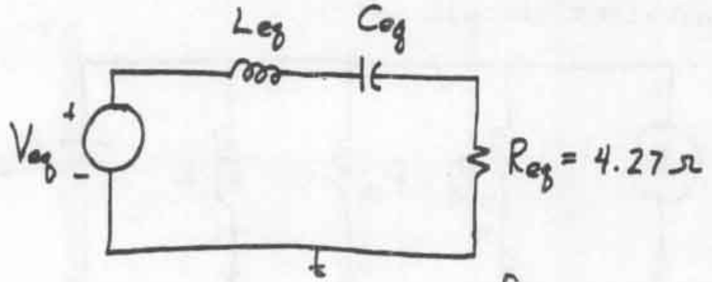
A simulation comparing the voltage across the current source in the original circuit with that of the equivalent circuit is stored in the file named P11_33.

Problem 11.34

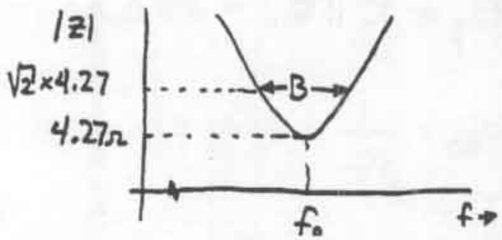
We assume that high-Q approximations apply. Then we have $L_{eq} = L = 0.5\ \mu H$ and $C_{eq} = 1/(1/C_1 + 1/C_2) = 18.1818$ pF. Also we have $f_0 = \left[2\pi\sqrt{L_{eq}C_{eq}}\right]^{-1} = 52.79$ MHz.







$$Q_{eq} = 38.81 \qquad B = \frac{f_0}{Q_{eq}} = 1.36\ \text{MHz}$$



The simulation file is P11_34. The original circuit and the series equivalent have nearly identical impedances over the frequency range from 50 MHz to 55 MHz.

Problem 11.35

The functions of the matching network in a class-D amplifier are to filter out undesired harmonics (or the dc component) and to step the amplitude of the desired term either up or down as needed to achieve the desired output power.

Problem 11.36

Following the approach of Example 11.8, we obtain

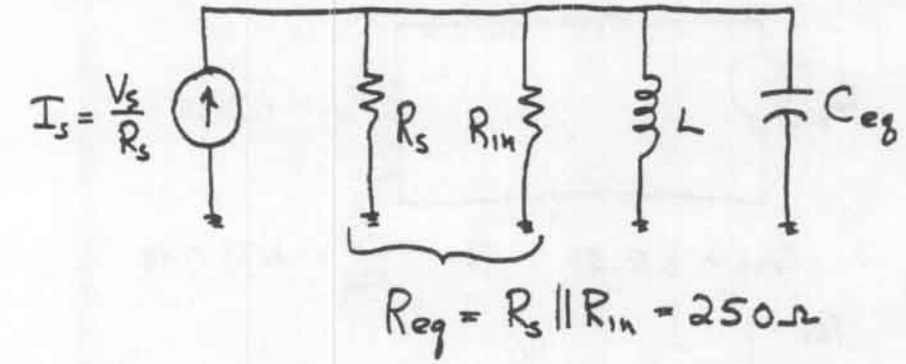
$L = 23.05$ nH $\qquad C_1 = 77.6$ pF $\qquad C_2 = 160$ pF

As in the example we have assumed an unloaded Q of 200. A simulation can be found in P11_36. We ran the program and adjusted L (ending up at 22.94 nH) to achieve a resonant frequency of exactly 145 MHz. (Because of inaccuracies of the high-Q approximation, the computed values are not exact. In practice, the inductor and/or capacitors would be adjustable.)

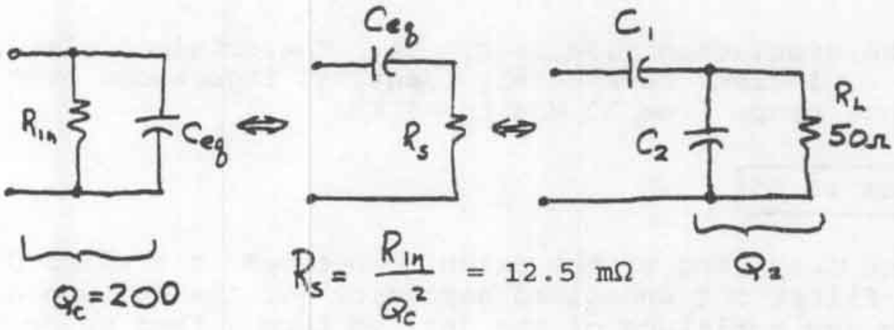
Problem 11.37

$$Q = f_0/B = (10\ \text{MHz})/(100\ \text{kHz}) = 100$$

The parallel equivalent circuit is:



$L = R_{eq}/(Q\omega_0) = 39.8$ nH $\qquad C_{eq} = \frac{1}{\omega_0^2 L} = 6364$ pF



$$R_s = \frac{R_{in}}{Q_c^2} = 12.5\ \text{m}\Omega$$

$$Q_2^2 = R_L/R_s = 63.24 = \omega_0 C_2 R_L \Rightarrow C_2 = 20.13\ \text{nF}$$

$$C_{eq} = \frac{1}{1/C_1 + 1/C_2} \Rightarrow C_1 = 9.305\ \text{nF}$$

The simulation file is P11_37.

Problem 11.38

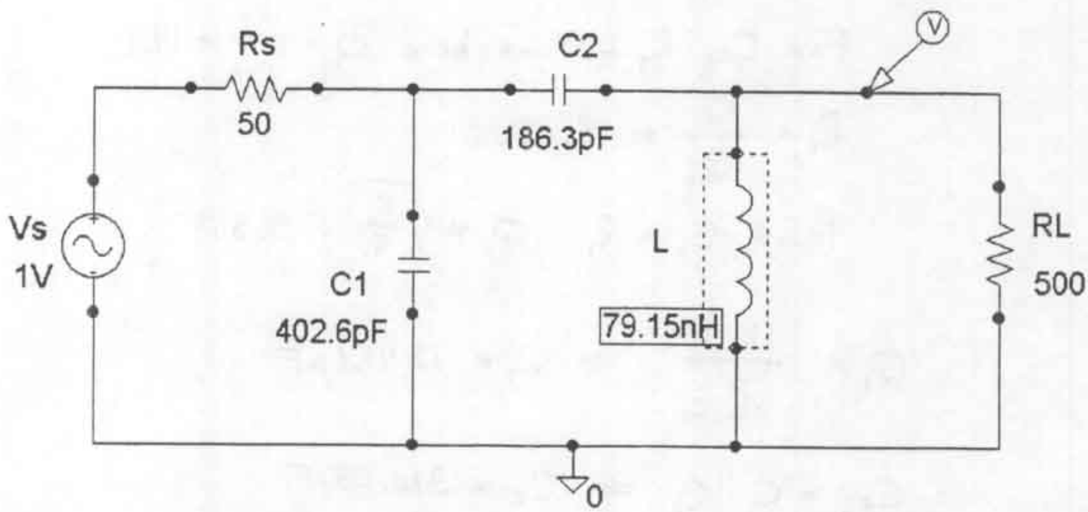
Following the approach used in solving Problem 11.37, we obtain $Q = 5$, $L = 795.8$ nH, $C_{eq} = 318.18$ pF, $R_s = 2.5\ \Omega$, $Q_2 = 4.47$, $C_2 = 1423.5$ pF, and $C_1 = 409.77$ pF. The simulation file is P11_38. Because Q_2 is relatively low, the results are not exact. However we can make minor adjustments by trial and error to achieve the desired performance. This yields $L = 795.8$ nH, $C_1 = 459.93$ pF, and $C_2 = 970$ pF. In practice, some of the components are usually adjustable.

Problem 11.39

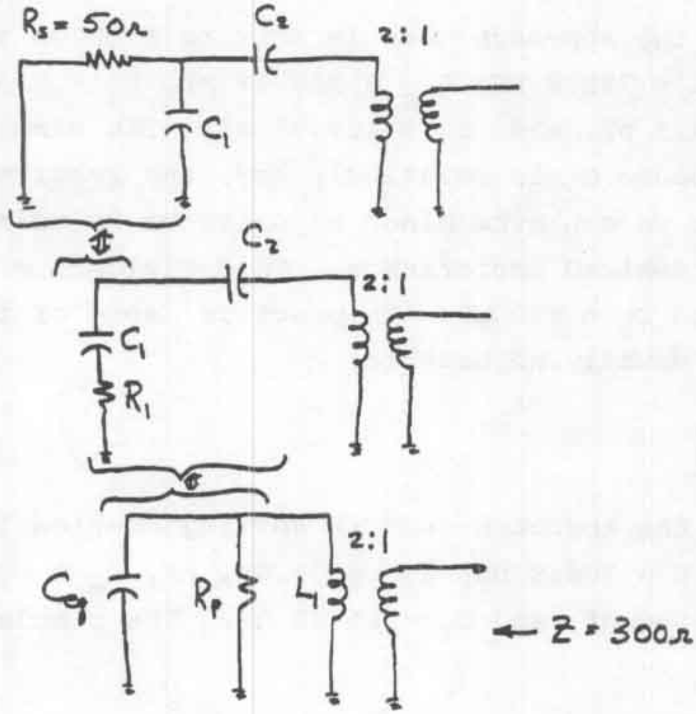
Following the approach used in solving Problem 11.37, we obtain $Q = 50$, $L = 795.8$ nH, $C_{eq} = 31.831$ nF, $R_s = 0.50$ mΩ, $Q_2 = 31.63$, $C_2 = 100.66$ nF, and $C_1 = 46.55$ nF. The simulation file is P11_39.

Problem 11.40

Here is one answer. Other correct answers exist. The simulation file is P11_40.



Problem 11.41



Now $Z = \left(\frac{1}{2}\right)^2 R_p$ thus $R_p = 1200\Omega$

$\omega_0 = \frac{1}{\sqrt{C_{eq} L_1}}$ thus $C_{eq} = 253.3\,pF$

For $C_{eq}\ R_p\ L_1$ we have $Q_{eq} = \frac{R_p}{\omega_0 L_1} = 19.1$

$R_1 = \frac{R_p}{Q_{eq}^2} = 3.29\,\Omega$

For C_1 & R_1 $Q_1 = \sqrt{\frac{R_s}{R_1}} = 3.899$

$Q_1 = \frac{R_s}{1/\omega_0 C_1} \Rightarrow C_1 = 1241.1\,pF$

$C_{eq} = C_1 \| C_2 \Rightarrow C_2 = 318.25\,pF$

Including refected input resistance of Q_1, the resistance in parallel with L_1 is

$$R_p' = R_p \| 2000\Omega = 750\Omega$$

$$Q = \frac{R_p'}{\omega_o L} = 11.94 \quad B = \frac{f_o}{Q} = 838\ kHz$$

Problem 11.42

C_c acts as a short at the resonant frequency. Because $|V_o| >> |V_{id}|$ we can (approximately) assume that C_{gd} is in parallel with C. Thus

$$C_{eq} \cong C + C_{gd} = 31pF$$

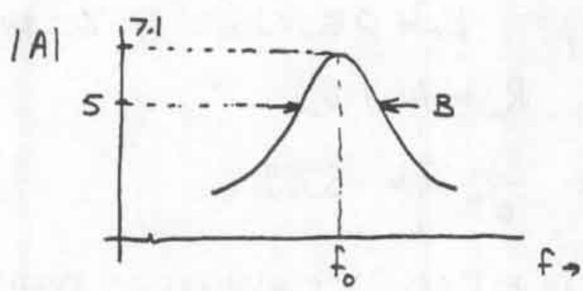
$$f_o = \frac{1}{2\pi\sqrt{L\,C_{eq}}} = 40.43\ MHz$$

$$R_p = Q_{coil}\,\omega_o L = 19.05\ k\Omega$$

$$R_{eq} = R_L \| R_p \| r_d = 2.84\ k\Omega$$

$$Q = \frac{R_{eq}}{\omega_o L} = 22.3$$

$$B = 1.81\ MHz \qquad |A_o| = g_m R_{eq} = 7.1$$



Problem 11.43

The circuit configuration is shown in Figure 11.48 on page 776 in the book. We can use a 1:1 turns ratio and $C_{neut} = C_{gd} = 1$ pF. Other combinations will also work such as a neutralization coil with half as many turns as L and $C_{neut} = 2C_{gd} = 2$ pF.

Problem 11.44

$$Q = \frac{f_0}{B} = 50$$

From Figure 11.35 we choose

$L = 100\ \mu H$ (Practical range ≈ $5\mu H - 500\mu H$)

$$C = \frac{1}{\omega_0^2 L} = 253.3\ pF$$

$$R_p = Q_{coil}\, \omega_0 L = 125.7\ k\Omega$$

$$R = Q\, \omega_0 L = 31.42\ k\Omega$$

$$R = R_L \| R_p \| r_d \Rightarrow R_L = -40.9\ k\Omega$$

but this is not possible. Therefore we must make a new choice for L.

Say $L = 20\mu H$ Then

$C = 1266\ pF$ $R_p = 25.14\ k\Omega$ $R = 6.284\ k\Omega$

and then $R_L = 14.1\ k\Omega$

$$A_v(\omega_0) = -g_m R = -37.9$$

The simulation file is P11_44. The simulation results agree very well with the design calculations.

Problem 11.45

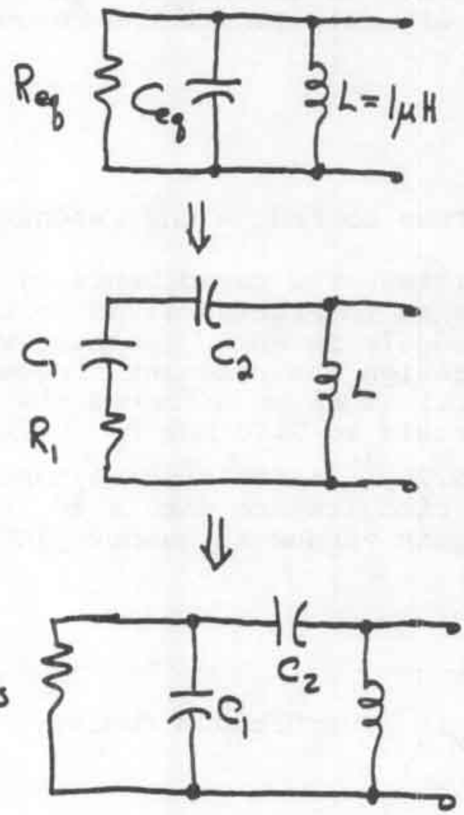
(a) $K = I_{DSS}/V_{to}^2 = (4 \times 10^{-3})/(-2)^2 = 1 \text{ mA/V}^2$

$$I_{DQ} = K(V_{GSQ} - V_{to})^2 \quad \Rightarrow \quad V_{GSQ} = -0.585 \text{ V}$$

$$R_{s1} = R_{s2} = (15 + 0.585)/I_{DQ} = 7.79 \text{ k}\Omega$$

Thus we choose the standard value $R_{s1} = R_{s2} = 8.2 \text{ k}\Omega$.

(b)



$$Q = f_0/B = (10 \text{ MHz})/(500 \text{ kHz}) = 20$$

$$C_{eq} = 1/\omega_0^2 L = 253.3 \text{ pF}$$

$$R_{eq} = Q\omega_0 L = 1257 \ \Omega$$

$$R_1 = R_{eq}/Q^2 = 3.142 \ \Omega$$

$$Q_1 = 1/\omega_0 C_1 R_1 = \sqrt{R_s/R_1} = 3.99$$

$$C_1 = 1269 \text{ pF}$$

$$C_{eq} = \frac{1}{1/C_1 + 1/C_2}$$

$$C_2 = 316.43 \text{ pF}$$

(c) This part is very similar to part (b). The results are C_3 = 256.51 pF and C_4 = 20.21 nF.

(d) First we compute g_m for the transistors.

$$g_m = \frac{2\sqrt{I_{DSS} I_{DQ}}}{|V_{to}|} = 2.83 \text{ mS}$$

The voltage gain at resonance is the product of three terms:

(1) voltage step up in the input circuit
(2) voltage gain of the differential pair
(3) voltage step down in the output circuit

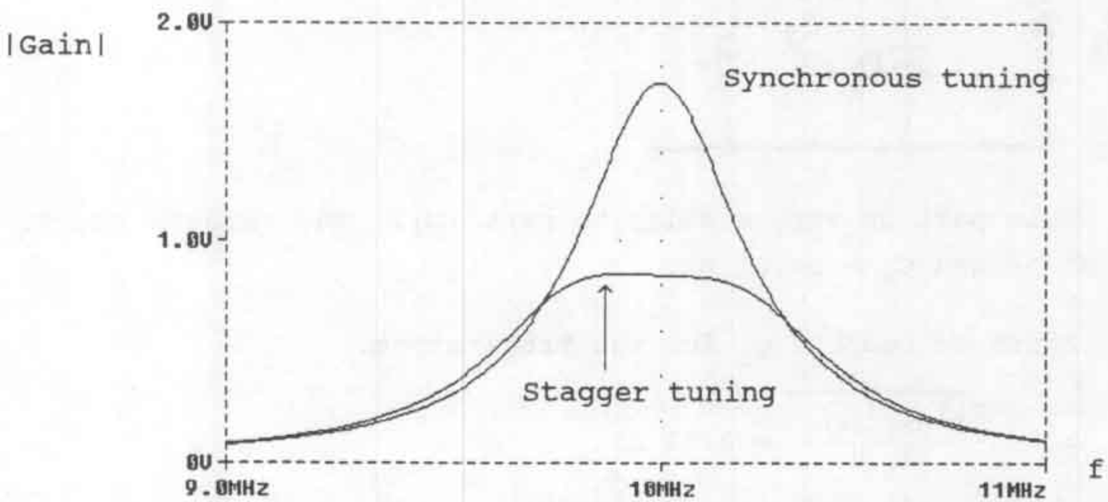
Factors 1 and 3 offset one another and the voltage gain is

$$A_V = g_m R_{eq}/2 = 1.78$$

(e) The simulation file is P11_45. The results of the simulation agree very well with the design calculations. Keep in mind that the overall bandwidth is less than 500 kHz because two tuned circuits are cascaded. Also, the resonant frequency is slightly low because of the approximate calculations. In practice, we would have adjustable elements to set the resonant frequencies.

Problem 11.46

Recall that $f_0 = 1/(2\pi\sqrt{LC})$. Thus to reduce the resonant frequency by a factor x we must multiply the capacitance by x^2. First we adjusted the circuit designed in Problem 11.45 so the resonant frequencies were almost exactly 10 MHz. (Because we used high-Q approximations in the design the resonant frequencies were slightly different from 10 MHz.) Then we adjusted the resonant frequency of the input circuit to 9.75 MHz by increasing the capacitances by the ratio $(10/9.75)^2$. Similarly we tuned the output circuit to 10.25 MHz. Both circuits are simulated in the file named P11_46. The resulting gain versus frequency plots are:

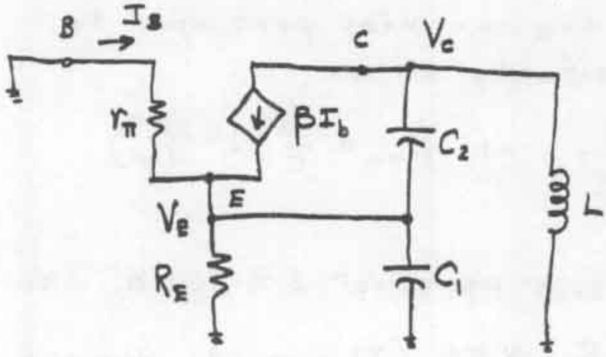


Problem 11.47

See pages 780-781 in the book.

Problem 11.48

(a)



(b) $I_B = -\dfrac{V_E}{r_\pi}$

Write node equations:

$$\frac{V_E}{R_E} + \frac{V_E}{r_\pi} + \beta \frac{V_E}{r_\pi} + j\omega C_1 V_E + j\omega C_2 (V_E - V_c) = 0$$

$$\frac{V_c}{j\omega L} + j\omega C_2 (V_c - V_E) - \beta \frac{V_E}{r_\pi} = 0$$

Set system determinant to zero:

$$\begin{vmatrix} \left[\frac{1}{R_E} + \frac{\beta+1}{r_\pi} + j\omega(C_1+C_2)\right] & -j\omega C_2 \\ \left(-j\omega C_2 - \frac{\beta}{r_\pi}\right) & j\omega C_2 - j\frac{1}{\omega L} \end{vmatrix} = 0$$

Next we expand the determinant and set the real part to zero this eventually yields

$$\omega = \frac{1}{\sqrt{L C_{eq}}} \quad \text{where } C_{eq} = \frac{1}{1/C_1 + 1/C_2}$$

Then we set the imaginary part equal to zero and eventually obtain

$$\frac{C_2}{C_1} = \frac{\beta}{1 + \frac{r_\pi}{R_E}} \quad \text{or} \quad \beta_{min} = \frac{C_2}{C_1}\left(1 + \frac{r_\pi}{R_E}\right)$$

(c) From Figure 11.35 we select $L \approx 50 \mu H$. Also we design for $\beta_{min} \approx 50$ (This is the minimum $h_{fe} \approx \beta$ at $I_{CQ} = 1mA$ according to the data sheet.) Now $R_E \approx \frac{V_{EE}}{I_{CQ}} = 15 k\Omega$.

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{50\,(26mV)}{1mA} = 1300\Omega$$

$$\frac{C_2}{C_1} = \frac{\beta}{1 + \frac{r_\pi}{R_E}} = \frac{50}{1 + \frac{1.3}{15}} = 46$$

$$C_{eq} \approx \frac{1}{\omega^2 L} = \frac{1}{(2\pi \times 10^6)^2 \times 50 \times 10^{-6}} = 507 pF$$

Thus we choose nominal values:

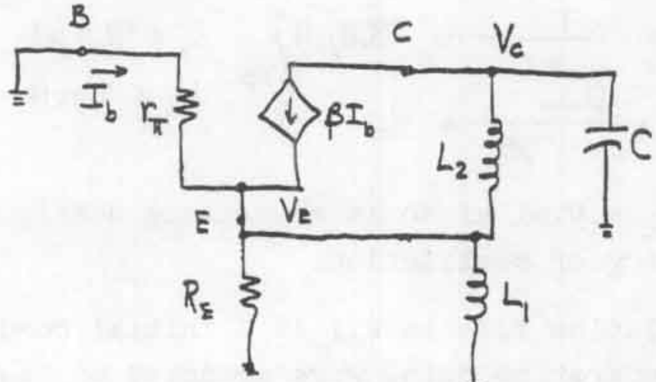
$C_1 = 560 pF$ $C_2 = 27000 pF$ and

finally settle on $L = 46.2 \mu H$

(d) The simulation file is P11_48. Initial conditions close to the eventual operating point were selected so the simulation settles into steady state sooner. The frequency is about 6% low. In practice the inductor could be variable so the frequency could be adjusted to the desired value.

Problem 11.49

(a)



(b) Write node voltage equations:

$$\frac{V_E}{r_\pi} + \beta\frac{V_E}{r_\pi} + \frac{V_E}{R_E} + \frac{V_E}{j\omega L_1} + \frac{V_E - V_c}{j\omega L_2} = 0$$

$$-\beta\frac{V_E}{r_\pi} + \frac{V_c - V_E}{j\omega L_2} + j\omega C V_c = 0$$

$$\begin{vmatrix} \frac{1}{R_E} + \frac{\beta+1}{r_\pi} + \frac{1}{j\omega L_1} + \frac{1}{j\omega L_2} & -\frac{1}{j\omega L_2} \\ -\frac{\beta}{r_\pi} - \frac{1}{j\omega L_2} & j\omega C + \frac{1}{j\omega L_2} \end{vmatrix} = 0$$

Eventually we have:

$$\omega = \frac{1}{\sqrt{C(L_1 + L_2)}} \qquad \beta_{min} = \frac{L_1}{L_2}\left(1 + \frac{r_\pi}{R_E}\right)$$

(c) Design for $\beta_{min} = 50$

$$R_E \approx \frac{V_{EE} - V_{BEQ}}{I_{CQ}} = 15\,k\Omega$$

$$r_\pi = \beta\frac{V_T}{I_{CQ}} = \frac{50\,(26mV)}{1mA} = 1300\,\Omega$$

Choose $C = 270\,pF$

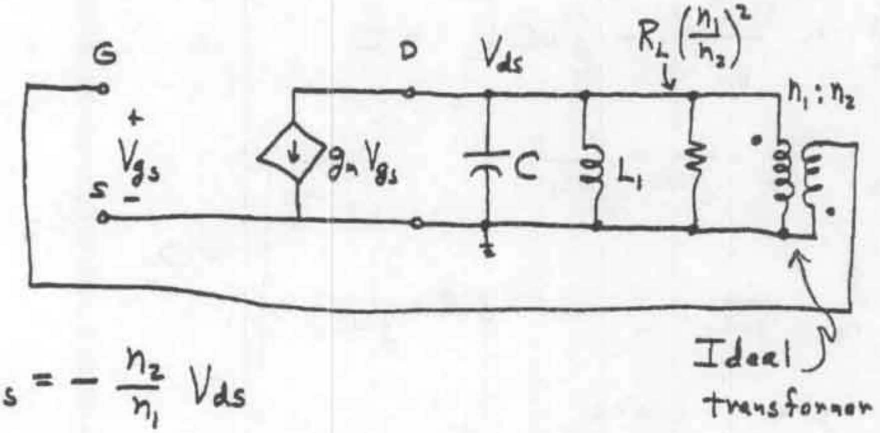
$$\left.\begin{array}{l} L_1 + L_2 = \dfrac{1}{\omega^2 C} = 93.8\mu H \\ \dfrac{L_1}{L_2} = \dfrac{\beta_{min}}{1 + r_\pi / R_B} = 46 \end{array}\right\} \Rightarrow \begin{array}{l} L_1 = 91.8\mu H \\ L_2 = 2\mu H \end{array}$$

We selected $C_C = 0.01\ \mu F$ so it appears as nearly a short circuit at the frequency of oscillation.

(d) The simulation file is P11_49. Initial conditions close to the eventual operating point were selected so the simulation settles into steady state sooner. The frequency is about 6% low. In practice, one of the components could be variable so the frequency could be adjusted to the desired value.

Problem 11.50

(a)



(b) $V_{gs} = -\dfrac{n_2}{n_1} V_{ds}$

Node voltage equation at node D:

$$-g_m\left(\frac{n_2}{n_1}\right)V_{ds} + j\omega C V_{ds} + \frac{V_{ds}}{j\omega L_1} + \frac{V_{ds}}{R_L\left(\frac{n_1}{n_2}\right)^2} = 0$$

Set imaginary terms equal to zero

This yields: $\omega = \frac{1}{\sqrt{L_1 C}}$

Set real terms equal to zero. This yields:

$$g_{m\,min} = \left(\frac{n_2}{n_1}\right)\frac{1}{R_L}$$

(c) According to data sheet* for $V_{DSQ} = 15V$ and $V_{GSQ} = 0$ $\quad g_{m\,min} = 3500\ \mu S$

We design assuming $g_{m\,min} = 2500\mu S$ to allow design margin.

Pick $C = 270pF$

Then $L_1 = \frac{1}{\omega^2 C} = 93.8\mu H$

$$\frac{n_2}{n_1} = g_{m\,min} R_L = 2500\times10^{-6}\times50 = 0.125$$

$$L_2 = \left(\frac{n_2}{n_1}\right)^2 L_1 = 1.46\mu H$$

* Look for the 2N5485 data sheet at:

http://www.fairchildsemi.com/pf/2N/2N5485.html

Problem 11.51

In the piezoelectric effect, application of an electric field produces forces on the charges in certain crystalline materials resulting in deformation. Similarly deformation of the crystal by an external force displaces charges, resulting in an electric field.

Problem 11.52

As an electronic component, a "crystal" is a piece of piezoelectric material (usually quartz) that has electrodes plated on it and is mounted so it can vibrate freely in certain modes.

Problem 11.53

See Figures 11.56 and 11.57 on pages 787 and 788 in the book.

Problem 11.54

The second overtone is at approximately double the fundamental mode.

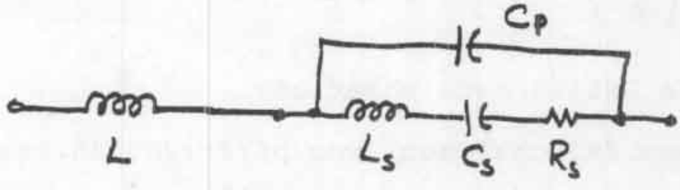
Problem 11.55

$$\frac{\pm 1 \text{ ms}}{1 \text{ day}} = \frac{\pm 10^{-3}}{24 \times 60 \times 60} = \pm 1.16 \times 10^{-8} = \pm 0.0116 \text{ ppm}$$

Most crystal oscillators are not capable of this degree of accuracy over several days.

Problem 11.56

The equivalent circuit is:



For frequencies close to series resonance of the crystal, we can neglect C_p because the impedance of the series branch of the crystal is very small in magnitude. Then the circuit is a simple series resonant circuit, and the resonant frequency is $f_s = 1/\sqrt{C_s(L + L_s)}$. Thus adding series inductance lowers the frequency of oscillation.

Problem 11.57

Adding capacitance in parallel with the crystal has the effect of increasing the value of C_p. Therefore, the antiresonant frequency is lowered. (See Figure 11.57 and consider the effect on f_p when $|X_{Cp}|$ is lowered in magnitude.)

Problem 11.58

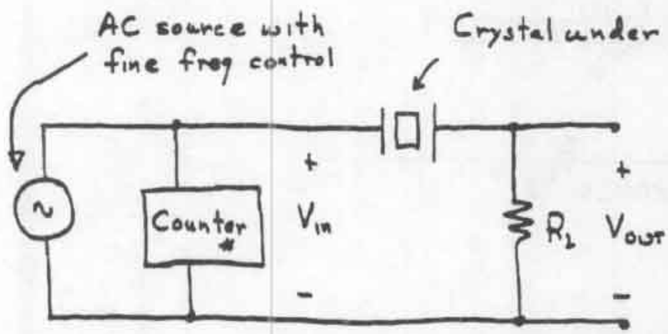
$$L_s = R_s Q/\omega_s = 31.8310 \text{ mH} \qquad C_s = 1/(Q\omega_s R_s) = 0.0318310 \text{ pF}$$

$$f_p = \frac{1}{2\pi\sqrt{L_s C_{eq}}} \qquad \text{where } C_{eq} = \frac{1}{1/C_s + 1/C_p} = 0.0317468 \text{ pF}$$

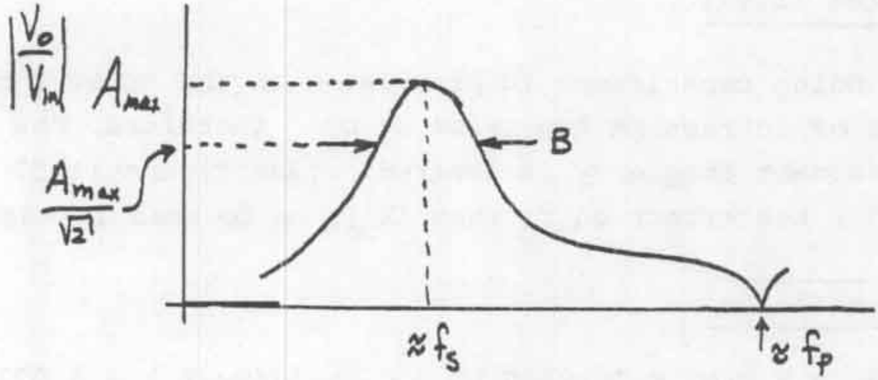
$$f_p = 5.0066 \text{ MHz}$$

Problem 11.59

(a) Set up the system shown below.



Use the counter to accurately measure the frequency of the source. Choose $R_L \cong R_s$ of the crystal. Start with about 50 Ω and adjust as needed. Observe the voltage transfer function magnitude $|V_o/V_{in}|$ which will appear much like the sketch shown on the next page. From the plot, determine the peak A_{max}, f_s at which the transfer function peak occurs, the half-power bandwidth B of the peak, and f_p which is the frequency of the null.



Then the crystal parameters can be calculated:

$$A_{max} = \frac{R_L}{R_s + R_L} \quad \Rightarrow \quad R_s = \frac{1 - A_{max}}{A_{max}} \times R_L$$

$$Q_{circuit} = \frac{f_s}{B} = \frac{\omega_s L_s}{R_s + R_L} = \frac{1}{\omega C_s (R_s + R_L)}$$

$$L_s = \frac{(R_s + R_L) Q_{circuit}}{\omega_s}$$

$$C_s = \frac{1}{\omega_s Q_{circuit} (R_s + R_L)}$$

$$Q = \frac{\omega_s L_s}{R_s}$$

(b) Given $f_s = 1.000000$ MHz, $f_p = 1.000500$ MHz, $R_s = 300\ \Omega$ and $Q = 10{,}000$ we have:

$$L_s = R_s Q/\omega_s = 477.465 \text{ mH}$$

$$C_s = 1/(Q\omega_s R_s) = 53.0516 \times 10^{-15} \text{ F}$$

Let $C_{eq} = \frac{1}{1/C_s + 1/C_p}$ denote the parallel equivalent capacitance. Then we have:

$$C_{eq} = \frac{1}{\omega_p^2 L_s}$$

$$= 52.9986 \times 10^{-15} \text{ F}$$

$$C_p = \frac{1}{1/C_{eq} - 1/C_s}$$

$$= 53 \text{ pF}$$

Problem 11.60

(a) For the current through C_{neut} to cancel the current through C_p, we need $C_{neut} = C_p = 6$ pF

(b) Consider the circuit of Figure P11.60a on page 798 in the book. Near the series resonant frequency, the reactance of C_p is much larger than the impedance of the series arm of the crystal. Thus, we can ignore C_p, and we have a simple series resonant circuit for which:

$$Q \cong \frac{\omega_s L_s}{R_{sa} + R_s + R_{La}}$$

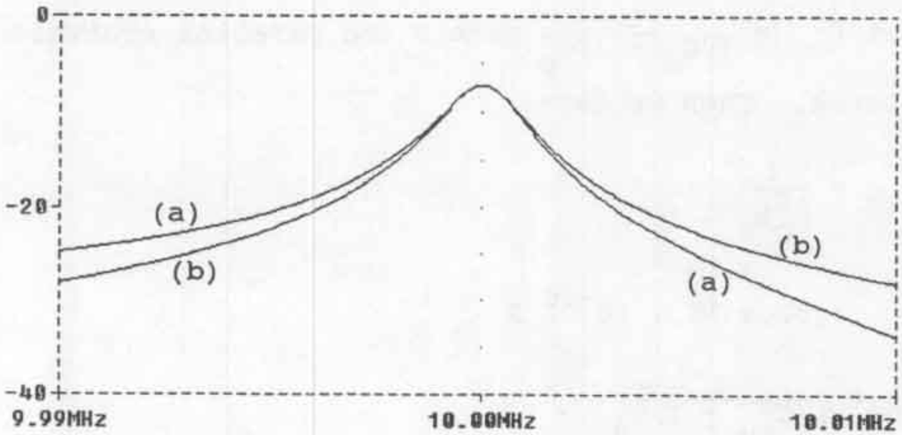
$$= \frac{2\pi 10^7 (10.132 \times 10^{-3})}{50 + 15 + 50}$$

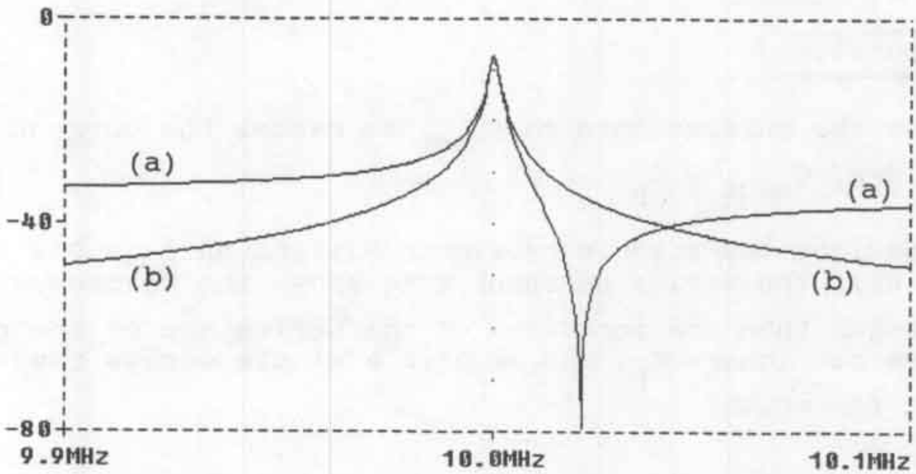
$$= 5536$$

$$B = f_s/Q = 1.80 \text{ kHz}$$

In the circuit of Figure P11.60b, the current through C_p is canceled by the current through C_{neut} so the half-power bandwidth is approximately 1.8 kHz as well.

(c) Both circuits are included in the simulation file P11_60. Plots of the transfer ratio magnitudes are shown on the next page.

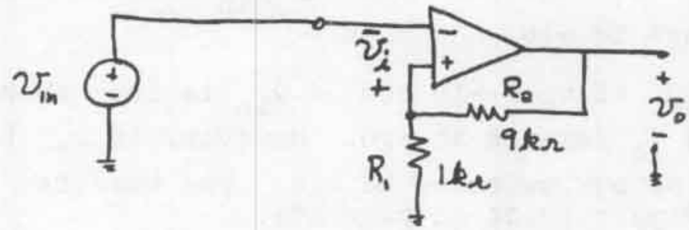




In the passband, both circuits have about the same performance. The half-power bandwidth agrees very well with the value calculated earlier (1800 Hz) However, circuit b has better attenuation for signals well outside of the passband.

Chapter 12

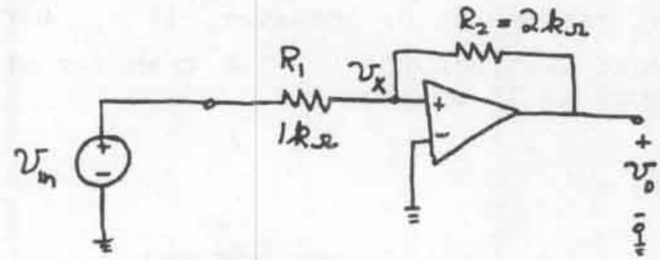
Exercise 12.1



The voltage across R_1 is equal to $v_o/10$. Thus, the input to the comparator is $v_i = 0.1v_o - v_{in}$. When $v_o = 0$, this becomes $v_i = -v_{in}$. As long as v_{in} is positive, v_i is negative, and the output remains at zero. When v_{in} becomes negative, v_i becomes positive, and the output switches to +5 V.

When $v_o = +5$, we have $v_i = 0.5 - v_{in}$. As long as v_{in} is less than 0.5 V, v_i is positive, and the output remains at +5. However, when v_{in} exceeds 0.5, the output switches to zero. The transfer characteristic is shown in Figure 12.13 on page 808 in the book.

Exercise 12.2



Writing a node equation at the noninverting input, we have:

$$\frac{v_x - v_{in}}{R_1} + \frac{v_x - v_o}{R_2} = 0$$

Solving for v_x and substituting values, we have:

$$v_x = 0.667v_{in} + 3.333 \quad \text{for } v_o = +10$$

$$v_x = 0.667v_{in} - 3.333 \quad \text{for } v_o = -10$$

Thus if $v_o = +10$ and if v_{in} is greater than -5, v_x is positive, and v_o remains at +10. However, if v_{in} becomes less than -5, the output switches to -10.

Similarly, if $v_o = -10$ and if v_{in} is less than +5, v_x is negative, and v_o remains at -10. However, if v_{in} becomes greater than +5, the output switches to +10. The transfer characteristic is shown in Figure 12.14 on page 808.

Exercise 12.3

Using the same approach as in the solution to Exercise 12.2, we obtain

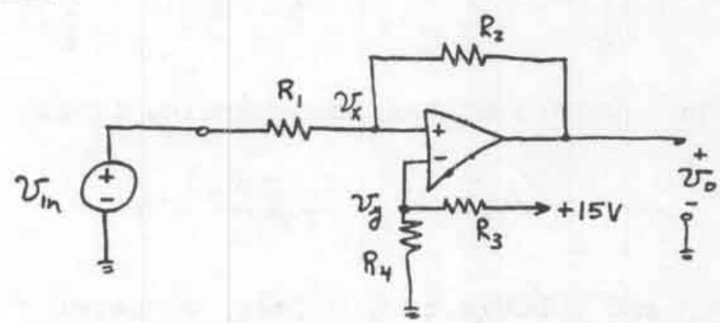
$$v_x = 0.667v_{in} - 1.667 \quad \text{for } v_o = 5$$

$$v_x = 0.667v_{in} \quad \text{for } v_o = 0$$

Thus, if $v_o = 5$ and if v_{in} is greater than -2.5, v_x is positive, and v_o remains at 5. However, if v_{in} becomes less than -2.5, the output switches to 0.

Similarly, if $v_o = 0$ and if v_{in} is less than 0, v_x is negative, and v_o remains at 0. However, if v_{in} becomes greater than 0, the output switches to +5. The transfer characteristic is shown in Figure 12.15 on page 809.

Exercise 12.4



Current equation at noninverting input:

$$\frac{v_x - v_{in}}{R_1} + \frac{v_x - v_o}{R_2} = 0$$

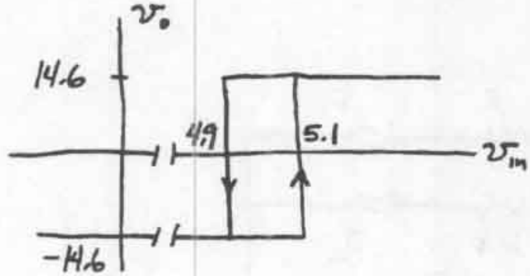
Solve for v_x:

$$v_x = v_{in}\frac{R_2}{R_1+R_2} + v_o\frac{R_1}{R_1+R_2}$$

Also

$$v_y = 15\frac{R_4}{R_3+R_4}$$

Desired transfer characteristic:



For $v_o = -14.6$ $v_x = v_y$ when $v_{in} = 5.1$:

$$5.1\frac{R_2}{R_1+R_2} - 14.6\frac{R_1}{R_1+R_2} = 15\frac{R_4}{R_3+R_4} \qquad (1)$$

For $v_o = +14.6$ $v_x = v_y$ when $v_{in} = 4.9$:

$$4.9\frac{R_2}{R_1+R_2} + 14.6\frac{R_1}{R_1+R_2} = 15\frac{R_4}{R_3+R_4} \qquad (2)$$

Subtract Equation (2) from Equation (1):

$$0.2\frac{R_2}{R_1+R_2} - 29.2\frac{R_1}{R_1+R_2} = 0 \Rightarrow R_2 = 146 R_1$$

Substituting $R_2 = 146 R_1$ into Equation (1) eventually yields

$$R_3 = 2.0205 \times R_4$$

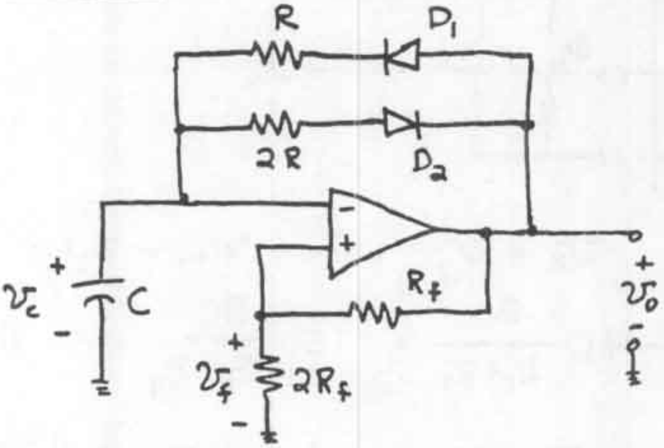
Now we try to find practical 1%-tolerance values such that $R_2 = 146 R_1$ and $R_3 = 2.02 R_4$

One good choice is:

$$R_1 = 6.65\ k\Omega \quad R_2 = 976\ k\Omega$$

$$R_3 = 20\ k\Omega \quad R_4 = 10\ k\Omega$$

Exercise 12.5



For $v_o = +A$ $\quad v_f = \frac{2}{3} A$ and D_1 forward biased

For $v_o = -A$ $\quad v_f = -\frac{2}{3} A$ and D_2 forward biased

(a) Schmitt changes state for $v_c = \pm \frac{2}{3} A$

(b) Waveforms are shown in Figure 12.21 in text.

(c) $\frac{T_L}{T_H} = 2$ because the time constant has a 2:1 ratio due to the diodes.

(d) For $0 < t < T_H$ (See Figure 12.21 in the book.)

$$v_C(t) = K_1 + K_2 e^{-t/RC}$$

$$\left.\begin{array}{l} v_C(0) = -\frac{2A}{3} = K_1 + K_2 \\ v_C(\infty) = A = K_1 \end{array}\right\} \Rightarrow K_2 = -\frac{5A}{3}$$

$$v_C(T_H) = A - \frac{5A}{3} e^{-\frac{T_H}{RC}} = \frac{2A}{3}$$

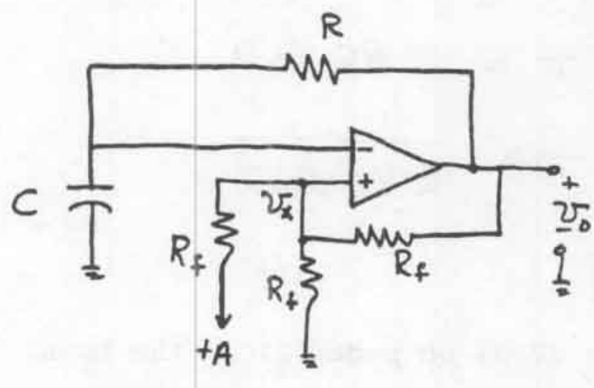
This yields $T_H = RC \ln 5$

Similarly $T_L = 2RC \ln 5$

$T = T_H + T_L = 3RC \ln 5$

$f = \frac{1}{T} = 1/[3RC \ln 5]$

Exercise 12.6



(a) Current equation at noninverting node:

$$\frac{v_x - A}{R_f} + \frac{v_x}{R_f} + \frac{v_x - v_o}{R_f} = 0$$

Solve for $v_x = \frac{1}{3}A + \frac{1}{3}v_o$

For $v_o = A$ switching is at $v_c = v_x = \frac{2}{3}A$

For $v_o = 0$ switching is at $v_c = v_x = \frac{1}{3}A$

(b) The waveforms are shown in Figure 12.23.

(c) $v_c(t) = K_1 + K_2 e^{-t/RC}$

$v_c(0) = \frac{A}{3} = K_1 + K_2$ (See Figure 12.23.)

$v_c(\infty) = A = K_1$

$v_c(t) = A - \frac{2}{3}Ae^{-t/RC}$

$v_c(T/2) = A - \frac{2}{3}Ae^{-T/2RC} = \frac{2A}{3}$

$$e^{-T/2RC} = \frac{1}{2}$$

$$T = 2RC\ln 2$$

$$f = \frac{1}{2RC\ln 2}$$

Exercise 12.7

Refer to Figure 12.27 on page 821 in the book.

(a) $$v_c(t) = K_1 + K_2 e^{-\frac{t}{(R_A+R_B)C}}$$

$$v_c(0) = \frac{V_{cc}}{3} = K_1 + K_2$$

$$v_c(\infty) = V_{cc} = K_1 \qquad \therefore K_2 = -\frac{2}{3}V_{cc}$$

$$v_c(t) = V_{cc} - \frac{2}{3}V_{cc}\, e^{-\frac{t}{(R_A+R_B)C}}$$

(b) $$v_c(T_H) = \frac{2V_{cc}}{3} = V_{cc} - \frac{2}{3}V_{cc}\, e^{-\frac{T_H}{(R_A+R_B)C}}$$

$$e^{-\frac{T_H}{(R_A+R_B)C}} = \frac{1}{2}$$

$$T_H = (R_A+R_B)C \ln 2$$

Exercise 12.8

(a) $$v_c(t) = K_1 e^{-\frac{t}{R_B C}}$$

$$v_c(0) = \frac{2V_{cc}}{3} = K_1$$

$$v_c(t) = \frac{2V_{cc}}{3} e^{-\frac{t}{R_B C}}$$

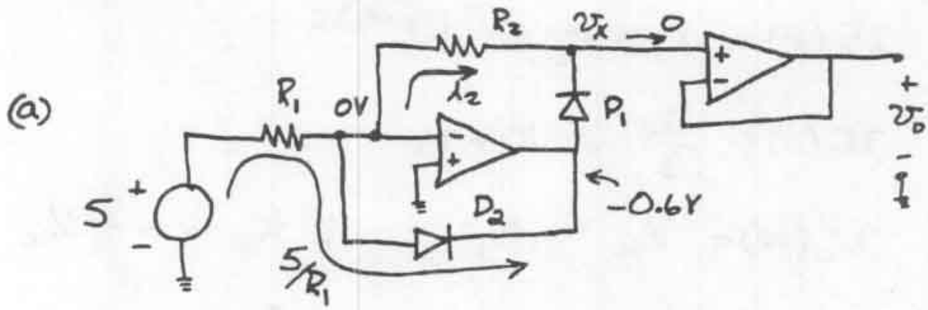
(b) $$v_c(T_L) = \frac{V_{cc}}{3} = \frac{2V_{cc}}{3} e^{-\frac{T_L}{R_B C}}$$

$$e^{-\frac{T_L}{R_B C}} = \frac{1}{2}$$

$$T_L = R_B C \ln 2$$

Exercise 12.9

(a)



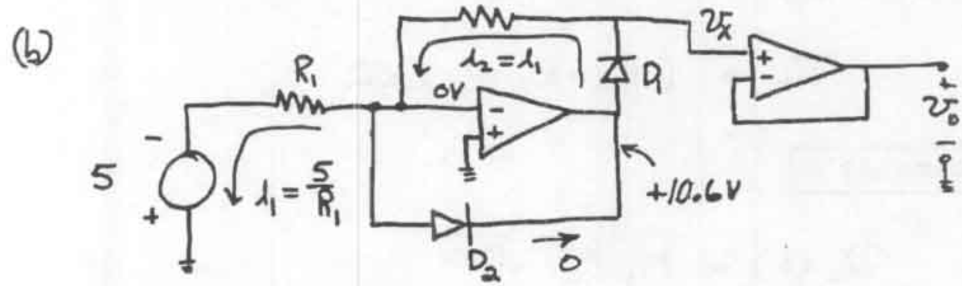
D_2 is forward biased

D_1 is reverse biased

$i_2 = 0 \quad v_x = -R_2 i_2 = 0$

$v_o = v_x = 0$

(b)



D_2 is reverse biased

D_1 is forward biased

$v_x = R_2 i_2 = \frac{R_2}{R_1}(5) = 10V$

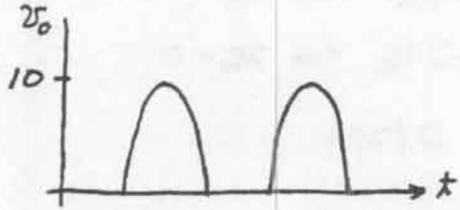
$v_o = v_x = 10V$

(c) Thus we see that

$v_o = 0 \quad \text{for } v_{in} > 0$

$v_o = -2 v_{in} \quad \text{for } v_{in} < 0$

if $v_{in} = 5 \sin \omega t$:



Thus the circuit functions as an ideal half-wave rectifier.

Exercise 12.10

See Figure 12.32 on page 826 in the book.

Exercise 12.11

Refer to Figure 12.31. For the summer we have:

$$v_o = -\frac{R_2}{R_1} v_{in} - 2\frac{R_2}{R_1} v_A \quad (v_A \text{ is voltage at point A})$$

(a) For $v_{in} = +5V$:

D_1 is reverse biased

D_2 is forward biased

$v_A = -v_{in} = -5V$ (output of x_1 is $-5.6V$)

$v_o = -2v_{in} - 2(2)(-v_{in}) = 2v_{in} = 10V$

(b) For $v_{in} = -5V$:

D_1 is forward biased (output of x_1 is $+0.6V$)

D_2 is reverse biased

$v_A = 0$

$v_o = -2v_{in} = +10V$

(c) Thus $v_o = 2v_{in}$ for $v_{in} > 0$

$v_o = -2v_{in}$ for $v_{in} < 0$

or $v_o = 2|v_{in}|$

Exercise 12.12

Refer to Figure 12.34 on page 827 in the book.

The current flowing from the capacitor is $2I_B$ (I_B for each opamp).

$$2I_B = i_c = C\frac{dv_c}{dt} \approx C\frac{\Delta v_c}{\Delta t}$$

(a) $$C = \frac{2I_B \Delta t}{\Delta v_c} = \frac{200\times10^{-9}\times10\times10^{-3}}{10^{-3}} = 2\mu F$$

(b) $$C = \frac{2\times10^{-9}\times10\times10^{-3}}{10^{-3}} = 0.02\mu F$$

Exercise 12.13

See Figure 12.35 on page 829 in the book.

Exercise 12.14

See Figure 12.38 on page 833 in the book.

Exercise 12.15

The minimum sampling rate is twice the highest frequency of the signal. Thus $f_s = 2 \times 18 = 36$ kHz.

Exercise 12.16

There are $N = 2^{12} = 4096$ zones. $\Delta = 10/N = 2.44$ mV.

Exercise 12.17

The data rate is the product of the number of bits per sample and the sampling rate. $8 \times 8 \times 10^3 = 64$ kbit/s.

Exercise 12.18

$$D = d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \ldots + d_n 2^{-n}$$

$$= 0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-5} + 1 \times 2^{-8}$$

$$= 0.41016$$

$$v_o = V_{ref} D = 10 \times 0.41016 = 4.1016 \text{ V}$$

Exercise 12.19

Refer to Figure 12.45 on page 840 in the book. The emitter current of Q_1 is $I_{E1} = V_{ref}/2R$. Then $I_{C1} = \alpha I_{E1} = \alpha V_{ref}/2R$. If d_1 is high, α times this current is steered through the current switch to the inverting input of the op amp. If d_1 is low, the current is steered to ground by the current switch. Thus, the current taken from the inverting op amp input by the first current switch is $d_1 \alpha^2 V_{ref}/2R$ (where we are assuming that $d_1 = 0$ or 1). The analysis for Q_2 is the same, except that the current is half as much. Finally, the sum of the currents flows through R_f, and the output voltage is R_f times the total current, so we can write

$$v_o = V_{ref} \frac{R_f}{R} \alpha^2 D$$

Exercise 12.20

Refer to Figure 12.48 on page 844 in the book. There is an error in the figure. The number of comparators needed is equal to the number of amplitude zones minus one, which is $2^n - 1$, not 2^{n-1} as indicated in the figure. Thus for $n = 8$, the number of comparators is 255, and for $n = 12$, the number of comparators is 4095.

Exercise 12.21

We assume that the largest value allowed for v_s is V_{ref}. Then the maximum conversion time is $2T_1$. Solving the equation given on page 846 for T_1 and doubling its value, we have the maximum conversion time:

$$T_{conv} = 2T_1 = 2RCV_{peak}/v_s = 2RCV_{peak}/V_{ref}$$

Then solving for C and substituting values, we have

$$C = V_{ref}T_{conv}/(2RV_{peak}) = 250 \text{ nF}$$

Exercise 12.22

Each step results in 1 bit of the result. Thus a 12-bit converter requires 12 steps. At 0.2 μs/step, the time required is $T_{conv} = 2.4\ \mu s$. The conversion rate is $f_{conv} = 1/T_{conv} =$ 416.7 kHz.

Problem 12.1

An ideal comparator compares the voltage at its noninverting input with the voltage at its inverting input. If the voltage at the noninverting input is higher (lower) than the voltage at the inverting input, the output of the comparator is high (low). See Figures 12.1 and 12.2 on page 800 in the book.

Problem 12.2

Op amps are frequency compensated so they have good response characteristics and do not oscillate when used with negative feedback. Comparators are not intended to be used with negative feedback, and compensation is not needed. Otherwise, the circuits used for op amps and comparators are similar.

Problem 12.3

If the output stage of a comparator is a BJT with the collector connected to the output terminal (and no internal pull-up resistor), we say that the comparator has an open-collector output. A resistor connected from the collector to the power supply is called a pull-up resistor. Figure 12.4 on page 802 shows an example of such a comparator.

Problem 12.4

Unless positive feedback is used, the output of a comparator can switch many times each time the input signal goes through the reference value, due to noise and/or oscillation. Another problem is that the output may not switch quickly enough.

Problem 12.5

Figures 12.13, 12.14 and 12.15 on pages 808 and 809 in the book show examples of transfer characteristics with hysteresis.

Problem 12.6

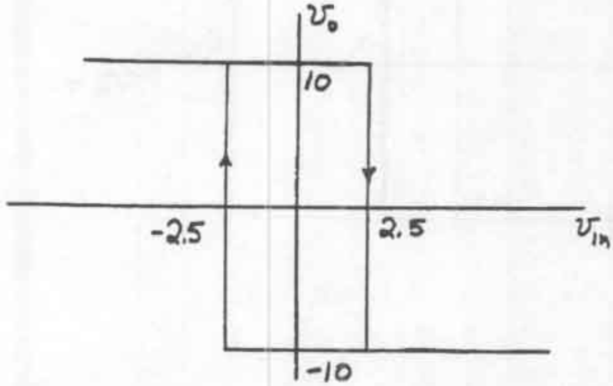
See Figure 12.9 on page 805 in the book.

Problem 12.7

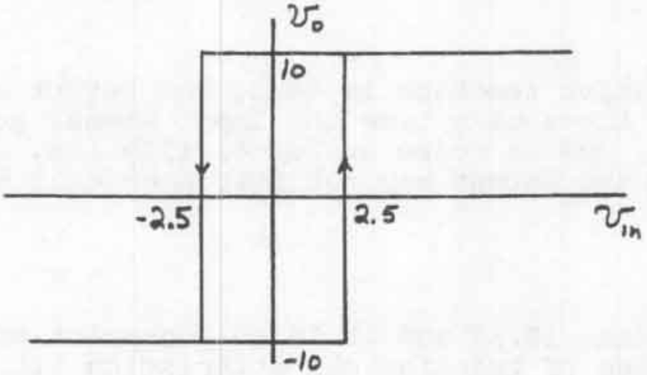
If the resistances are very small, the currents may be too large, resulting in an unnecessary load for the power supply. If the resistances are too large, noise coupled from other circuits can be a problem. Furthermore, large resistances lead to inaccuracy caused by the comparator bias currents. Finally, very large resistances may consume too much chip area if they are to be integrated.

Problem 12.8

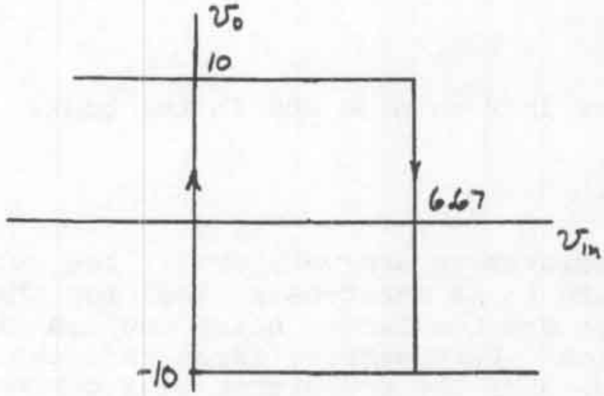
(a)



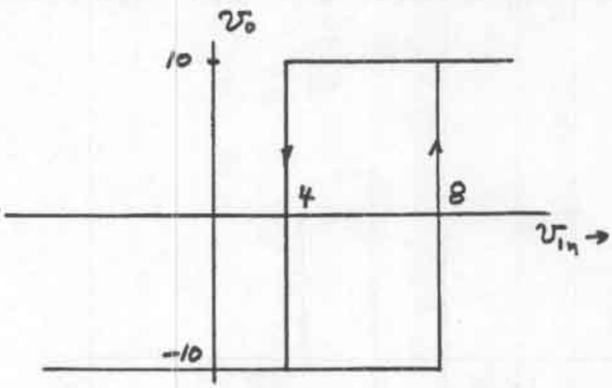
(b)



(c)

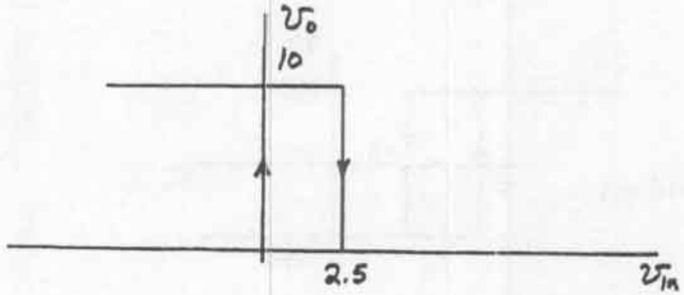


(d)

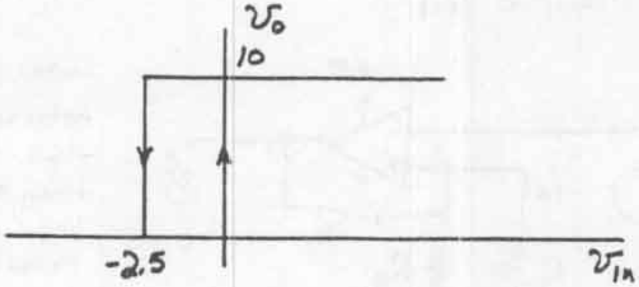


Problem 12.9

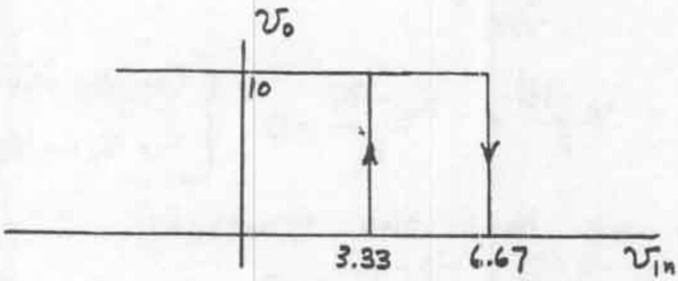
(a)



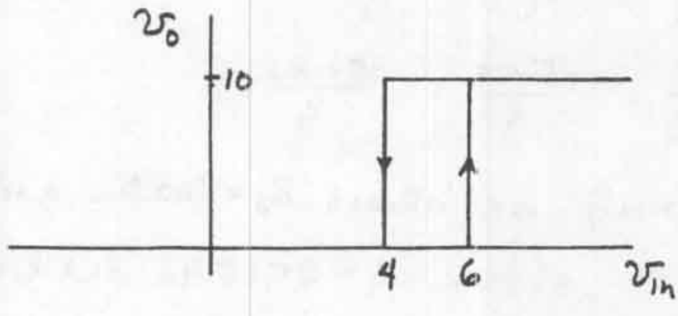
(b)



(c)

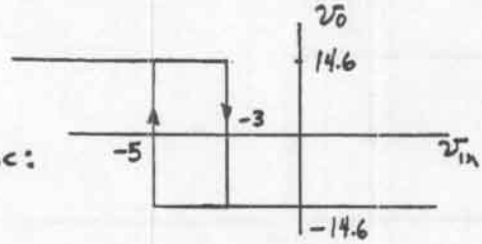


(d)

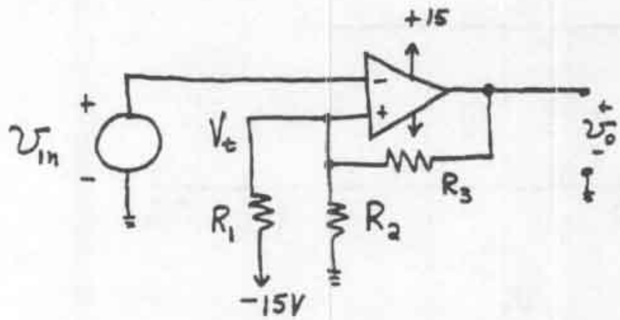


Problem 12.10

Desired characteristic:



Follow Example 12.1



Note: R_1 is returned to -15V rather than +15V because the threshold V's are negative.

$$\frac{V_t}{R_2} + \frac{V_t + 15}{R_1} + \frac{V_t - v_o}{R_3} = 0 \quad \begin{cases} \text{For } v_o = 14.6 \quad V_t = -3 \\ \text{For } v_o = -14.6 \quad V_t = -5 \end{cases}$$

Thus we have two equations:

$$\frac{-3}{R_2} + \frac{-3+15}{R_1} + \frac{-3-14.6}{R_3} = 0$$

$$\frac{-5}{R_2} + \frac{-5+15}{R_1} + \frac{-5+14.6}{R_3} = 0$$

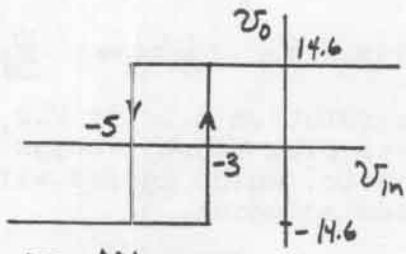
Arbitrarily we choose $R_3 = 100\,k\Omega$ and solve to obtain $R_1 = 25.68\,k\Omega$ and $R_2 = 10.30\,k\Omega$

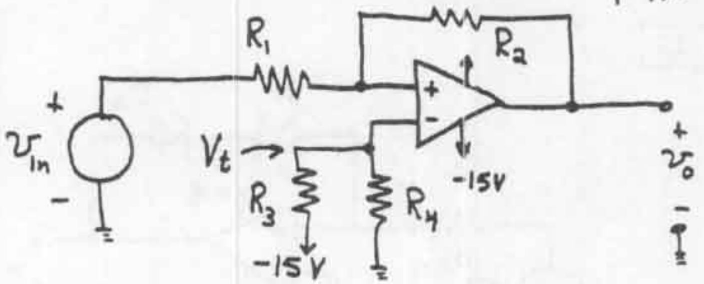
Finally we choose the nearest 1-% tolerance values: $R_1 = 25.5\,k\Omega$ and $R_2 = 10.2\,k\Omega$

The simulation file is P12_10. After we run the program we use Probe to plot V(out) versus V(in) and obtain the transfer characteristic, which agrees with the sketch shown above.

Problem 12.11

Desired characteristic:





At the switching points, the voltage at node 2 must equal V_t. Writing a current equation at node 2:

$$\frac{v_{in} - V_t}{R_1} = \frac{V_t - v_o}{R_2} \quad \begin{cases} \text{For } v_o = 14.6 & v_{in} = -5 \\ \text{For } v_o = -14.6 & v_{in} = -3 \end{cases}$$

Thus we have two equations:

$$\frac{-5 - V_t}{R_1} = \frac{V_t - 14.6}{R_2} \quad \text{and} \quad \frac{-3 - V_t}{R_1} = \frac{V_t + 14.6}{R_2}$$

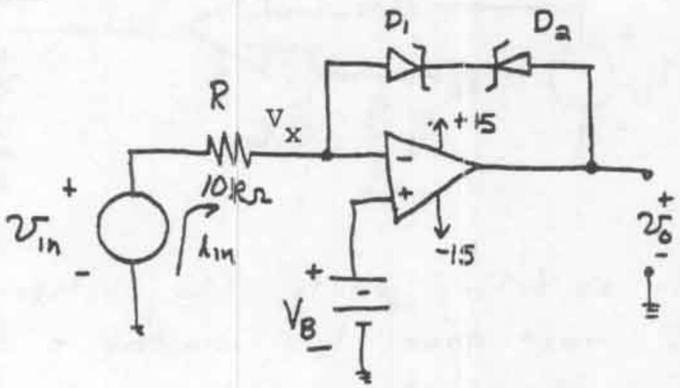
Arbitrarily we choose $\underline{R_1 = 10\,k\Omega}$, then solve for $R_2 = 146\,k\Omega$ and $V_t = -3.74V$. We choose the standard value $\underline{R_2 = 147\,k\Omega}$. Next we have

$$V_t = -3.74 = -15\frac{R_4}{R_3 + R_4}$$

Arbitrarily we choose $R_4 = 10\ k\Omega$ and then solve to obtain $R_3 = 30.1\ k\Omega$.

The simulation file is P12_11. After we run the program, we use Probe to plot V(out) versus V(in) and obtain the transfer characteristic, which agrees with the sketch shown earlier in this problem solution.

Problem 12.12



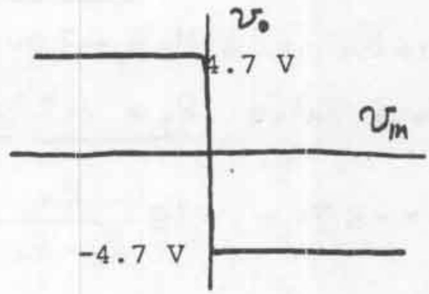
The circuit has negative feedback. Therefore $V_x = V_B$. We have $i_{in} = (v_{in} - V_B)/R$, and i_{in} flows through the diodes. For $v_{in} > V_B$, D_1 is forward biased and D_2 is in reverse breakdown. We have:

$$v_o = V_B + 4.7 \text{ for } v_{in} > V_B$$

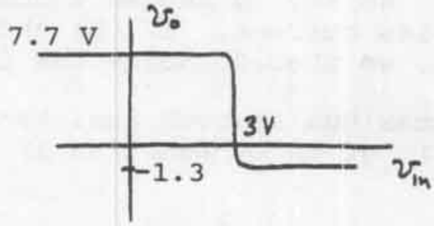
On the other hand, for $v_{in} < V_B$, D_1 is in reverse breakdown and D_2 is forward biased. Then we have:

$$v_o = V_B - 4.7 \text{ for } v_{in} > V_B$$

For $V_B = 0$:



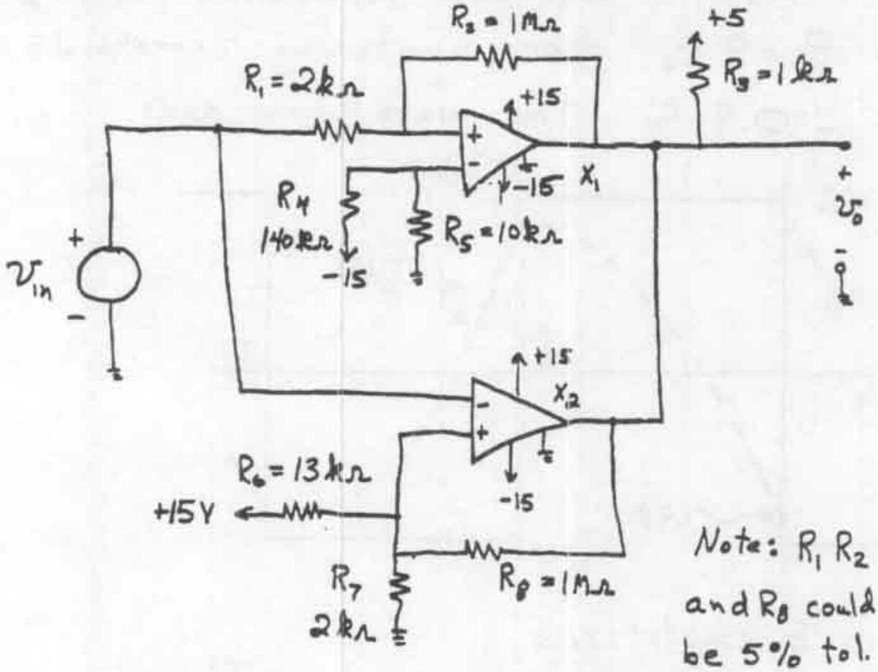
For $V_B = 3$ V:



The simulation file is P12_12.

Problem 12.13

Here is one solution for the problem:



R_1, R_2, and R_8 can be 5%-tolerance. The remaining resistors should be 1%. The Schematic file is P12_13.

Problem 12.14

See Figure 12.16 on page 810 in the book.

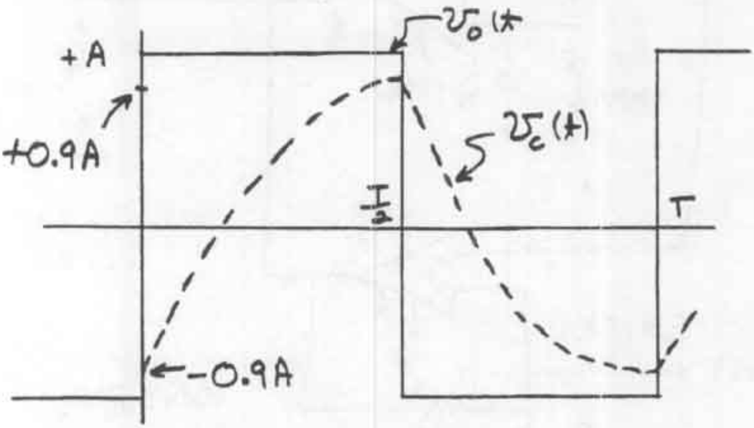
Problem 12.15

(a) To achieve very low frequency, we need to choose large values for R and C. Thus, the charging current for the capacitor will be very small. We should choose a comparator with the smallest possible bias current. If the choice is between the μA741 and the LF411, we should choose the LF411.

(b) We choose the maximum allowed resistance and capacitance. Then the frequency is given by Equation 12.7 on page 812.

$$f = \frac{1}{2RC\ln(3)} = \frac{1}{2(20 \times 10^6)10^{-6}\ln(3)} = 0.0228 \text{ Hz}$$

(c) For a longer period we want to raise the threshold voltage. $\therefore$ choose $R_1 > R_2$. For $R_1 = 9R_2$ the switching thresholds are at $\pm 0.9A$ The waveforms are:



As in Example 12.2:

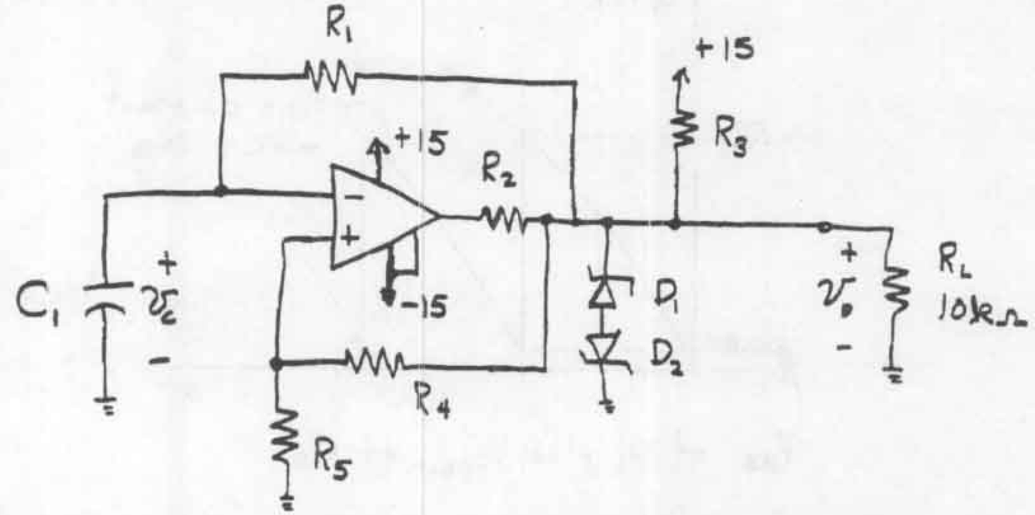
$$v_c(T/2) = 0.9A = A - 1.9Ae^{-T/2RC}$$

$$f = \frac{1}{T} = \frac{1}{2RC\ln(19)} = 0.00849 \text{ Hz}$$

(d) The problem is that if the comparator bias current is large or if the capacitor is leaky, the period will be affected.

Problem 12.16

Here is one solution:



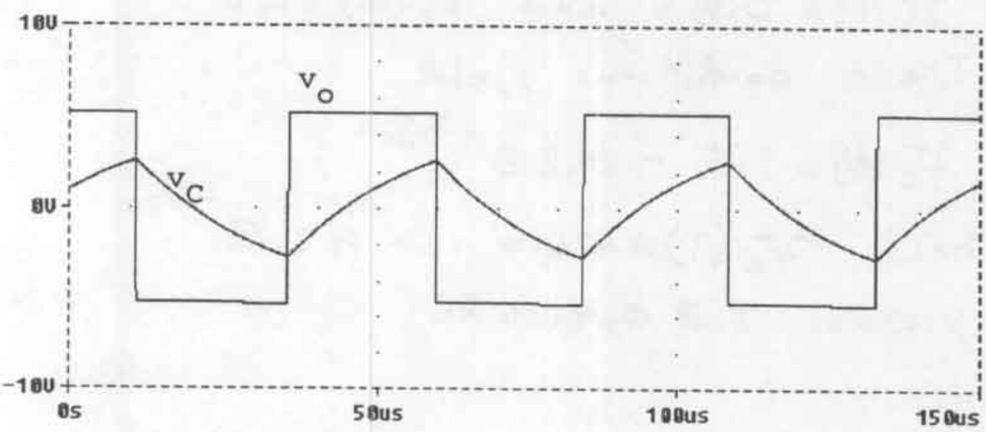
$$\text{Choose } C_1 = 1000\text{pF} \quad \text{than } R_1 = \frac{1}{2fC\ln(3)} = 22.7\text{k}\Omega$$

choose $R_1 = 22\text{k}\Omega$

$R_4 = R_5 = 100\text{k}\Omega \qquad R_3 = 4.7\text{k}\Omega$

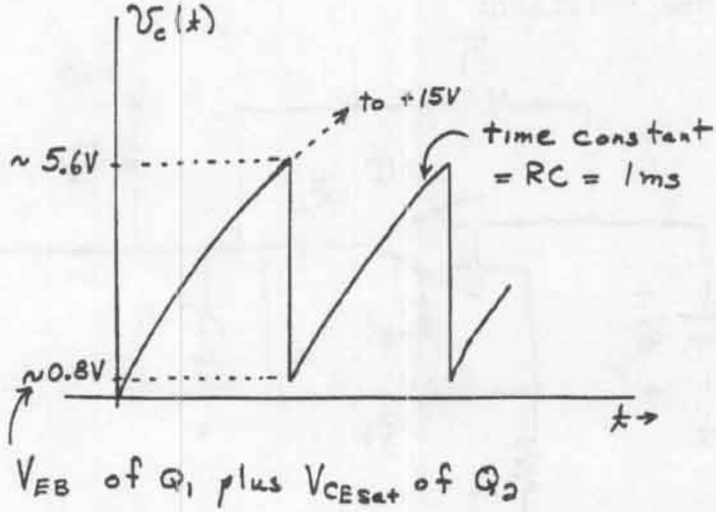
$D_1 = D_2 = 1N750 \qquad R_2 = 1.5\text{k}\Omega$

The simulation file is P12_16. (It is necessary to specify a nonzero initial condition on the capacitor for the circuit operation to start rapidly.) Waveforms from the simulation:



Problem 12.17

(a)



(b) The simulation file is P12_17. The voltage across the capacitor is very similar to the sketch shown in part (a).

(c) First redefine $t=0$ to be at the start of the second cycle (because the first cycle is not typical). Then

$$v_c(t) = A + Be^{-t/RC}$$

but

$$v_c(0) \cong 0.8\,V \quad \text{and} \quad v_c(\infty) = 15\,V$$

These conditions yield

$$v_c(t) = 15 - 14.2e^{-t/RC}$$

now $v_c(T) \cong 5.6 = 15 - 14.2\,e^{-T/RC}$

yields $T \cong 0.4125\,RC$

$$f = 1/T = \frac{1}{0.4125\,RC} = 2.42\ kHz$$

(d) Neglecting the base current of Q_1 we have $I_{C2} \approx \frac{V_{CC} - 0.2}{R_2}$ (we have also neglected the current in R_1). Assuming that the transistors are saturated and that the current from C has fallen to zero, we have $I_{B2} \approx I_{E1} \approx \frac{V_{CC} - 0.8}{R}$. Now for Q_2 to remain in saturation, we must have

$$I_{C2} < \beta_2 I_{B2}$$

$$\frac{V_{CC} - 0.2}{R_2} < \beta_2 \frac{V_{CC} - 0.8}{R}$$

Assuming that $V_{CC} \gg 0.8V$ this simplifies to $R < \beta_2 R_2$. Thus for oscillations to continue, we must have $R > \beta_2 R_2$. To demonstrate reduce the value of R to 100 kΩ and run the program. After the first cycle, the transistors remain in saturation.

Problem 12.18

Each time a monostable multivibrator is triggered, it produces a single output pulse of predetermined duration. See Figure 12.25(b) on page 819 in the book for typical waveforms.

Problem 12.19

See Figure 12.24 and the related discussion on pages 817 and 818 in the book.

Problem 12.20

The duration of the pulse is the time that it takes for C to charge to $2V_{CC}/3$ starting from zero. Define $t = 0$ as the beginning of the transient. Then we have

$$v_C(t) = V_{CC} - V_{CC}\exp(-t/R_AC)$$

Then at $t = T$ we have

$$v_C(T) = 2V_{CC}/3 = V_{CC} - V_{CC}\exp(-T/R_AC)$$

$$\exp(-T/R_AC) = 1/3$$

$$-T/R_AC = \ln(1/3) = -\ln(3)$$

$$T = R_AC\ln(3)$$

Problem 12.21

The circuit is shown in Figure 12.25 on page 819 in the book. We pick $C = 10\ \mu F$ and then we compute R_A using Equation 12.8.

$$R_A = \frac{T}{C\ln(3)} = \frac{1}{10^{-6}\ln(3)} = 910\ k\Omega$$

This happens to be a standard value for 5%-tolerance resistors.

Other values of components will also work. However, R_A should not be larger than a few megohms or the current taken by the discharge and threshold inputs will affect the pulse duration too much. Usually, we want to keep C small so it does not occupy too much volume.

Problem 12.22

The circuit diagram is shown in Figure 12.26 on page 820 in the book. The duty ratio d is given by Equation 12.15:

$$d = 75\% = \frac{R_A + R_B}{R_A + 2R_B} \times 100\%$$

Solving we find $R_A = 2R_B$.

The frequency is given by Equation 12.13.

$$f = \frac{1}{(R_A + 2R_B)C\ln(2)}$$

Let us select $C = 0.1\ \mu F$. Then we have

$$R_A + 2R_B = \frac{1}{fC\ln(2)} = \frac{1}{2000 \times 10^{-7}\ln(2)} = 7.213\ k\Omega$$

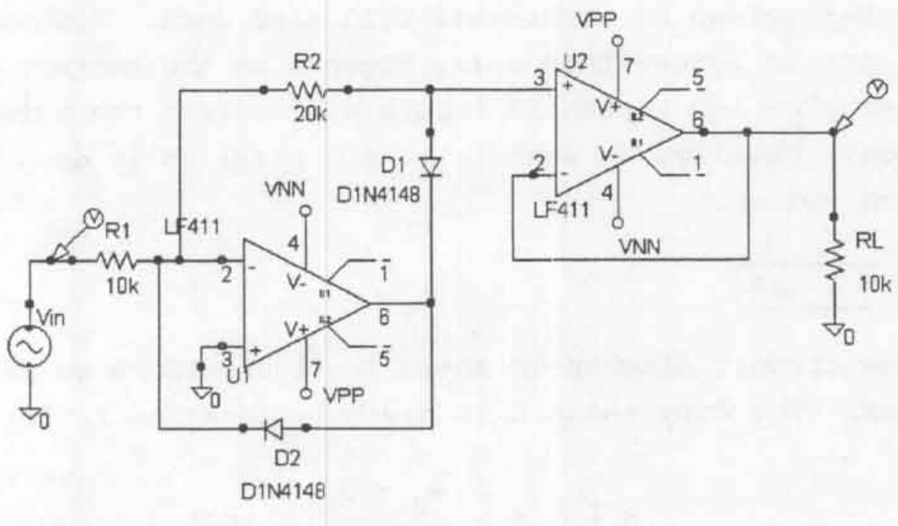
Finally, using $R_A = 2R_B$, we obtain $R_A = 3.6\ k\Omega$ and $R_B = 1.8\ k\Omega$. These are standard values for 5%-tolerance resistors.

Problem 12.23

We use a precision rectifier in instrumentation applications where accuracy is important. We use simple rectifiers for power supplies, in high-frequency applications, and where accuracy is less important.

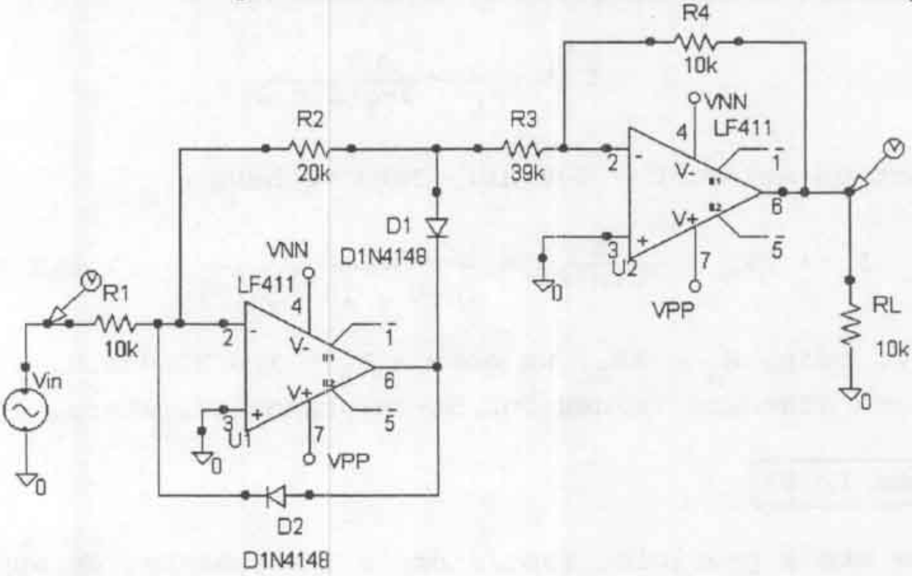
Problem 12.24

One solution is shown on the next page. The simulation shows that the desired waveform is produced. The simulation file is P12_24.



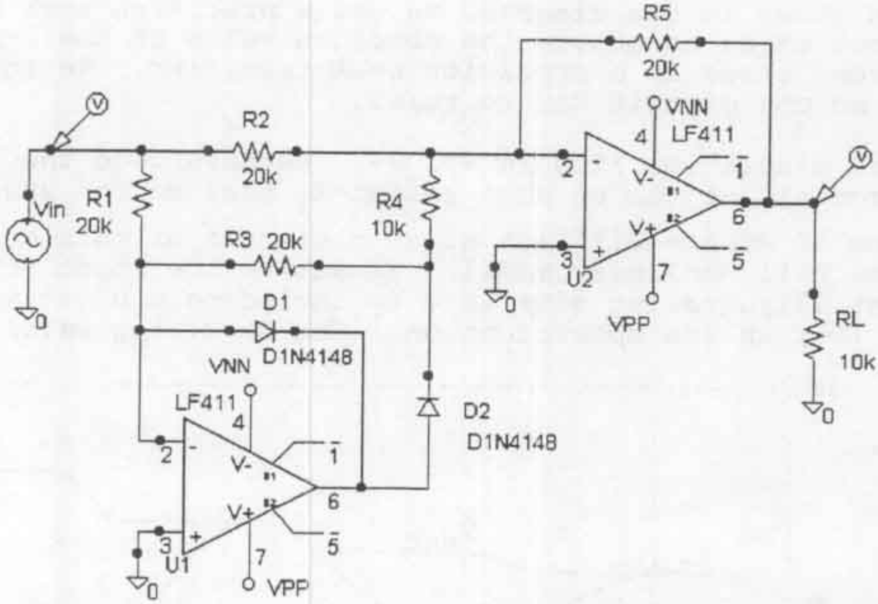
Problem 12.25

One solution is shown below. The simulation shows that the desired waveform is produced. The simulation file is P12_25.



Problem 12.26

One solution is shown on the next page. The simulation shows that the desired waveform is produced. The simulation file is P12_26.



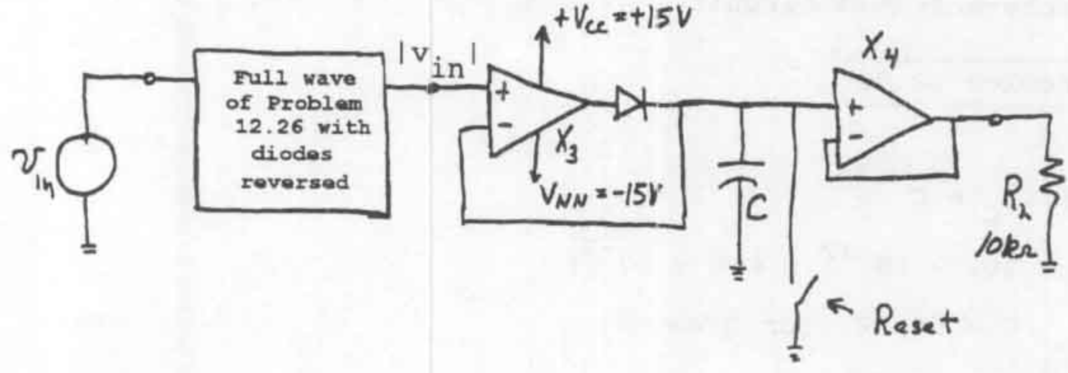
Problem 12.27

A peak detector produces an output that is equal to the previous peak value of the input signal. A circuit for a simple peak detector is shown in Figure 12.33 and a precision peak detector is shown in Figure 12.34 on page 827.

Problem 12.28

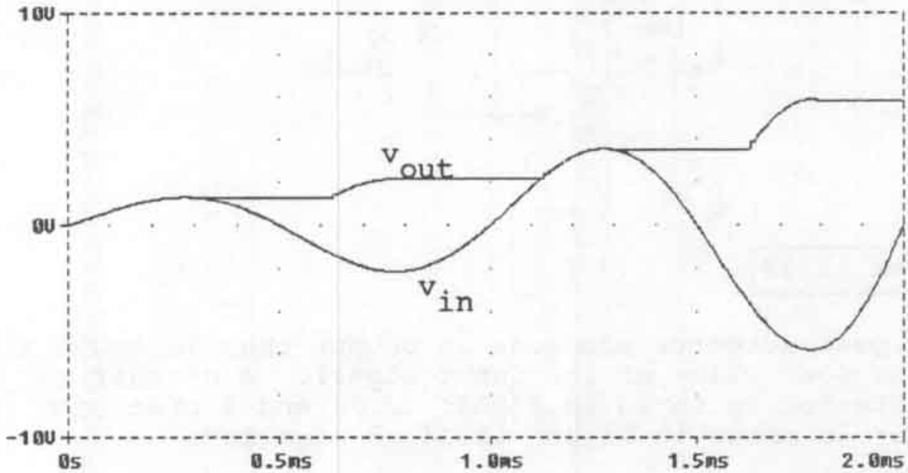
To modify the circuit of Figure 12.34 to produce an output that is the previous minimum value of the input voltage, we simply need to reverse the connections to the diode.

Problem 12.29



As shown in the diagram, we use a precision peak detector as the first stage to obtain the absolute value of the input signal. The second stage is a precision peak rectifier. We include a switch so the circuit can be reset.

The simulation file is P12_29. We have used the linear model for all of the op amps except X_3 because the student versions of PSpice will not allow a circuit of this complexity with the full nonlinear model. We set up the input source as an exponentially growing sine wave by including a negative damping factor (DF) in its specification. The resulting waveforms are:



Problem 12.30

A sample-and-hold circuit has two modes. In the sample (or track) mode, the output follows the input signal. In the hold (or store) state, the output is constant and equal to the value of the input immediately prior to entering the hold state.

See Figure 12.36 on page 830 for the circuit diagram of a sample-and-hold circuit.

Problem 12.31

(a) $i_C = C \dfrac{dv_C}{dt}$

$$100 \times 10^{-12} = C(2 \times 10^{-3})$$

$$C = 50 \text{ nF} \quad \text{(or greater)}$$

(b) maximum acquisition time $\cong \dfrac{|\Delta v_o|_{max} \times C}{|i_C|}$

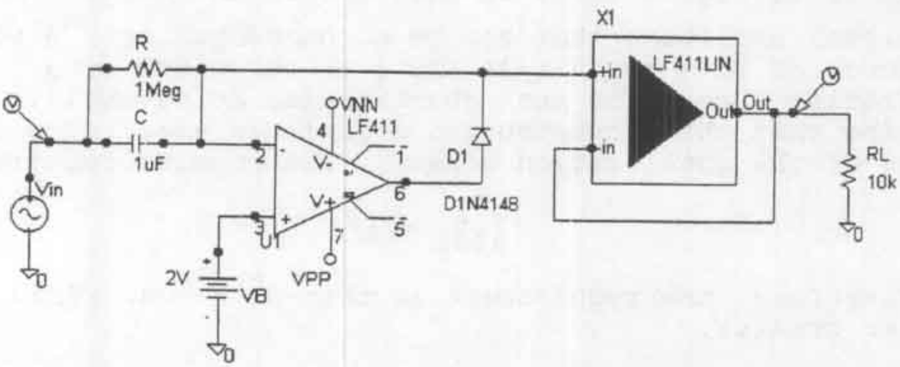
$$= \frac{10 \times 50 \times 10^{-9}}{10 \text{ mA}}$$

$$= 50\ \mu s$$

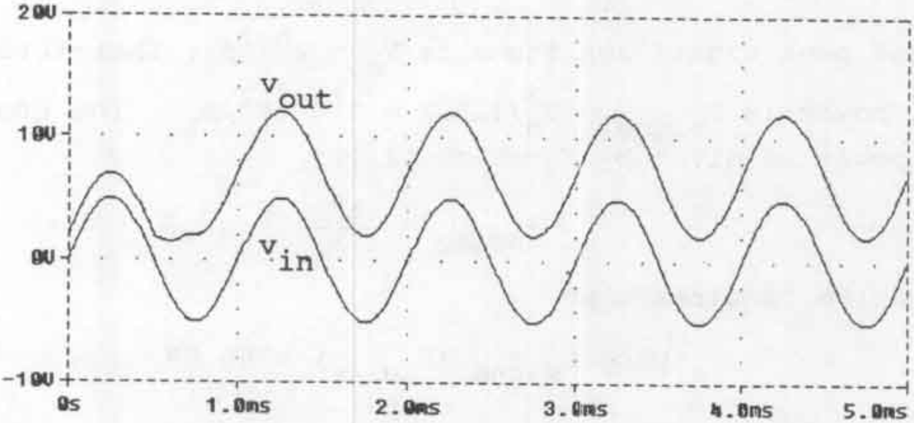
Problem 12.32

A clamp circuit produces an output that is equal to the input plus a constant. The constant is adjusted so the positive (or negative) extreme of the output is a predetermined value. The circuit diagram of a precision clamp circuit is shown in Figure 12.37 on page 831 in the book.

Problem 12.33



The simulation file is P12_33. Other values of R and C will work as long as the RC time constant is long compared to the period of the input. The input and output waveforms are:



Notice that the first cycle is distorted but after that the circuit performs as desired.

Problem 12.34

The primary consideration for the sampling rate is the frequency distribution of the significant components of the input signal. The sampling rate should be at least twice the highest frequency.

The primary consideration for the number of bits per sample is the amount of quantization noise that can be tolerated.

Problem 12.35

The sampling rate is $1.5 \times 2 \times f_H = 300$ Hz.

Refer to Figure 12.39 on page 834 in the book. The peak-to-peak signal amplitude that can be accommodated is $2^n\Delta$ where n is the number of bits per sample and Δ is the width of a quantization zone. The peak quantization noise amplitude is $\Delta/2$ (assuming that the reconstructed signal has amplitudes in the centers of the quantization zones). The problem requires that

$$\frac{2^n\Delta}{1000} = \Delta/2$$

Therefore, the requirement is that $2^n \geq 500$. This requires $n = 9$ or greater.

The data rate is (300 samples/s) $\times$ (9 bits/sample) = 2700 bits per second.

Problem 12.36

The peak signal amplitude is $V_m = 2^{n-1}\Delta$. Therefore, the signal power is $P_{signal} = V_m^2/(2R_L) = 2^{2n-3}\Delta^2/R_L$. The quantization noise power is given by Equation 12.18.

$$P_{noise} = \frac{\Delta^2}{12R_L}$$

The problem requires that

$$10\log(P_{signal}/P_{noise}) = 50 \text{ dB}$$

$$P_{signal} = 10^5 P_{noise}$$

$$\frac{2^{2n-3}\Delta^2}{R_L} = 10^5 \frac{\Delta^2}{12R_L}$$

$$2^{2n-3} = 8333$$

$$(2n-3)\log(2) = \log(8333)$$

From which we obtain $n \cong 8$.

Problem 12.37

(a) For a sine wave, we have $V_{rms} = V_{peak}/\sqrt{2}$. Therefore the peak factor is $V_{peak}/V_{rms} = \sqrt{2}$.

(b) The ADC can accommodate the same V_{peak} for both the sine wave and the music waveform. We can write

$$V_{peak} = \sqrt{2}V_{rms,sine} = 100V_{rms,music}$$

Squaring both sides and dividing by the load resistance:

$$\frac{2V^2_{rms,sine}}{R_L} = \frac{10^4 V^2_{rms,music}}{R_L}$$

$$P_{sine} = 5000P_{music}$$

$$SNR_{music} = \frac{P_{music}}{P_{noise}} = \frac{P_{sine}}{P_{noise}} \times \frac{P_{music}}{P_{sine}} = \frac{P_{sine}}{P_{noise}} \times \frac{1}{5000}$$

In decibels this becomes:

$$SNR_{music,dB} = SNR_{sine,dB} - 37 \text{ dB}$$

For a sine wave the SNR is given by Equation 12.23, so we have:

$$SNR_{music,dB} = 6n - 35.2 \text{ dB}$$

For $SNR_{music,dB}$ to exceed 60 dB, we need $n \geq 16$.

Problem 12.38

The weighted resistance DAC contains a wide range of resistances. If the same material is to be used, the larger resistances need a large L/W ratio. W cannot be made smaller than the minimum that the process can provide. Thus L must be large and the resistors consume large amounts of chip area. (Using a wide range of materials is not practical.)

On the other hand, the R-2R DAC requires only a 2-to-1 ratio of resistances, and all of the resistors can have W/L close to unity so they consume relatively little chip area.

Problem 12.39

If the switches did not connect to ground, the current through the V_{ref} source would vary greatly depending on the switch settings. Practical sources have internal resistance and variable current would cause V_{ref} to vary resulting in inaccuracies in the analog output.

Problem 12.40

The current flowing through the weighted resistances is:

$$i_o = V_{ref}/R + V_{ref}/2R + V_{ref}/4R + \ldots$$

$$= 10 + 5 + 2.5 + 1.25 + 0.625 + \ldots$$

19.92 mA

$$v_o = i_o R/2$$

$$= 9.96 \text{ V}$$

Problem 12.41

For the weighted resistance DAC of Figure 12.42 on page 838, the total resistance is:

$$R + 2R + 4R + \ldots 128R = 255R$$

Because each R-Ω resistor consumes 100 $(\mu m)^2$, the resistances consume 25,500 $(\mu m)^2$.

For the R-2R DAC of Figure 12.44 on page 840, a total of 7 resistors of value R and 9 resistors of value 2R are needed. Thus the total resistance is 25 R and the area consumed is 2500 $(\mu m)^2$. Notice that the R-2R DAC consumes much less chip area.

Problem 12.42

(a) V_b must be high enough so that all of the transistors can operate in the active region. The negative power supply terminal is at -15 V. Because $V_{ref} = 5$ and $V_{BE} = 0.7$, the bases of Q_1, Q_2, etc. are at -9.3 V. As a minimum the collectors of Q_1, Q_2, etc. should be at the same voltages as the bases. Thus, the bases of the switching transistors must be at -8.6 V as a minimum. On the other hand the bases of the switching transistors should not be at a higher voltage than that of the collectors of the switching transistors. Since the collectors are at 0 V due to the op amp, the upper limit for the base voltages is zero. Furthermore, we must allow for d_1, d_2, etc. to be at least several tenths of a volt higher than V_b. Thus the allowed range is $-8.6 < V_b < 0.2$.

(b) If we select $V_b = -5$ V, the suitable logic-high range for d_1, d_2, etc. runs from about -4.8 V to 0 V. (Approximately 0.2 V differential is sufficient to steer the current.) The range for the low state is downward from -5.2 V. However the low logic level should not be so low that breakdown of the base--emitter junctions may occur. Typically the base--emitter breakdown voltage is about 6 V in magnitude. To be on the safe side, we design for a maximum base-emitter reverse voltage of 3 V. Thus, a reasonable range for the low state is -5.2 to -8V.

(c) Using Equation 12.26 on page 841, we have

$$v_o = V_{ref}\frac{R_f}{R}\alpha^2 D$$

$$= 5\frac{1000}{1000}(0.99)^2(0.5 + 0.25)$$

$$= 3.675 \text{ V}$$

Problem 12.43

In the weighted resistance DAC shown in Figure 12.42 on page 838, the most critical resistance is the left-most one, whose value we denote in this solution as R_{left} which has a nominal value of R. For this circuit, the smallest increment in the output voltage occurs when switch d_n changes. Then the change in the current is

$$\Delta i_o = \frac{V_{ref}}{R2^{n-1}} = \frac{V_{ref}}{128R}$$

The current through the left-most resistor must be within $\Delta i_o/2$ of its nominal value, which is V_{ref}/R.

$$V_{ref}/R_{left} = V_{ref}/R \pm V_{ref}/(256R)$$

$$R_{left} = \frac{256R}{256 \pm 1} = R \pm 0.39\%$$

Of course, the other resistors will also contribute to inaccuracy of the output, so tolerances of about ±0.2% would be needed overall.

Problem 12.44

In the weighted resistance DAC of Figure 12.42, the current drawn from the reference source is

$$I_{ref} = V_{ref}[1/R + 1/(2R) + ... + 1/(2^{n-1}R)]$$

$$= V_{ref}(2 - 2^{1-n})/R$$

Thus the resistance seen by the reference source is

$$R_{load} = \frac{V_{ref}}{I_{ref}} = \frac{R}{2 - 2^{1-n}}$$

In the R--2R DAC of Figure 12.44, the resistance seen by the reference source is $R_{load} = R$.

Problem 12.45

A flash ADC is best if high speed is the primary consideration. Usually a dual-slope ADC is best if accuracy is the primary consideration.

Problem 12.46

The interval T_1 corresponds to a count of 2^{18} which requires $2^{18}T_{clock} = 2^{18}(0.2\ \mu s) = 52.43$ ms. Conversion can take up to $2T_1 = 0.105$s which corresponds to a conversion rate of 9.53 Hz.

Refer to Figure 12.50 on page 846 in the book. The slope of v_x is $v_s/(RC) = V_{peak}/T_1$. Solving for C and substituting values we have

$$C = v_sT_1/(RV_{peak}) = 10(52.43 \times 10^{-3})/(1000 \times 10)$$

$$= 52.43\ \mu F$$

(Larger R and smaller C would be more practical.)

The accuracy of the converter is independent of R within reasonable limits. If R increases, V_{peak} will decrease.

Problem 12.47

The diagram of the flash converter is shown in Figure 12.48 on page 844 in the book. Because the peak signal is 5 V, we choose V_{ref} = 5 V so the entire range of the converter is utilized. Any value of R in the range from 1 kΩ to 10 kΩ is suitable. The number of comparators indicated in the figure is in error (at least for the first printing). The number of comparators should be $2^n - 1$. For n = 4, a total of 15 comparators are needed. The truth table for the decoding logic is:

Input to decoding logic read from top to bottom	$d_1d_2d_3d_4$
111111111111111	0000
111111111111110	0001
111111111111100	0010
111111111111000	0011
111111111110000	0100
.	
.	
.	
100000000000000	1110
000000000000000	1111
Other combinations	Don't care

Errata for the first printing of *Electronics*, 2^{nd} edition
by Allan R. Hambley

Page	Location	Correction (underlined)
ix	Line 5	…Chapters 4 and 5 can be reversed…
80	Figure 2.23	Delete the vertical line through the voltage source v_1.
83	Sentence above Equation 2.25	The voltage across R_1 is given by
125	D2.33 line 8	$W_{space} = 10\ \mu m$. (For consistency with the solutions manual.)
301	First margin comment	using SPICE to play with circuits.
476	Problem 7.20 line 5	percentage does I_{C2} change?
476	Problem 7.22 line 3	Derive an expression for the current I_O for the circuit
479	Problem 7.38 line 2	Figure P7.38. Allow…
563	Line 4	Interchange *pnp* and *npn*.
592	Lines 9 and 10	…R_{if} = 24.6 MΩ
651	D9.40 line 2	Insert magnitude bars around beta: $\lvert\beta\rvert$
651	D9.49 line 3	…with a gain magnitude …
653	Problem 9.78	Should refer to Problem 9.76 rather than Problem 9.75.
703	Equation 10.49	Replace $\frac{R_2}{R_1 + R_2}$ with $\frac{R_1 + R_2}{R_2}$.
717	Line 6	10.8 Repeat Example 10.8, …
721	Problem 10.10	The third sentence of the problem should read: "The case-to-sink thermal resistance is $\theta_{CS} = 0.5^{N}C/W$."
725	Hint for problem D10.50	The input terminals do not need to be interchanged.
750	Line 2 from bottom	f_L = 6.96 MHz
777	Line 12	R_L = -1.875 MΩ
791	Problem 11.2	Write the transfer function magnitude…
844	Figure 12.48	There are $2^n - 1$ comparators not 2^{n-1} as indicated in the figure.

852	Problem 12.17 line 9	Replace v_2 with v_1.

Please contact the author at arhamble@mtu.edu with any additional corrections.